2.77 kV/m/s^2 Sensitivity Digital Demodulator-Decimator-Filter on Xilinx Spartan-7 FPGA for sub-Hz Aerospace Nano-Gravimetry Accelerometers down to 10 nm/s^2

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Abstract—Nano-gravimetry accelerometers read-out front ends for aerospace gravimetry measurements require both accurate analog and digital signal processing to extract with ultra-low noise power (< 5 nV_{RMS} at 1 Hz bandwidth) the weak sub-Hz acceleration signal. To migrate toward fully integrated monolithic silicon systems, such weak acceleration signal requires advanced analog and digital signal processing techniques: an analog low-noise amplification and digitization, and digital precise demodulation and filtering with a strong (x100 power w.r.t. sub-Hz acceleration) rejection of the non-scientifically relevant out-of-band acceleration interferers. This paper focuses on the digital signal conditioning section composed of demodulation, decimation and filtering stages. To validate the proposed design, we designed an analog front end that amplifies, filters, and digitizes acceleration signals produced by an emulated sensor. The complete design and behavioral/electrical characterization are presented and deployed on a Digilent CMOD S7 35T evaluation board mounting the cost-optimized Spartan-7 FPGA. The digital demodulator, decimator, and filter stages reconstruct the minimum amplified signal of 10 nm/s^2 at 1 Hz with a measured SNR of 12.2 and 12.4 dB with and without the out-of-band interferers respectively.

Index Terms—Aerospace Applications, Digital Integrated Circuits, Digital Signal Processors, Gravimetry.

I. INTRODUCTION

The Italian Spring Accelerometer (ISA) is a three-axis accelerometer designed to directly measure the total non-gravitational acceleration acting on the spacecraft [1]. Each ISA's element measures a one-dimensional, orthogonal component of the overall acceleration acting on a spacecraft, making it an a-posteriori drag-free satellite, where non-gravitational forces are measured and compensated. Each sensor's core consists of a proof mass attached to an external structure via a tiny spring and surrounded by a pair of symmetrical electrodes, forming a capacitor that senses any acceleration that causes the mass displacement by a proportional modulation of the polarization voltage. The ISA performance requirements were derived from the need to recover Mercury's gravity field with a spatial resolution of about 300 km [2]. To achieve this, the orbit must be known with an accuracy of at least 1 m in the along-track direction over one Mercury planetary orbital revolution (8355 s), equivalent to an along-track acceleration accuracy of about 10 nm/s^2 [1-4]. The accelerometer's sensitivity is particularly crucial in the sub-Hz frequency domain down to 10^{-4} Hz, where it must overcome various noise sources including thermal disturbances at the spacecraft-accelerometer interface and tracking errors [1,3]. Furthermore, the accelerometer band extend to 10 Hz, where non-relevant acceleration signals are higher in power (up to 100 µm/s^2) [2,4].

State-of-the-art manages such stringent specifications in terms of noise (< 5 nV_{RMS}) and bandwidth (< 1 Hz) by advanced system-level solutions with very large sensitivity and output signal-to-noise-ratio (SNR) [3]. This has implied throughout the last decades to adopt dedicated discrete off-the-shelf JFET components for low noise amplification and digitalization, which are not compatible with very large scale integration (VLSI). Moreover, to reject dominant low frequency 1/f noise acceleration, signals are typically modulated by analog sinewaves provided by large area transformers at 10 kHz modulation frequency, where coherently JFET electronics does not introduce significant 1/f noise power [5]. To open advanced scenarios in terms of VLSI, some key aspects must be addressed: the analog sinusoidal carrier must be replaced with digital-oriented switching modulation, while its frequency must be increased above the higher 1/f flicker noise (> 1 MHz) of nanometric CMOS technologies (65 and 28 nm).

This letter focusses on Digital Signal Processor (DSP) development. We propose transient noise SPICE simulations within the Cadence environment to emulate the nano-gravity acceleration signal produced by the ISA gravimetry accelerometer, alongside an analog front-end that amplifies and digitizes it. We then introduce the DSP implementation designed to reconstruct the weak acceleration signal of interest, targeting the cost-effective AMD Spartan-7 FPGA. The fully-integer arithmetic DSP processes the signal through a digital demodulation stage followed by decimation and filtering achieved with a Cascaded Integrator-Comb (CIC) filter. Finally, the DSP isolates the weak acceleration signals down to a few nm/s^2 within the sub-Hz target frequency band through a finite impulse response (FIR) filter. Fig. 1 shows the full system, with the analog signal conditioning performed in Cadence, the demodulation, decimation, and filtering designed in HDL and implemented on FPGA, and the post-calibration reconstruction in the floating-point domain. Also, various test-points are indicated and used to show and monitor the various stages output throughout the work.

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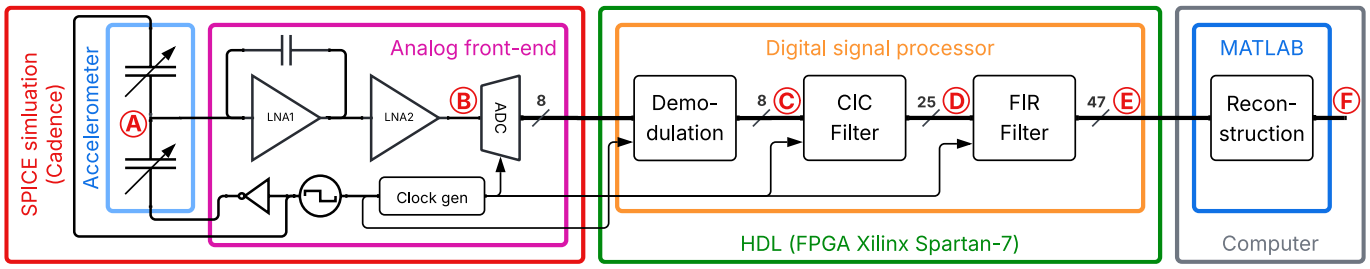

Fig. 1: Accelerometer, analog front-end, and DSP structure.

The main contributions of this letter are:

- The design and hardware validation of a fully-integer DSP on a cost-effective FPGA for nano-gravimetry, demonstrating a clear path towards low-power VLSI integration.
- The adoption of a 1 MHz square wave carrier as digital demodulation scheme, specifically tailored to overcome the 1/f noise limitations of modern nanometric CMOS technologies.
- A comprehensive validation of the digital system through a hardware-in-the-loop co-simulation, using a detailed analog front-end model designed in a 28-nm process and real-time processing on the target FPGA.
- The experimental demonstration of achieving the required 10 nm/s² sensitivity with robust rejection of out-of-band interferers, matching the performance of state-of-the-art systems with a CMOS-ready approach.

II. METHODS

The weak acceleration signal of interest falls within the sub-Hz frequency band, dominated by the flicker noise in the electronic domain. Double-sideband suppressed carrier amplitude modulation (DSB-SC AM) is chosen to mix the acceleration source with a carrier signal that shifts the signal power beyond frequencies where thermal noise dominates in CMOS technology. The accelerometer sensor structure prevents any phase and quadrature modulation, thus the carrier frequency and phase are explicitly transmitted alongside the modulated signal to the demodulation stage. The modulation is achieved via a square wave approach that streamlines the transmission to the digital demodulation stage, minimizing carrier frequency and phase errors, while retaining signal reconstruction accuracy.

Table 1. Sensor and circuit parameters.

Target signal	Amplitude range	10n to 3µ $m/s^2_{0\text{-peak}}$
	Max frequency	1 Hz
Out-of-band	Max amplitude	100 $\mu m/s^2$ 0-peak
	Max frequency	10 Hz
Carrier	Frequency	1 MHz
	Amplitude	1.2 $V_{0\text{-peak}}$
Sensor	Quality factor	10
	Mass	200 g
	Sensitivity	15
	Noise	0.88 $nm/s^2/\sqrt{Hz}$
	Modulation freq.	1 MHz
	Capacity	200 pF
Technology	CMOS	TSMC 28-nm HPC+
	Power supply	1.2 V
Amplification	Sensitivity	2.77 $kV/m/s^2$
	Gain	43.74 dB
	Bandwidth	77 kHz to 3.3 MHz
	Input referred noise	0.70 $nm/s^2/\sqrt{Hz}$
ADC	Sampling freq.	10 MHz
	Voltage range	0.8 V
	Resolution (LSB)	8 bits (3.1 mV)

A. Analog front-end model

The sensor and the analog front-end are modeled and simulated within the Cadence 2024 suite environment in TSMC's 28-nm HPC+ CMOS technology. The acceleration-varying sensor proof mass capacitance is biased using two opposing 1 MHz square wave carriers while the injected charge is read from a common node and processed by a low-noise amplifier (LNA1), converting differential charge variations into a voltage signal. Simulations account for sensor and bonding pad capacitance. A second low-noise amplifier (LNA2) further amplifies the signal to optimize utilization of the ADC's dynamic range. Key implementation parameters are summarized in Table 1. The ADC works at 10 MSamples/s to ensure a 5× oversampling ratio over the square carrier frequency. The DSP output must ensure 18 effective number of bits (ENOB) to avoid the reconstructed acceleration is affected by quantization noise; of these, 11 bits are provided by the oversampling ratio (10 M) over the target frequency band of 1 Hz, while the remaining 7 bits must be provided by the ADC. Also, exceeding 6 ENOB ensures LSB variation due to the analog in-band noise, useful to reconstruct the weakest acceleration signal. Digitization is here performed using an ideal 8-bit ADC.

B. Hardware design

The Cadence-simulated ADC outputs a signed 8-bit signal, along with a 1-bit logical equivalent carrier square wave, both saved to a text file. The ADC and carrier samples are interleaved and streamed via UART to a Xilinx Spartan-7 FPGA (mounted on a Digilent CMOD S7 35T evaluation board). UART is bottlenecking the sample rate, thus filters are activated only when a new sample is received, emulating continuous transmission. The signal is then demodulated by conditional inversion of the sample sign based on the 1-bit square carrier. The CIC filter receives the 8-bit demodulated signal and provides a full-precision 25-bit output every 100'000 samples (frequency response is in Fig. S1). The FIR filter implementation leverages a single DSP48E1 multiply and accumulate (MAC) block for an efficient, pipelined, fully serial architecture. The two DSP48E1 inputs of 25 and 18 bits are used respectively for the input samples and the FIR coefficients. The full-precision FIR output requires 47 bits, which conveniently fits within the 48-bit MAC output width.

The FIR filter, featuring 200 taps, is designed in MATLAB to approximate a Chebyshev response with 0.001 dB attenuation in the 1 Hz passband frequency range and 120 dB attenuation at the 5 Hz stopband. The coefficients are quantized to 18 bits for fixed-point arithmetic implementation. Fig. 2 presents the filter's frequency and phase response, highlighting the quantization effect compared to the full-precision design.

Table 2. CIC and FIR filter details.

CIC	Decimation	100’000
	Stages / Differential delay	1 / 1
	Input size	8 bits
	Output resolution	25 bits
FIR	Type (order)	Chebyshev (199)
	Passband (attenuation)	1 Hz (0.001 dB)
	Stopband (attenuation)	4 Hz (120 dB)
	Input size	25 bits
	Coeff. Quantization (fractional)	18 (21) bits
	Output resolution	47 bits

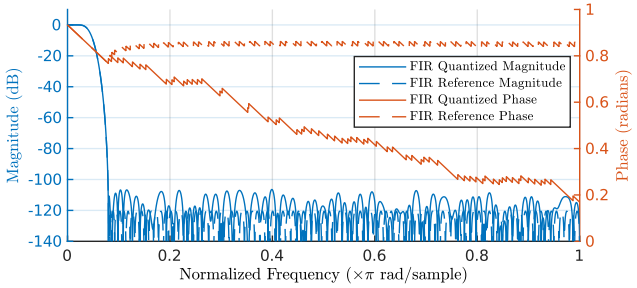

Fig. 3. FIR filter magnitude and phase response.

Both the CIC and the FIR filters operations are safely performed in integer domain arithmetic. Their characteristics are detailed in Table 2. The FPGA design, described in Verilog in Xilinx Vivado 2024.2, utilizes 1759 LUTs, 5355 flip-flops, and 1 DSP block. The dynamic power consumption is estimated to be 2 mW through a testbench feeding the DSP a sample each clock cycle. The overall complexity of the proposed DSP is O(N), where N is the tap length of the FIR filter of 200. The CIC filter contribution to the algorithm complexity is null, being O(1), but instead alleviates the FIR requisites by lowering the FIR throughput to only 100 Hz. Flowchart of the implemented algorithms are available in Fig. S2.

C. Simulation

The simulations cover edge cases, with the target signal amplitude set at the minimum (10 nm/s^2) and the maximum (3 µm/s^2) of its range, with and without the out-of-band (OOB) 5 Hz interferer of 100 µm/s^2. The target signal frequency is set at 1 Hz, where the oversampling frequency is the lowest. The FIR filter output is processed in MATLAB, where it is converted into acceleration by means of floating-point division operation. Any offset in the amplifiers operating point and any dampening introduced by the filter is estimated by a calibration measurement and corrected during floating-point reconstruction of the acceleration.

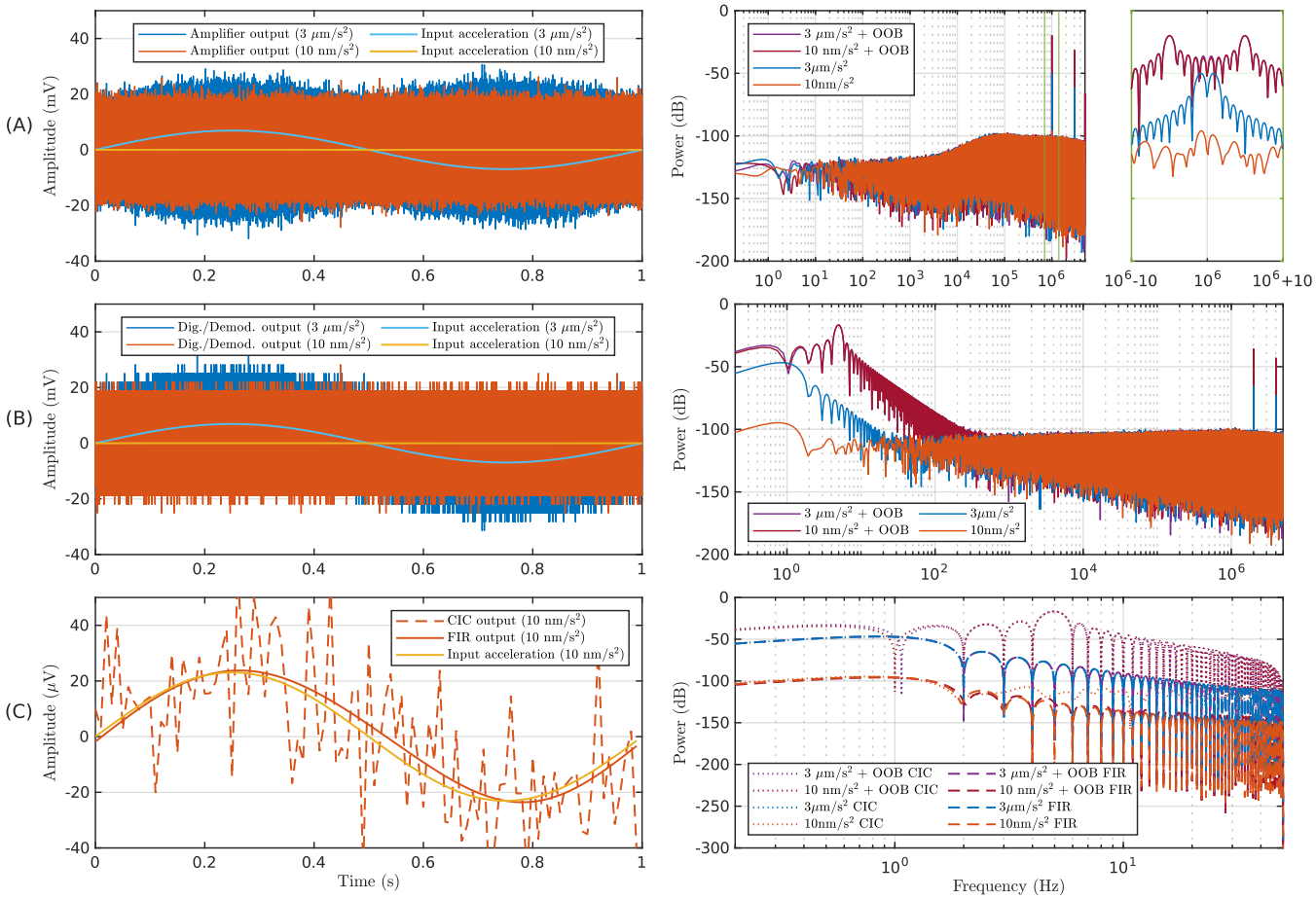

Fig. 2: Time (left) and frequency (right) domain analysis for (A) modulated and amplified (test-point B), (B) digitized and demodulated (test-point C), and (C) CIC (test-point D) and FIR (test-point E) output signals. Power spectrums include simulations with out-of-band (OOB) interferers. In (A), augmentation of the peaks at the carrier frequency are highlighted in the right green box.

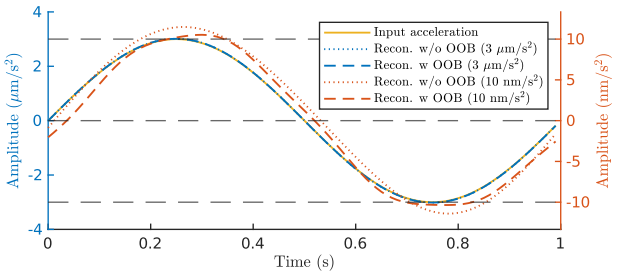

Fig. 4: Reconstructed acceleration (test-point F) of 10 nm/s² (red) and 3 μm/s² (blue) amplitude at 1 Hz with (dashed) and without (dotted) OOB interferent of 5 Hz compared to the ideal input acceleration (yellow, test-point A).

III. RESULTS

Spanning a few MHz of bandwidth, the noise at the ADC input completely overwhelms the minimum acceleration signal (10 nm/s²), while only faintly revealing the shape of the largest expected in-band signal (3 μm/s²), as in left side of Fig. 3A (test-point B in Fig. 1). Frequency analysis enables comparison between signals with such large amplitude gaps. As shown on the right side of Fig. 3A, the energy of the modulated signals peaks at the carrier frequency of 1 MHz and its harmonics. In the magnified section, the target tones at 1 Hz are visible, along with the 5 Hz out-of-band (OOB) interferer when present. The minimum acceleration signal remains just above the noise power level. Notably, the noise itself allows the ADC to quantize the minimum signal –smaller than the least significant bit (LSB)– into a few discrete bits.

The signal is then demodulated using the carrier (Fig. 3B, left; test-point C in Fig. 1), bringing the acceleration power back to its original frequency while leaving some energy at the harmonics (Fig. 3B, right). The demodulated acceleration is then passed through the CIC filter for decimation. Leveraging the oversampling ratio within the 50 Hz output band, the CIC filter significantly reduces noise while enhancing signal resolution, as shown in Fig. 3C (test-point D in Fig. 1). The FIR filter further refines the signal bandwidth to 1 Hz, effectively attenuating OOB noise and any OOB sources (Fig. 3C, test-point E in Fig. 1). Any non-linearity induced by the filter quantization remains out of the target band and is attenuated by more than 100 dB, not affecting the reconstruction.

Finally, as illustrated in Fig. 4 (test-point F in Fig. 1), the system reconstructs the minimum amplitude acceleration signal (10 nm/s²) with a typical SNR of 12.4 dB when OOB sources are not present and 12.2 dB when combined with the maximum expected OOB source (100 μm/s²). The largest relevant acceleration amplitude (3 μm/s²) is reconstructed with an SNR of 48.2 dB and 48.0 dB, respectively, with and without OOB sources. Table 3 shows the signal and noise evolution at the various test-points by evaluating both the calibration measurements (full-dynamic signal) and the no-signal condition, estimating the theoretical maximum SNR for the smaller signal (10 nm/s²). The signal is dampened (0.91×) mostly at the CIC filter output, which removes the high-frequency components remained from the demodulation, but also drastically reduces the noise thanks to the great oversampling ratio (100 k). Finally, the FIR filter further boosts the SNR, given the sharp focus on the 1 Hz bandwidth, allowing the precise reconstruction of the target weak acceleration signal.

Table 3. Noise analysis referred to 10 nm/s² acceleration

Test-point	Signal ampl.	Noise level	Theoretical SNR
A	10 $nm/s^2_{0\text{-peak}}$	0.88 $nm/s^2/\sqrt{Hz}$	15.97 dB @ 1Hz BW
B	27.77 $\mu V_{0\text{-peak}}$	4.67 mV_{rms}	-47.52 dB
C	25.36 $\mu V_{0\text{-peak}}$	4.75 mV_{rms}	-48.46 dB
D	24.89 $\mu V_{0\text{-peak}}$	17.4 μV_{rms}	0.10 dB
E	24.89 $\mu V_{0\text{-peak}}$	3.2 μV_{rms}	14.81 dB

Table 4. State-of-the-art comparison.

	This work	ISA [2,3]
Acceleration	DC to 1 Hz 10 nm/s² to 173 μm/s²	DC to 0.1 Hz 10 nm/s² to 30 μm/s²
Carrier	Square wave @ 1 MHz On chip	Sine wave @ 10 kHz Transformer
Technology	CMOS (SoC oriented)	JFET (discrete components)

IV. CONCLUSION

This work proves that a fully integrated CMOS-based acquisition system for nano-gravity accelerometers is feasible. The presented System-on-Chip-oriented approach unlocks the potential for multi-functional monolithic circuits, where a single chip could process data from accelerometers alongside other onboard instruments. This paves the way for next-generation scientific payloads with drastically reduced size, weight, and power consumption essential for smaller, cost-effective satellites. While the transition to a physical prototype requires careful consideration of the sensor's physical interconnects to maintain signal integrity, this work provides the foundational validation for this technological leap. A picture of the hardware-in-the-loop co-simulation system is shown in Fig. S3. Compared to the current state-of-the-art ISA (Table 4), the proposed solution achieves the same specifications while enabling full on-chip integration.

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