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Stacked-Cell Power Amplifier Design based on Technology Characterization and Modeling

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Abstract

The continuous evolution of wireless communication, radar, and sensing systems toward millimeter-wave (mm-wave) frequencies imposes increasingly stringent requirements on Radio Frequency (RF) power amplifiers in terms of output power, efficiency, linearity, and reliability. Gallium Arsenide (GaAs) pseudomorphic high-electron-mobility transistor (pHEMT) technologies continue to offer a compelling solution for these applications due to their superior high-frequency performance, linearity, and process maturity. Nevertheless, the relatively low breakdown voltage limits the achievable voltage swing and output power in conventional power amplifier architectures.

This thesis addresses these limitations through the investigation and development of GaAs-based stacked-cell power amplifier architectures. A comprehensive and experimentally validated design framework is proposed that spans device-level characterization, compact model extraction, architectural analysis, and millimeter-wave monolithic microwave integrated circuit (MMIC) design and implementation.

This research begins with an extensive experimental characterization of GaAs pHEMT devices, including DC and multi-bias on-wafer S-parameter measurements, large-signal low-frequency (LSLF) characterization, and accelerated stress testing under realistic operating conditions. These measurements are used to evaluate technology robustness, dispersion effects, and nonlinear behavior, as well as the extraction of accurate extrinsic and intrinsic device parameters. A systematic modeling procedure is established to derive reliable small-signal compact models appropriate for stability analysis and circuit-level design.

A key contribution of this work is the comprehensive analysis and modeling of common-gate device behavior in stacked-cell configurations, emphasizing its essential function in inter-stage impedance matching, voltage distribution, stability, and bandwidth at millimeter-wave frequencies. Utilizing the validated models, a complete technology-aware design flow is developed and implemented for a 27-GHz GaAs MMIC stacked-cell power amplifier,

encompassing stability network design, impedance matching, layout optimization, and electromagnetic co-simulation.

In summary, this thesis establishes a rigorous modeling and design methodology for GaAs stacked-cell power amplifiers at millimeter-wave frequencies. The proposed framework provides a strong foundation for building and testing high-performance GaAs MMIC power amplifiers and demonstrates that GaAs technology remains important for future millimeter-wave RF front-end applications.

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Chapter 1

Introduction

Nowadays, the continuous demand for higher data rates in both industrial and consumer mobile communication systems has driven the exploration of increasingly higher carrier frequencies. Parallel advances in semiconductor device technology have profoundly enhanced the design of power amplifiers (PAs). In particular, the adoption of high-performance compound semiconductor substrates such as Gallium Arsenide (GaAs) and Gallium Nitride (GaN) has enabled the development of active devices with superior power density, breakdown voltage, and high-frequency performance. These advancements make such technologies especially suitable for meeting the stringent requirements of modern microwave and millimeter-wave (mm-wave) power amplifiers.

Radio frequency (RF) communication systems fundamentally rely on transceiver architectures, as shown in Figure 1. 1, in which both the transmitting and receiving sections incorporate amplification stages to preserve signal integrity. In the transmit path, the signal undergoes attenuation as it propagates through air and other media; hence, a PA is employed to boost its strength prior to radiation. Conversely, in the receiver chain, a low-noise amplifier (LNA) is required to amplify the weak incoming signal while minimizing the overall noise contribution.

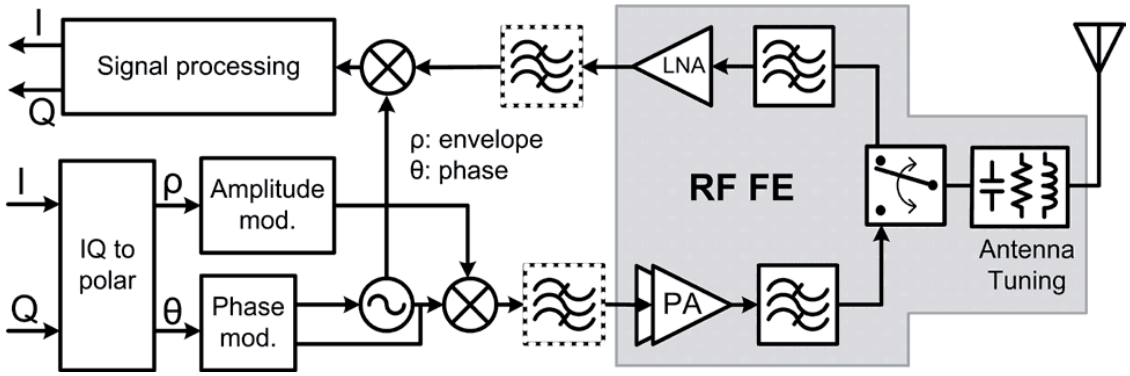

Figure 1. 1: RF transceiver architecture

1.1 Motivation for mm-Wave Power Amplifier Design

The rapid evolution of wireless communication and sensing technologies has accelerated the transition toward the mm-wave frequency spectrum. This shift is primarily motivated by the growing demand for wider bandwidth, higher data throughput, and improved energy efficiency required by emerging communication and radar applications.

Operating in the mm-wave range provides access to substantially larger bandwidths compared to conventional microwave bands, enabling the transmission of massive volumes of data. Such capability is essential for next-generation wireless standards, including 5G and 6G, which target carrier frequencies extending into the mm-wave and even terahertz domains. These systems aim to deliver ultra-high data rates, low latency, and enhanced spectral efficiency, key enablers for innovative applications such as augmented and virtual reality (AR/VR), telemedicine, industrial automation, and the Internet of Things (IoT).

In parallel, the rapid expansion of mm-wave radar technologies in automotive, imaging, and security sectors has intensified the need for high-efficiency and highly linear PAs capable of providing sufficient output power at high frequencies. As a critical element in the transmitter chain, the PA directly impacts system-level metrics such as output power, efficiency, and linearity, thereby determining the overall performance and reliability of the RF front-end. Achieving this vision relies heavily on developing compact, efficient, and robust mm-wave PAs capable of stable operation under harsh environmental conditions.

Given their crucial role, microwave and mm-wave PAs represent a cornerstone of modern wireless communication infrastructures. In practical systems such as radio base stations the PA

typically accounts for a significant portion of the total power consumption, making efficiency optimization one of the most critical objectives in amplifier design.

1.2 GaAs Technology

Achieving high performance in the analog front end at millimeter-wave (mm-wave) frequencies, particularly in terms of medium-to-high output power, high efficiency, and a high level of integration, remains a major design challenge. Within mm-wave transceivers, the power amplifier (PA) plays a pivotal role, as it largely determines the achievable output power, power-added efficiency (PAE), and linearity of the overall system. At these frequencies, simultaneously realizing high output power and efficiency over a wide bandwidth is inherently difficult due to fundamental trade-offs among gain, bandwidth, stability, and device parasitics. Consequently, substantial research efforts have been devoted in recent years to mm-wave PA development, driven in particular by the stringent requirements of emerging 5G wireless communication systems.

A wide range of semiconductor technologies has been explored for medium-power monolithic microwave integrated circuit (MMIC) PAs in the Ka-band, including complementary metal–oxide–semiconductor (CMOS), Gallium Arsenide (GaAs), and Gallium Nitride (GaN). CMOS-based PAs offer clear advantages in terms of cost reduction, very high integration density, and high transition frequencies (f_T), making them attractive for highly integrated transceiver architectures. However, their limited breakdown voltage and low power density constrain the achievable output power and efficiency at mm-wave frequencies.

In contrast, III–V semiconductor technologies provide superior power handling capability and lower noise figures, enabling higher output power levels. Among them, GaAs offers a favorable compromise between performance, cost, and process maturity. Although both GaAs and GaN enable high-performance RF and mm-wave circuits, their distinct material properties lead to different performance trade-offs and application domains, which are discussed in detail in Chapter 2. Despite their advantages, III–V-based PA implementations often suffer from reduced PAE and relatively large chip area, which remain key challenges [1].

In particular, GaAs pHEMT technologies with gate lengths down to 100 nm have demonstrated strong potential for high-performance mm-wave front-end circuits [2]. Owing to their mature

fabrication processes, favorable cost-to-performance ratio, and excellent high-frequency characteristics, GaAs pHEMTs remain a preferred choice for Ka-band power amplifier design [3], [4]. However, the relatively low breakdown voltage of GaAs devices limits the allowable voltage swing, requiring conventional GaAs PAs to operate at low supply voltages (typically below 10 V). This constraint restricts the achievable output power and results in a low optimum load impedance. Moreover, the associated high impedance transformation ratio (ITR) complicates the design of wideband matching networks, leading to large circuit dimensions and increased RF losses, which further degrade output power and efficiency.

To address these limitations, the stacked cell topology has emerged as a promising alternative to conventional current-combining approaches. By connecting multiple transistors in series, stacked architectures enable a larger effective voltage swing at the output, thereby mitigating the breakdown voltage limitation and allowing higher output power to be achieved in GaAs-based mm-wave Pas [4].

1.3 Stacked Cell Architecture

Device stacking is of particular interest because it overcomes the primary limitation of parallel current-combining architectures, namely the reduction of the optimum load impedance as the number of transistors increases. This reduction leads to a high impedance transformation ratio when matching to an external load, which severely limits the achievable bandwidth. In contrast, stacked-cell topologies enable higher-voltage operation by connecting multiple series transistors, thereby increasing the overall voltage handling capability without a proportional increase in current. As a result, higher output power can be achieved while maintaining a compact layout and reduced losses in the output matching network. In addition, stacked architectures inherently exhibit a higher output impedance, which relaxes the quality-factor requirements of the load network and further supports broadband operation. These advantages can also translate into a gain enhancement, typically on the order of 3 dB or more. As reported in the literature, stacked power cells represent an effective solution for extending the output power capability of GaAs technologies even beyond the W-band, where low-breakdown devices are commonly used. Despite their potential, the widespread adoption of stacked-cell PAs is currently limited by the lack of comprehensive design methodologies and accurate nonlinear device and cell models,

particularly those accounting for the electromagnetic effects of complex passive structures and the behavior of common-gate transistors. Moreover, stacked architectures introduce additional design challenges related to biasing, stability, and voltage distribution among devices. Consequently, a rigorous theoretical analysis of the stacked-cell structure is essential to fully understand its operating principles and performance trade-offs, especially at mm-wave frequencies where the balance between output power, gain, and voltage handling becomes increasingly critical [5]. The operating principles and design considerations of stacked-cell architectures are therefore examined in detail in Chapter 3.

1.4 Thesis Motivation

In this research, the problem is addressed from an architectural perspective by developing a device model that overcomes the limitations of existing devices, relying on GaAs technology, which has the advantage of maturity, linearity, reliability, and Space qualification. The goal of this project is to push even further the exploitation of GaAs technology by merging its high-frequency performance with the Stacked Cell, which can become a key enabling solution as higher-voltage/higher-power macro-devices, suitable for replacing single transistors in PA design for the intended applications.

1.5 Thesis Organization

The overarching objective of this thesis is to establish a complete GaAs-based modeling to design and validation framework that bridges device-level characterization, compact model development, and the realization of mm-wave power amplifiers. The work aims to provide a unified and experimentally validated methodology for GaAs pHEMT-based stacked-cell architectures.

The research activities are structured into three main phases:
The first phase encompasses the experimental characterization, model extraction, and technology validation, with the objective of quantitatively assessing their performance and verifying their applicability within a realistic technological framework.

1. Perform comprehensive small-signal and large-signal low-frequency (LSLF) characterization of GaAs pHEMT devices up to mm-wave frequencies, enabling an accurate understanding of their linear and nonlinear behavior under realistic operating conditions.

2. Extract the extrinsic parasitic network and develop a reliable intrinsic compact model, so that the device representation is accurate and robust for circuit-level simulations, stability analysis, and reliable large-signal performance prediction.

3. Investigate and formalize a novel modeling insight for the common-gate device in stacked-cell topologies, aiming to enhance the accuracy of model-based predictions of gain, stability, inter-stage voltage distribution, and mm-wave bandwidth.

The second phase is design, optimize, and simulate a 27-GHz MMIC stacked-cell power amplifier using the developed modeling framework.

The design flow begins with a theoretical analysis that derives the stacked-cell architecture, stability conditions, matching targets, and expected large-signal behavior, supported by numerical simulations. This is followed by a technology-aware phase in which device models are validated, layout-dependent parasitics are accounted for, and the physical layout is implemented. The final stage includes EM co-simulation of the layout, design rule verification, and preparation for tape-out.

Finally, the third phase focuses on implementing a complete fabrication and measurement flow to experimentally validate both the device model and the power amplifier. This phase establishes a clear connection between device-level parameter extraction, model-based design choices, and the measured PA performance. The proposed structures are designed and fabricated using a GaAs MMIC technology.

In Chapter 2, the fundamental concepts of power amplifiers are introduced, including their operating principles, main figures of merit, and the theoretical background of the stacked-cell architecture, outlining its advantages and design challenges.

Chapter 3 is dedicated to the analysis of a real device, focusing on GaAs pHEMT transistors. It introduces the device structure and the main physical mechanisms governing high-frequency behavior, followed by the measurement setup and calibration procedures (TRL, LRRM, SOLT) for on-wafer characterization up to 110 GHz. Large-Signal Low-Frequency (LSLF) and small-signal measurements are presented to evaluate the technology, along with extrinsic parasitic extraction and nonlinear and linear model development.

In Chapter 4, the design flow of the stacked-cell amplifier is presented, including stability analysis, matching optimization, and large-signal behavior. The validated models are incorporated into a technology-aware design, accounting for layout-dependent parasitics, EM co-simulation, and tape-out preparation.

Finally, Chapter 5 conclusion and future overview will be given.

Chapter 2

Power Amplifier Basics and Technology Selection

2.1 Introduction

This chapter provides the fundamental knowledge and aspects of RF power amplifier design. Several performance metrics, such as output power, drain efficiency, and power-added efficiency, are introduced, followed by a description of PA classes and how they operate. The PA classes covered linear amplifiers, such as class A, AB, B, and C, and switched-mode classes.

2.2 Definition of Power Amplifier

Wireless communication systems rely on modulated signals that must be transmitted over long distances through free space. These signals are radiated by antennas, and the achievable transmission range is strongly dependent on the power level delivered to the antenna terminals. In many applications, the antenna may require input power levels of several hundred watts. To meet this requirement, RF PAs are employed to increase the signal power at the transmitter output

so that it can be efficiently radiated, while avoiding excessive signal degradation caused by added noise or linear and nonlinear (harmonic or intermodulation) distortions.

PA is a quasi-linear system used to amplify the power coming from other transmitter parts, transforming the DC power coming from a DC source into an AC signal at the output, as shown in Figure 2. 1[6]. Ideally, the output signal should remain a faithful replica of the input waveform. For this to happen, the amplifier should amplify the signal by the same amount over the bandwidth and input dynamic range (DR), keep the signal timing unchanged, and avoid creating distortion or unwanted extra signals, ensuring a linear phase relationship between the input and output signals, and minimizing nonlinear distortion products[7].

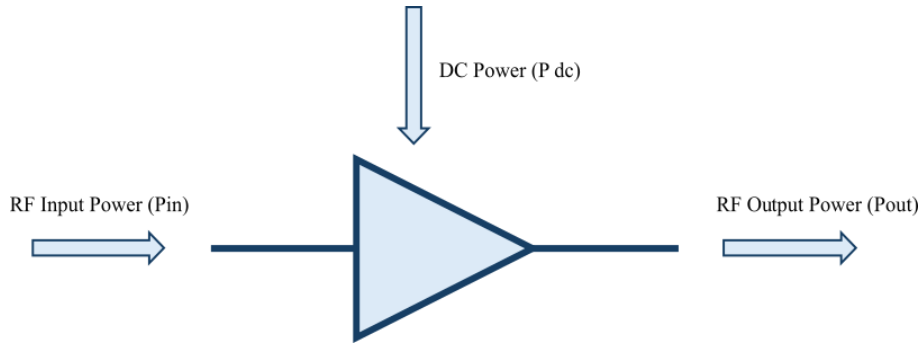

Figure 2. 1: Schematic representation of a PA operation[6]

Achieving high saturated output power, high average efficiency under power back-off conditions, compact layout, and wide bandwidth, therefore, requires a carefully optimized balance among device sizing, biasing, matching networks, and architecture selection. This challenge is further exacerbated by non-ideal device behaviour at mm-Wave frequencies. For instance, in silicon CMOS technologies, low supply voltage, reduced breakdown margins, lossy substrates, and thin gate oxides limit both achievable output power and efficiency at 60 GHz and beyond, restricting their suitability to short-range applications. In addition, mm-Wave passive components such as transmission lines, impedance matching networks, and supply-ground routing exhibit significant parasitic effects, which degrade matching quality, reduce available gain, and lower PAE.

Moreover, as devices are driven closer to saturation to maximize output power or power density, nonlinear distortion mechanisms, including AM/PM conversion, intermodulation products, and

memory effects, become increasingly dominant. These nonlinearities make it difficult to simultaneously maintain high linearity and high efficiency, further highlighting the inherent complexity of mm-Wave PA design.

The evaluation and comparison of RF power amplifiers rely on a common set of performance metrics, even though the required specifications vary widely across communication standards and system applications. At millimetre-wave (mm-Wave) frequencies, the design of MMIC power amplifiers becomes particularly demanding, as it requires achieving these metrics under stringent conditions that significantly increase design complexity. Typical figures of merit include stability, power gain, efficiency, power-added efficiency (PAE), output power, linearity, and bandwidth. Since the PA is generally the most power-consuming block within the RF front-end, its design strongly influences overall system efficiency, signal quality, and power budget. The following section provides a detailed discussion of each metric.

2.2.1 Stability

Stability analysis is a fundamental aspect in the design of active RF circuits and is particularly critical in power amplifier implementation. Oscillations are highly undesirable, as they can generate complex and uncontrolled waveforms with unpredictable amplitude and spectral content, resulting in significant deviation from the intended behavior of the amplifier. Depending on their nature, spurious oscillations may introduce several detrimental effects, including interference with the desired signal, unintended modulation, increased noise levels, and, in severe cases, device over-stress and potential damage to active components. Furthermore, once oscillations occur, the small-signal linear model is no longer valid and, consequently, scattering parameters lose their applicability, causing the circuit to deviate from its expected operational characteristics.

Unstability may originate from various mechanisms, including internal or external feedback paths, improper transistor loading, low-frequency oscillations, off-chip biasing networks, odd-mode oscillations, and sub-harmonic oscillation modes. In particular, feedback-induced unstability can occur when the magnitude of the feedback signal becomes sufficiently large due to coupling between the input and output nodes through the gate-to-drain capacitance C_{gd}.

Oscillation conditions are satisfied when a negative resistance is observed at either the input or output port of the device, ultimately rendering the amplifier unstable. Moreover, low-frequency oscillations may arise from thermal feedback mechanisms associated with internal negative-resistance effects or from insufficient DC-supply decoupling[8].

A power amplifier is considered stable if it preserves its intended performance independent of variations in source and load impedances. Stability can be classified into two main forms: unconditional and conditional stability. A transistor is regarded as unconditionally stable if it remains stable across all frequencies for any passive source and load impedance combination connected to its input and output ports. This condition, however, is not always fulfilled in practical devices, many of which exhibit conditional stability. Consequently, stability assessment is imperative prior to the deployment of a transistor in a power amplifier, as source or load impedances may vary in operation due to changes in temperature, supply voltage, or antenna mismatch conditions [9]. Equally important is how the power amplifier is terminated at frequencies outside its operating band.

$$\text{Stability Factor} \qquad \mathrm{k} = \frac{1 - |\mathrm{S}_{11}|^2 - |\mathrm{S}_{22}|^2 + |\Delta|^2}{2|\mathrm{S}_{12}\mathrm{S}_{21}|} \tag{2 . 1}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2 . 2}$$

Stability evaluation can be performed either graphically, using stability circles, or analytically, using well-established stability criteria. In this thesis, analytical stability verification is carried out based on the k-Δ Factors employing S-parameters for quantitative assessment.

An amplifier is considered unconditionally stable if $K > 1$ and $| \Delta | < 1$. The only limitation of the K-factor is that it cannot be used to compare the degree of stability between different devices, which essentially stems from the fact that the criterion is defined based on two independent parameters. If a transistor is not unconditionally stable, stabilization networks such as series or parallel resistors at the input or output can be employed. It is worth noting that circuits with a large K-factor typically exhibit low gain, due to the relationship $K \propto 1/S_{21}$. Therefore, it is preferable to design the circuit such that K remains close to unity.

2.2.2 Power Gain

A power amplifier should increase the power of the signal from the input to the output port, so it should introduce a gain larger than 1. Actually, three types are defined, depending on whether the amplifier is input-matched or not. Power gain $(G_P)[10]$ is defined as the ratio of output power to input power, as expressed in Equation (2. 3), where P_{IN} is the power transferred from the input power generator to the device input. This parameter expresses the capability of the power amplifier to deliver a significantly higher power level to the load compared to the input power.

$$G_p = \frac{P_{out}}{P_{IN}} \qquad (2.\ 3)$$

A power amplifier aims to enhance overall efficiency and sensitivity by increasing output power. In practical amplifier design, the most used gain definition is the transducer power gain, (G_T). obtained from Equation (2. 4)[10] where P_{AVS} is the power available (generated) by the input power generator. G_T accurately accounts for mismatch effects at both the input and output terminals.

$$G_T = \frac{P_{out}}{P_{AVS}} \qquad (2.\ 4)$$

Another definition of gain is the available gain (G_A)which is used to estimate the maximum achievable performance under the assumption of a perfect conjugate-matched condition at the power amplifier output. It is defined as the ratio of the available output power to the available input power, as expressed in Equation (2. 5)[10]. This definition assumes conjugate matching at both source and load and is therefore dependent on the source impedance but independent of the load impedance.

$$G_A = \frac{P_{AVO}}{P_{AVS}} = G_T(1 + \frac{P_{REFO}}{P_{out}}) \qquad (2.\ 5)$$

Power gain = G = $\frac{P_{out}}{P_{IN}}$ is the ratio of power dissipated in the load Z_L to the power delivered to the input of the two-port network. This gain is independent of Z_s, although the characteristics

of some active devices may be dependent on Z_S Available power gain (G A = $\frac{P_{AVO}}{P_{AVS}}$) is the ratio of the power available from the two-port network to the power available from the source. This assumes conjugate matching of both the source and the load and depends on Z_S, but not Z_L Transducer power gain (GT = $\frac{\mathrm{P_{out}}}{\mathrm{P_{AVS}}}$) is the ratio of the power delivered to the load to the power available from the source it depends on both Z_S, and Z_L.

2.2.3 Output Power

In RF applications, power levels are typically expressed in dBm. In the general case, assuming a complex load $Z_{\mathrm{Load}} = R + jX$, the output power is given by Equation (2.6). When the load at the output is purely resistive, R_L, the expression simplifies to Equation (2.7). In this formulation, V_{out} denotes the output voltage, while R_L represents the load resistance. As illustrated in Figure 2. 2 the term "peak-to-peak" refers to the total voltage swing observed at the output node.

In practice, increasing the effective active device periphery (by enlarging the transistor width or increasing the number of parallel cells) enhances the maximum achievable output power capability.

$$P_{out} = \frac{1}{2} real\,(V_{out} \cdot conj(ID)) \qquad (2.\ 6)$$

$$P_{out} = \frac{V_{out}^2}{2R_L} = \frac{(\frac{V_{peak-to-peak}}{2})^2}{2R_L} \qquad (2.\ 7)$$

$$P_{out} = \frac{1}{2} V_m I_m = \frac{1}{2} V_{DC} I_m \qquad (2.\ 8)$$

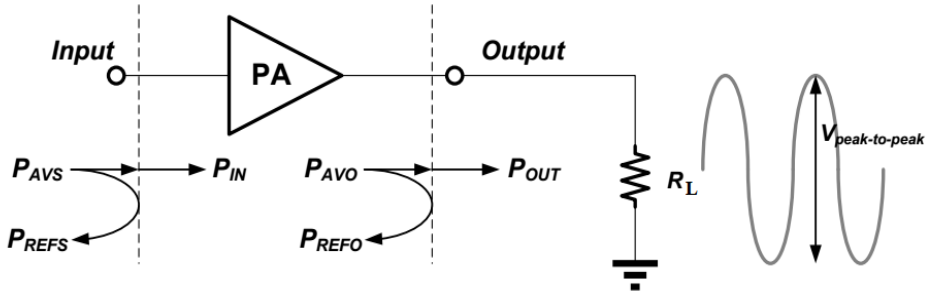

Figure 2. 2: Output Power definition

Saturated output power is the maximum power level that the device can deliver to the load under steady-state operating conditions. This limit is fundamentally constrained by the intrinsic electrical and physical properties of the device.

2.2.4 Efficiency

The efficiency of a power amplifier can be classified into two categories: Drain Efficiency and power-added efficiency (PAE).

Drain efficiency is defined as the ratio of the RF output power to the DC power consumption, as expressed in Equation (2. 9). This definition does not take into account the power delivered to the amplifier input. The most widely used and accurate efficiency metric, known as power-added efficiency (PAE), is presented in Equation (2. 10)[10].

PAE is defined as the ratio of the difference between the output and input RF powers to the DC power consumption. In these expressions, P_{out} represents the output RF signal power, P_{in} denotes the input RF signal power, and P_{DC} corresponds to the DC supply power consumption as shown in Equation (2. 11).

$$DE = \frac{P_{out}}{P_{(P_{DC/supp})}} \tag{2. 9}$$

$$PAE = \frac{(P_{out} - P_{in})}{P_{(P_{DC/supp})}} \tag{2. 10}$$

$$P_{DC} = V_{DC} I_{DC} = \frac{V_{DC}^2}{R_L} = = \frac{2}{\pi} I_m V_{DC} \tag{2. 11}$$

2.2.5 Linearity

Linearity is one of the most critical design parameters in RF wireless power amplifiers, and the required level is strongly dependent on the employed modulation scheme. Variable-envelope modulation formats require highly linear power amplification to avoid information loss and envelope distortion, whereas constant-envelope schemes allow operation closer to the compression region, improving efficiency.

Fundamentally, a power amplifier behaves as a nonlinear circuit block due to its large-signal operating regime, and the severity of nonlinear effects increases with output power. The sources of nonlinearity can be categorized into weak and strong mechanisms. Weak nonlinearities originate from the intrinsic nonlinear I–V characteristics of the active device, resulting in amplitude/phase distortion and intermodulation products generated by the interaction of multiple frequency components. These effects dominate when the amplifier operates below the 1-dB compression point. In contrast, strong nonlinearities emerge when the device approaches physical limitations, such as gain compression due to saturation or voltage swing constraints imposed by the supply. Insufficient linearity leads to adjacent-channel interference, where unwanted spectral components spill into neighbouring frequency bands, degrading system performance and violating spectral emission regulations. Linearity is typically quantified using performance metrics such as adjacent-channel power ratio (ACPR), third-order intermodulation distortion (IMD3), 1-dB compression point (P1dB), third-order input intercept point (IIP3), error vector magnitude (EVM), and AM-AM/AM-PM distortion.

At a certain input signal level, where the output voltage or current waveform reaches its maximum allowable swing, gain compression occurs, and the amplifier gain begins to decrease. As illustrated in Figure 2. 3, the 1-dB compression point of a power amplifier is defined as the point at which the actual gain drops by 1 dB from its ideal small-signal (linear) gain. Once the corresponding 1-dB compression input power level is identified, the amplifier can be considered to operate either in its linear or nonlinear region. Therefore, the 1-dB compression point is widely used as a straightforward indicator to characterize the linearity behavior of a power amplifier.

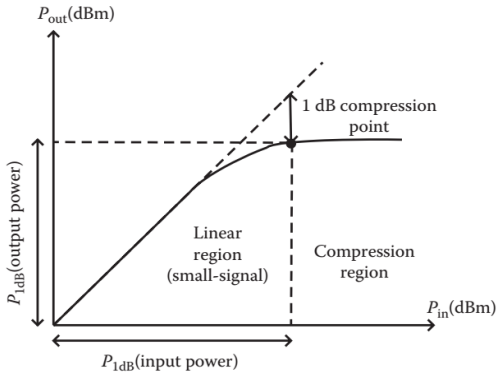

Figure 2. 3: 1dB compression Point for Power Amplifier [5]

The gain corresponding to the 1-dB compression point can be determined using the following equation, where G_0 represents the small-signal (linear) gain of the amplifier at the fundamental frequency:

$$P_{1dB,out} - P_{1dB,in} = G_{1dB} = G_0 - 1 \quad (2.12)$$

2.3 Power Amplifier Classes of Operation

Power amplifiers can be categorized into two main classes according to the biasing conditions applied to the transistor: linear and nonlinear (switching). In linear operation, the device is biased in the saturation region and behaves as a voltage-dependent current source, forming a transconductance-based power amplifier. In contrast, when the transistor is biased near cut-off or in the triode/linear region, it acts primarily as a switch, leading to switching (nonlinear) power amplifiers [9].

In linear classes of operation, the active device operates as a voltage-dependent current source. The transistor behaves as a controlled current source whose conduction angle (θ), defined as the portion of the RF period during which the device conducts current, determines the amplifier's class of operation. Depending on the bias conditions, the conduction angle can vary from a small fraction of the cycle up to a full 2π.

The equivalent circuit representation of a power amplifier operating in linear mode is shown in Figure 2. 4. When biased for linear operation, the amplifier can handle signals with non-constant envelopes, such as amplitude-modulated waveforms. All linear classes share a common circuit topology and therefore can be implemented using the schematic shown in Figure 2.4; the only distinguishing factor among these classes is the choice of bias point. Under sinusoidal or near-sinusoidal excitation, the transistor functions as a current source for a specific portion of the RF cycle, and this portion defines the class of operation [9].

Although the tuned parallel LC filter shown in Figure 2.4 is not strictly required for the basic amplifier topology, its incorporation substantially enhances overall performance. The filter is designed to provide a high impedance only at the fundamental frequency while presenting a short-circuit impedance to harmonic components generated by the nonlinearities of the device. This selective impedance shaping ensures that the active device effectively "sees" the load only at the fundamental tone. By suppressing harmonic currents and preventing them from dissipating power in the load or in the device itself, the filter improves efficiency and helps maintain the desired sinusoidal voltage waveform at the output. In practical RF amplifier design, such a resonant load network is almost always included because it contributes to cleaner spectral behaviour and reduces unnecessary stress on the transistor

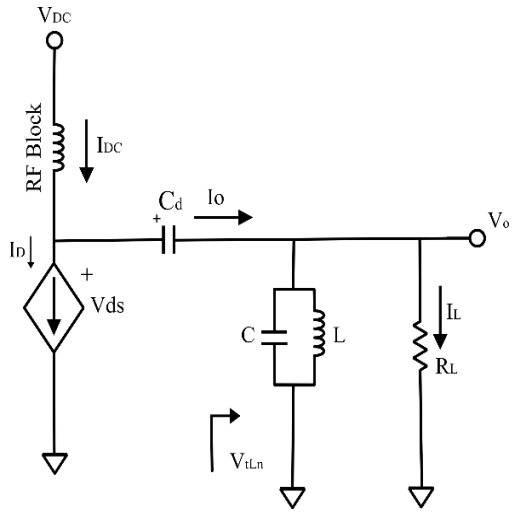

Figure 2. 4: Equivalent circuit representation of a power amplifier operating in linear mode

The conduction angle directly sets the balance between linearity and efficiency. Larger conduction angles, such as those in Class A operation, deliver high linearity but inherently lower efficiency. As the conduction angle is reduced progressing toward Class C, the efficiency increases at the cost of linearity, which is reflected in the decreasing average device current shown in Figure 2.5. Thus, by establishing the bias point, the designer defines both the conduction angle and the resulting amplifier class.

Ultimately, the class of operation can be determined by observing the drain current waveform. The fraction of the RF cycle during which current flows provide a direct and practical indication of the amplifier's conduction angle and therefore its class.

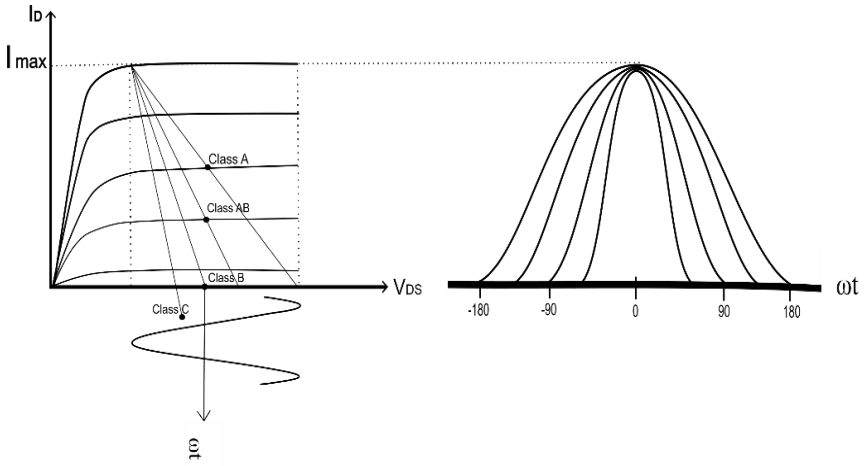

Figure 2. 5: Bias points and Load lines for Linear PA

Achieving higher efficiency requires biasing the transistor such that it remains ON for a shorter portion of the RF cycle. Theoretically, classes such as Class B and Class C deliver the same maximum output power as Class A, since the maximum voltage and current swing remain the same. Moreover, as the gate bias voltage decreases, the slope of the load line becomes steeper (as shown in Figure 2. 5), indicating a smaller load resistance. Therefore, as the device bias approaches the cutoff typical of Classes AB, B, and C, the load resistance must decrease to maintain maximum output power.

2.3.1 Class A Operation

In Class A amplifiers, the transistor is biased so that the gate–source voltage is greater than the device threshold voltage, causing the device to conduct during the entire RF cycle.

The minimum total input voltage (including both the input signal and the input voltage DC bias) is always larger than the device threshold voltage

Hence, Class A has a 360° conduction angle, offering the highest linearity but also the lowest efficiency because the device continuously dissipates power. The load line and drain voltage/current waveforms are shown in Figure 2. 5.

The maximum theoretical efficiency occurs when the drain voltage swings between 0 and $V_{DD.}$

Using (2.7), (2.8), and (2.11), the maximum theoretical efficiency of a Class A amplifier is 50%. Therefore, Class A amplifiers are employed in low-power applications that demand high linearity, where linear performance is prioritized over efficiency. They provide the highest linearity and can also deliver the maximum achievable gain among all amplifier classes.

2.2.2 Class B Operation

In Class B amplifiers, V_{GS} is biased approximately at the device threshold, and the transistor conducts for half of the RF cycle, yielding a 180° conduction angle, which means that when there is no input, the device is OFF and does not waste power like in class A.

Under ideal conditions, maximum efficiency occurs when the amplitude of the fundamental component of the drain voltage attains its maximum permissible value, such that the instantaneous drain voltage swings from 0 to $2V_{DD}$ without clipping. This condition enables maximum fundamental output power while maintaining the required half-sinusoidal drain current waveform.

By using (2. 7), (2. 12), and (2. 13), the ideal Class B efficiency becomes:

$$\eta_{max} = \frac{\pi}{4} = 78.5\%$$

Class B offers much higher efficiency than Class A, but at the expense of linearity and the penalty of 6 dB. To improve linearity while maintaining a reasonable efficiency level, a push–pull Class B configuration may be used.

2.2.3 Class AB Operation

Class AB amplifiers offer a compromise between Classes A and B. The gate–source bias is set slightly above the device threshold voltage, higher than in Class B but lower than in Class A, resulting in a conduction angle between 180° and 360°. Under ideal conditions, the theoretical efficiency ranges from 50% up to 78.5%, depending on the selected bias point. As a result, the achievable linearity, gain, and efficiency fall between those of Class A and Class B, making Class AB a practical trade-off for applications requiring both moderate linearity and improved efficiency.

2.2.4 Class C Operation

Class C amplifiers are biased below the threshold voltage, keeping the device OFF except when driven by the input signal. This results in a conduction angle less than 180°, producing a theoretical efficiency from 78.5% up to 100%. However, due to their severe nonlinearity, Class C amplifiers are unsuitable for linear modulation formats and are primarily used in high-efficiency narrowband systems [11].

Class	Mode	Conduction Angle (θ)	Efficiency (%)	Linearity
A	linear	2π	50	Good
AB		$\pi < \theta < 2\pi$	78.5	Moderate
B		π	78.5	Moderate
C		$< \pi$	~ 100	poor

Table 2. 1: Classification of power amplifiers by operation class

Table 2.1 summarizes the main categories of power amplifiers, based on their operating principles and biasing conditions.

2.4. Key Compound Semiconductor Technologies:

2.4.1. Gallium Nitride (GaN)

Gallium Nitride (GaN) has become an important semiconductor technology, especially for high-power applications such as base-station power amplifiers operating in the millimeter-wave range. Because gallium-based materials can support high output power, GaN offers the highest power-handling capability among them [12]. Its wide bandgap and ability to operate at high current levels make it widely used in satellite communication systems, electronic warfare, and modern wireless networks. Current research continues to explore GaN transistor technology to develop MMIC-based RF power amplifiers (PAs) with improved efficiency, sometimes using techniques such as envelope tracking (ET)[13].

Key Performance Merits of GaN Technology

GaN MMIC technology has developed quickly, moving from early research to commercial use in base stations, radar systems, and satellite communications. Modern GaN processes now provide better manufacturing yield, more accurate large-signal models, and more standardized process design kits (PDKs). Although GaN does not have the long history or widespread use of GaAs, it is now considered a mainstream technology for high-power RF applications. A strong ecosystem of foundries, design tools, and modeling techniques supports its use in both industrial and defence applications.

1. Electron Mobility and Saturation Velocity

Gallium Nitride (GaN) exhibits a unique combination of moderate electron mobility (≈1500–2000 $cm^2/V \cdot s$) [14] and remarkably high saturation velocity, exceeding 1.5×10^7 cm/s, which surpasses silicon and remains comparable to the effective velocity achieved in GaAs under strong electric fields[12]. In AlGaN/GaN HEMTs, these transport properties are further enhanced by the formation of a high-density two-dimensional electron gas (2DEG) induced by spontaneous and piezoelectric polarization at the heterojunction interface. This inherently large carrier density allows GaN devices to sustain fast electron transport while delivering substantial current levels, enabling efficient operation at microwave and millimeter-wave frequencies. As

a result, GaN-based transistors achieve short transit times, reduced delay, and robust gain even under high electric field stress, characteristics that are particularly advantageous for high-power and wideband mm-wave PAs, as used in radar, satellite communication, and emerging 6G systems.

2. Cut-off Frequency (f_t) and Maximum Oscillation Frequency (f_{max})

Advances in epitaxial growth, gate engineering, and scaling have enabled GaN HEMTs to achieve f_t and f_{max} values well into the 100–300 GHz range, depending on technology node and substrate (e.g., GaN-on-SiC or GaN-on-Si) [15]This combination of high current density and competitive f_t/f_{max} allows GaN devices to provide significant gain at mm-wave frequencies, enabling high-power amplification in the GigaHertz range. Consequently, GaN MMICs are increasingly used in front-end transmitters for 5G/6G base stations, E-band links, and wideband radar, where both high gain and output power are required [16], [17].

3. Breakdown Voltage

Compared with GaAs, CMOS, or SiGe, GaN transistors exhibit much higher breakdown voltages, typically ranging from 50 V up to 100–200 V, depending on device geometry[18] and substrate [19] and breakdown electric field is 3 MV/cm [20]. This capability allows GaN PAs to operate at high drain voltages while maintaining safe operating margins, enabling large voltage swings and very high RF output power. As a result, GaN-based PAs can achieve excellent power-added efficiency (PAE) even under demanding large-signal conditions, which is critical in high-power radar, electronic warfare, and long-range microwave links. The high breakdown strength also improves device robustness under mismatch and pulsed operation.

4. Parasitic Capacitance and Isolation (Especially on SiC Substrates)

When grown on semi-insulating substrates such as SiC [21] or engineered high-resistivity substrates [22], GaN HEMTs can exhibit relatively low output capacitance and good isolation between neighbouring devices. This helps reduce signal leakage and parasitic coupling in dense RF layouts. In addition, the relatively high resistivity and favorable dielectric properties of GaN-on-SiC platforms facilitate the integration of compact transmission lines and matching networks

with reduced substrate loss, enabling efficient and broadband impedance transformations in high-power MMICs[23].

5. Linearity and Noise (High Efficiency, Good Linearity Trade-Off, and Robust Large-Signal Behavior)

GaN devices combine high voltage and current handling with strong transconductance, enabling very high drain efficiency in power amplifiers, particularly in saturated and Doherty-type architectures [24], [25], [26]. Although intrinsic linearity is not as smooth as in GaAs, modern linearization techniques (digital predistortion, envelope tracking) allow GaN PAs to achieve good ACPR and EVM performance even for complex modulation schemes. Furthermore, GaN devices are inherently robust under large-signal and mismatch conditions, making them suitable for applications where high peak-to-average power ratios and dynamic loading are expected.

6. Power Density

Due to their wide bandgap and high breakdown field, GaN devices achieve power densities of several watts per millimetre of gate periphery, which significantly exceed those of GaAs or Si-based technologies. This enables compact, high-power MMICs that deliver tens of watts of RF output within a small chip area[13]. Such performance is particularly beneficial for phased array transmit modules, active antenna systems, and compact transmit/receive (T/R) modules [23], [27].

7. Thermal and Reliability Considerations

One of GaN device key strengths is its excellent thermal performance, especially when grown on SiC [21], [23] substrates with high thermal conductivity. This facilitates efficient heat removal from high-power devices operating at large drain bias and RF drive levels [22] GaN HEMTs have demonstrated robust reliability under CW and pulsed operation when properly biased and thermally managed[27]. Although self-heating and trapping phenomena must be carefully addressed in design and packaging, GaN devices are generally well suited for high-duty-cycle, high-power mm-wave operation [28].

2.4.2 Gallium Arsenide (GaAs)

GaAs pHEMT technology has historically been the mainstream process for commercial mm-Wave transceiver front ends [29]. It is often the preferred choice for PA design due to its superior high-frequency characteristics, robust thermal stability, high electron mobility, high breakdown voltage, and high-power capacity [29] GaAs is commonly employed in balanced PA designs operating in high-frequency ranges, such as the V-band (around 60 GHz) and W-band (75–110 GHz).

Key Performance Merits of GaAs Technology

The Gallium Arsenide (GaAs) Pseudomorphic High Electron Mobility Transistor (pHEMT) technology represents a mature and high-performance solution for microwave and millimeter-wave electronic circuits[30].

It benefits from decades of industrial optimization, offering high process uniformity, excellent yield, and stable performance over temperature and time.

Designers can rely on well-validated models, reproducible wafer processing, and established design kits, which significantly shorten the design-to-fabrication cycle.

This maturity translates into high product reliability and cost-effectiveness for medium-volume production, making GaAs a preferred technology in telecommunication, defense, and aerospace applications. GaAs pHEMTs are favoured due to their inherent advantages, including high electron mobility, high breakdown voltage, low noise, and high-power capacity[31].

1. Electron Mobility and Saturation Velocity

The electron mobility (μ_n) in GaAs, particularly in its purest forms at low electric fields (low-field mobility), is significantly higher than in materials like Silicon (Si)[32]. Gallium Arsenide (GaAs) has a high electron mobility of approximately 8000 $cm^2/V{\cdot}s$ [33] or 8500 $cm^2/V{\cdot}s$ [34]The high-field saturation velocity of electrons in GaAs, typically measured at room temperature (300 K), approaches values in the range of $6{-}8\times 10^7$ cm/s[12], which are considerably higher than those of silicon (≈ 1350 $cm^2/V{\cdot}s$) [1], [4].

These intrinsic material properties enable fast carrier transport within the channel, allowing transistors fabricated on GaAs substrates to operate efficiently at microwave and millimeter-

wave frequencies. As a result, GaAs-based devices can achieve short transit times, reduced delay, and enhanced gain at very high frequencies (up to and beyond 100 GHz). Such high electron transport properties directly translate into high-speed switching capability and low phase delay, which are essential for wideband and high-frequency PAs used in modern communication and radar systems.

2. Cut-off Frequency (f_t) and Maximum Oscillation Frequency (f_{max})

The combination of high mobility, low parasitic effects, and optimized device structures such as pseudomorphic high electron mobility transistors (pHEMT) and metal–semiconductor field-effect transistors (MESFETs) allows GaAs devices to reach cut-off frequencies (f_t) and maximum oscillation frequencies (f_{max}) well above 100 GHz[35].

This high-frequency potential enables high-gain amplification and efficient power delivery in the millimeter-wave regime, where conventional silicon devices suffer from excessive parasitic effects and reduced gain.

Consequently, GaAs MMICs are widely employed in front-end transmitters and receivers for applications such as 5G/6G communication, automotive radar, and satellite transceivers, where high power levels with both gain stability and phase linearity are required at high frequencies.

3. Breakdown Voltage

Compared with CMOS or SiGe devices, GaAs transistors offer a higher breakdown voltage, typically in the range of 15–25 V, depending on device gate length. As the gate length decreases, the breakdown voltage decreases [36], [37]. In GaAs pHEMTs, off-state breakdown (when the device is off) is primarily limited by tunnelling or thermionic-field emission (TFE) of gate electrons[38], [39].

Also, temperature is another important factor that can affect the breakdown voltage [39] This allows GaAs PHEMTs to operate under higher drain voltages (V_{ds}) without entering destructive breakdown, enabling larger voltage swings and higher output power.

As a result, GaAs PAs can deliver better power-added efficiency (PAE) while maintaining linear operation, which is particularly advantageous in high-efficiency or high-power applications such as satellite uplinks and point-to-point microwave systems.

The ability to withstand high electric fields also enhances device ruggedness and reliability under large-signal operation.

4. Parasitic Capacitance and Isolation

GaAs is grown on a semi-insulating substrate, which drastically reduces substrate coupling and parasitic capacitances between circuit nodes [40].

This feature minimizes signal leakage and power loss, providing excellent isolation between active and passive components integrated on the same chip[41].

As a result, GaAs MMICs exhibit superior gain stability, reduced crosstalk, and improved linearity, particularly important in multistage amplifiers and dense RF front-end layouts.

The low dielectric constant and high resistivity of GaAs also contribute to reduced substrate losses, allowing the design of compact, high-Q passive components such as transmission lines, inductors, and matching networks directly on chip.

5. Linearity and Noise

GaAs HEMTs are known for their excellent linearity and low noise performance, characteristics that stem from their smooth transconductance (g_m) behaviour and low 1/f noise.

These properties make GaAs technology particularly suitable for linear RF PAs and low-noise amplifiers (LNAs) used in high-performance communication front ends[42], [43].

In power amplifiers, linearity directly affects adjacent channel power ratio (ACPR), error vector magnitude (EVM), and spectral efficiency key parameters in modern modulation schemes such as QAM or OFDM.

The inherent low-noise figure of GaAs devices also ensures a high dynamic range, making them ideal for transceiver front-ends that demand both linearity and sensitivity.

6. Power Density

GaAs devices combine moderate breakdown voltage and high current capability, allowing power densities typically in the range of 0.5–1 W/mm for pHEMT technologies.

This balance enables the realization of compact amplifier designs capable of delivering sufficient output power while maintaining high gain and efficiency.

Such characteristics are particularly advantageous for space-constrained applications like

phased-array modules, point-to-point backhaul links, and integrated transceivers, where both miniaturization and thermal management are crucial [44].

7. Thermal and Reliability Considerations

Although the thermal conductivity of GaAs (approximately 0.46 W/cm·K) [14] is lower than that of silicon or gallium nitride, advancements in device architecture and packaging techniques effectively address these thermal limitations.

Techniques, including via-through substrates, flip-chip mounting, and metal heat-spreading backplanes, enhance thermal dissipation and support stable operation under medium-power conditions.

Furthermore, GaAs devices demonstrate high reliability under standard biasing conditions due to low trap density and stable surface passivation, which contribute to sustained performance during continuous-wave (CW) operation.

These characteristics render GaAs PHEMTs well-suited for reliable, high-frequency applications that demand moderate power and high linearity.

2.5. Conclusion of technology selection

Neither GaAs nor GaN power RF amplifiers are universally optimal; rather, each technology is advantageous under specific operating conditions. GaAs-based systems are commonly selected for applications requiring low noise, reduced signal interference, and reliable thermal performance[45]. In contrast, GaN devices are more suitable for applications that demand high voltage operation and the ability to withstand substantial heat generation. Additionally, GaN technology is often favored when high efficiency is a critical design requirement.

Both semiconductor types support the development of a wide range of amplifier architectures and can be integrated with other materials and components to enhance functionality and performance. GaAs is generally employed in larger-scale circuits and systems, whereas GaN devices, owing to their higher power density, are typically used in more compact implementations. Ultimately, the selection of semiconductor technology, component configuration, and system architecture should be guided by the specific performance requirements and constraints of the intended application.[46].

Overall, Gallium Arsenide (GaAs) particularly in regimes where high-frequency operation must be achieved without compromising efficiency, linearity, or reliability. The material's high electron mobility and advantageous transport characteristics support operation at very high frequencies while sustaining meaningful power densities, making GaAs a strong candidate for demanding applications such as satellite and space-based communication systems beyond 40 GHz[47]. In addition to enabling high-frequency performance, GaAs devices exhibit low conduction losses and favourable voltage-current characteristics, which contribute to improved linearity, reduced noise generation, and enhanced power efficiency. These properties also ease broadband impedance matching and reduce implementation complexity in advanced PA architectures [48], including load-modulated designs [49], [50]. Coupled with decades of technological refinement, proven operational robustness, and established qualification for space environments, GaAs continues to offer a balanced and trustworthy solution [47], [51], [52], [53]. Its widespread adoption in mobile and high-frequency RF systems further demonstrates its adaptability and long-term relevance in modern and emerging power amplifier applications.

Chapter 3

Device Level Analysis: Process Validation, Device Characterization, and Modeling

3.1 Introduction

In this chapter, a comprehensive device-level analysis is presented, starting with process validation, followed by on-wafer characterization, and small-signal modeling of the GaAs device, which is also employed for design-level purposes. As mentioned in the previous chapter, the GaAs HEMT is a semiconductor technology well suited to the requirements driving the development of microwave electronics, ranging from mobile communication and radar systems to satellite communications and, more generally, millimeter-wave applications

An improved version of the conventional HEMT is the pseudomorphic HEMT (pHEMT), which enables enhanced electron transport and improved electron confinement in the channel as a result of a larger bandgap difference [54]. Pseudomorphic HEMTs (pHEMTs) and traditional lattice-matched HEMTs have been fabricated using various material systems, such as Gallium Arsenide (GaAs) and Gallium Nitride (GaN). Furthermore, advanced device concepts exploiting two-dimensional electron gas (2DEG) channels in multiple dimensions,

including designs with a two-way heterojunction instead of a single heterojunction, have been proposed, as illustrated in Figure 3. 1.

The device has three terminals, i.e., gate, drain, and source, and, as in other FET devices, when a positive voltage VDS is applied, the current flows from drain to source (electrons move in the opposite direction) inside the channel, which lies in an undoped GaAs layer. The drain current magnitude can be modulated by the voltage applied to the gate terminal, which is realized by a Schottky junction.

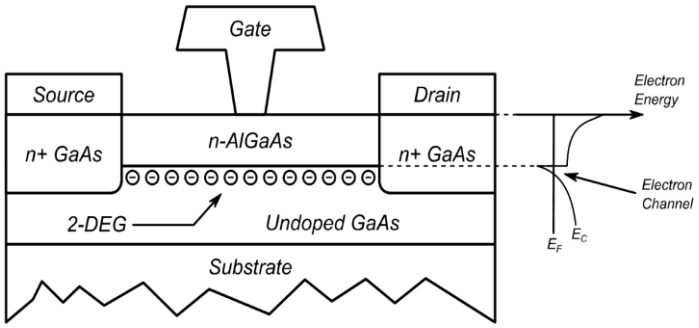

Figure 3. 1: Cross-section of an AlGaAs/GaAs HEMT

The key element of this device can be identified by examining the energy-band structure near the heterojunction between AlGaAs and GaAs. Here, a wide-band gap material (i.e., AlGaAs) interfaces with a low-band gap material (i.e., undoped GaAs). In this condition, the conduction-band level decreases below the Fermi level, although for a limited area, in the undoped GaAs. This phenomenon is confined to a very shallow region, resulting in a thin layer where the electron density is extremely high. This layer of electrons, referred to as a two-dimensional electron gas (2-DEG), lies within an undoped material; therefore, charge mobility is very high, as impurity scattering is absent. These characteristics guarantee high drain current and a very high operating frequency.

The design of this type of transistor depends on physical factors, such as gate width (W) and length (Lg), as well as on its use, including the frequency range and power settings.

The analysis of technology reliability is important for identifying and understanding degradation mechanisms that may cause performance limitations or premature failure. This is especially true when technology operates at its limits to meet the stringent requirements of demanding new applications [49]. To optimize performance and reliability across the

millimeter-wave regime, it is essential to adopt a methodology that efficiently characterizes process variants, such as accelerated life testing, statistical analysis of failure data, and real-time monitoring of device parameters. This approach should quickly extract key information on device robustness and performance metrics such as output power, efficiency, and maximum operating frequency. Evaluating the impact of well-known dispersive effects using frequency-dependent measurements and transient response analysis is equally important for improving the technological process and clarifying the suitability of a given technology for specific applications.

3.1.1 The low-frequency dispersion phenomena

Low-frequency dispersion refers to a resistive core of the device (which will be described in the following section), slow dynamic phenomena that induce frequency dependence in the electrical behavior of electron devices at low frequencies, despite the assumption of a frequency-independent intrinsic current generator. In contemporary microwave transistors, this effect primarily results from thermal phenomena and charge-trapping mechanisms, each exhibiting long time constants from microseconds to seconds[55].

Self-heating is related to the dissipated power on the device, producing a temperature increase. In FETs, this induces a reduction of electron mobility, which is responsible for a reduction of the current flowing through the channel of the device. This directly lowers the drain current and modifies the slope of the current-voltage (I/V) characteristics. Because thermal time constants are much longer than the RF signal period, the thermal state is governed by average voltages, currents, and delivered RF power rather than by instantaneous RF swings.

Trap states within the semiconductor bulk or at material interfaces represent another significant source of dispersion. The occupancy of these traps is governed by the local electric field, which depends on intrinsic gate–drain and drain–source voltages. During DC measurements, trap occupancy adjusts to the applied bias. In contrast, under RF large-signal operation, traps are unable to respond to rapid signal variations, resulting in a “frozen” state determined by average intrinsic voltages. This discrepancy between DC and dynamic conditions leads to distinct current–voltage characteristics.

This produces a difference between DC and dynamic current-voltage (I/V) characteristics, as qualitatively illustrated in Figure 3. 2. Three primary consequences are identified:

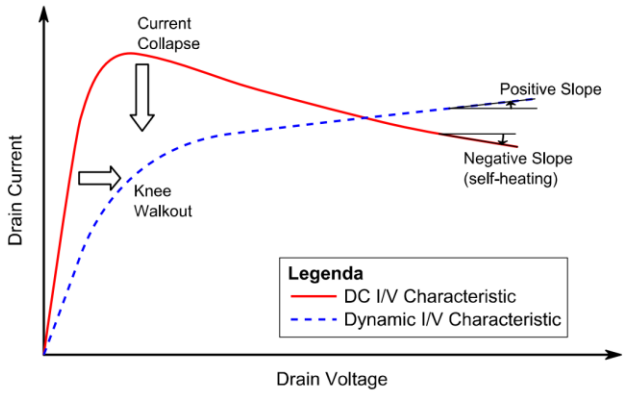

Figure 3. 2: Qualitative example of the effects of low-frequency dispersion in active devices

• A reduction in the maximum drain current, indicated as current collapse.

• A variation of the slope within the linear region of the I/V characteristics, resulting in a deviation of the dynamic knee voltage compared to the DC knee voltage.

• A change of the slope of the I/V characteristics in the saturation region, the DC characteristics present a negative slope due to self-heating.

These effects are clearly visible when comparing DC I–V curves with dynamic load lines measured at low frequencies above the dispersion cutoff (typically 100 kHz–1 MHz). Small-signal measurements further reveal dispersion: Y-parameters exhibit pronounced frequency dependence below a few hundred kilohertz, while becoming nearly constant above this range, indicating that the resistive core achieves stability only beyond the dispersion band.

An important consequence emphasized in the thesis is that DC measurements alone are not sufficient to predict RF performance. Low-frequency dispersion causes significant discrepancies between DC-extracted models and actual RF behavior, leading to errors in output power, efficiency, and load-line prediction. This is particularly critical for high-efficiency power amplifier design.

To address this issue, the thesis proposes low-frequency large-signal characterization as an effective alternative to pulsed I–V techniques. Operating at 2 MHz allows direct access to the

intrinsic current generator under realistic conditions. This approach facilitates accurate extraction of dynamic I–V characteristics which will explain in detail in the following section.

3.2 Technology evaluation and device characterization and modeling needs

In this section, the proposed characterization procedure is described, aimed to give a quick technology evaluation; the first step of the proposed procedure is the evaluation of technology robustness by means of 24-hour accelerated stress measurements at 80 °C under real operating conditions. This is one of the crucial steps of each characterization because, if the technology is not sufficiently stable, it is useless to proceed with further performance characterization. Following this large-signal low-frequency (LSLF) characterization, the impact of low-frequency dispersion phenomena is evaluated on the one hand, and the performance in terms of output power, drain efficiency, dynamic breakdown voltage, etc. is evaluated on the other hand [50]. Furthermore, multi-bias S-parameter measurements are essential for capacitance parameter extraction because they provide small-signal transistor parameters across multiple bias points, which are necessary to characterize the device's nonlinear reactive behaviour; this topic will be discussed in detail in the following section of this chapter.

3.2.1 Devices under test and experimental degradation test setup

The device under test (DUT) are on-wafer GaAs pHEMTs fabricated by United Monolithic Semiconductors (UMS). The studied pHEMT is mounted on a brass carrier and have a gate length of 0.1 µm and gate width of 6 × 40 µm as shown in Figure 3. 3.

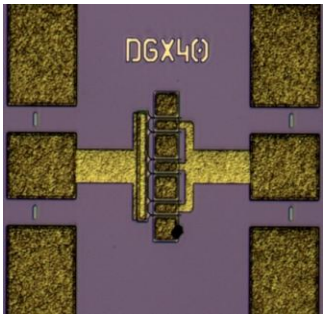

Figure 3. 3: Micrograph of GaAs Device Under Test

The schematic of the setup implementing the measurement technique is shown in Figure 3. 4 and Figure 3. 5 [56], [57]. The DUT is biased by a DC source measure unit (SMU, HP 4155B) with high resolution (4 µV; 20 fA) and accuracy (V: 0.05%, I: 0.2%). Two bias tees are used to supply DC currents or voltages to RF devices; on the input side, a commercial bias tee is used (Minicircuit ZX85-12G-S+, frequency range: 200 kHz–12 GHz); while on the output side, a customized bias tee has been designed to support high-power levels (frequency range: 200 kHz–200 MHz, maximum voltage: 100 V, maximum current: 2 A, and power handling: 30 W). These components provide DC-to-AC isolation and prevent low-frequency instabilities of the DUT. Two dual-directional couplers, operating in the 10 kHz–400 MHz frequency range, are used to separate the incident and reflected waves at the input and output ports of the DUT. The separated wave components are then routed to a 12-bit, 350-MHz, four-channel oscilloscope (Tektronix MSO54), which simultaneously acquires the incident and reflected waves at both DUT ports. The input signal is supplied by an arbitrary function generator (Tektronix AFG 3252) whereas the DUT output is terminated by passive loads as shown in Figure 3. 6. Operating at a few megahertz enables direct control of the current-generator load. Once the class of operation to be investigated is defined, the corresponding load conditions at the fundamental and harmonic frequencies can be determined and synthesized. For this purpose, an electronically controllable tuner coupled with a frequency multiplexer was designed and produced, which controls the load impedance up to the third harmonic. This configuration allows the synthesis of both conventional and high-efficiency classes of operation that require harmonic manipulation of the load, such as class-F.

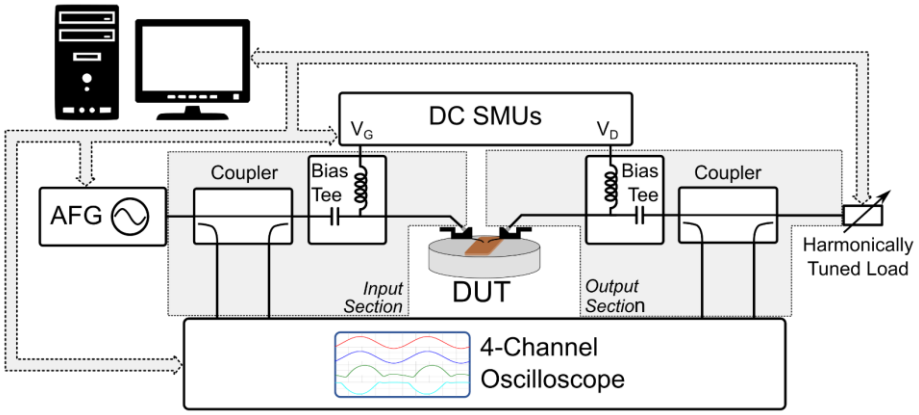

Figure 3. 4: Schematic of the low-frequency time-domain load-pull setup.

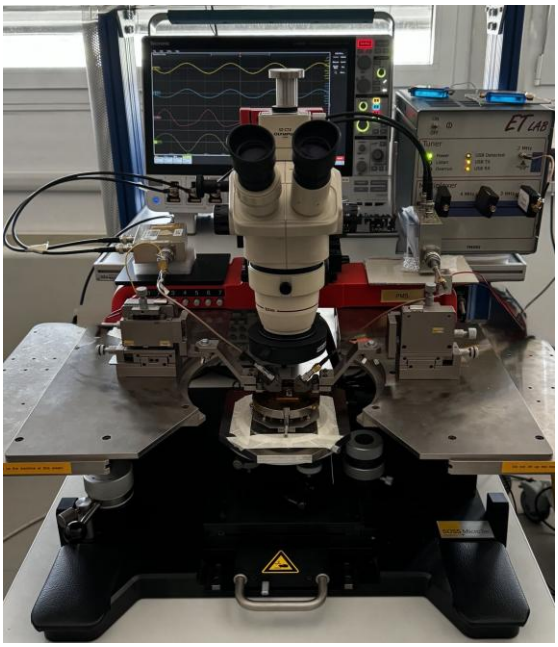

Figure 3. 5: Experimental setup of the low-frequency time-domain load-pull setup

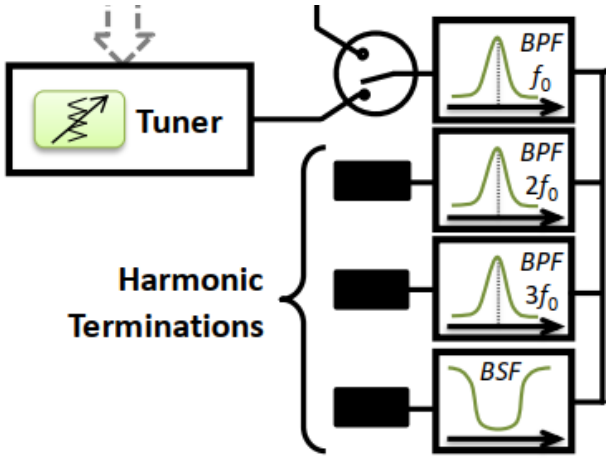

Figure 3. 6: Detailed schematic for Harmonically tuned load setup

The setup is fully controlled by an internally developed software, which includes the capability to implement a stress-measurement routine to evaluate the degradation effects of the specific operating condition applied to the DUT. It is worth noting, the calibration of the measurement system is not critical since it operates at low frequency and remain stable over long time period (i.e., days). The software enables users to organize automatic measurements that are performed sequentially on the DUT.

3.2.2 Scattering Parameter Characterization

At high frequencies, Scattering Parameters (S parameters) are used to characterize the small signal dynamic behavior of devices. MS4647B Anritsu Vector Network Analyzer (VNA) and the HP4155B DC source are employed to acquire S-parameters. The schematic of the S-parameter measurement is shown in Figure 3. 7 and a picture of the used for this work is reported in Figure 3. 8. Custom PC software controls the entire measurement process by setting a bias grid for gate and drain voltages and automatically conducting DC I/V and S-parameter measurements across the entire grid within the defined safe operating area.

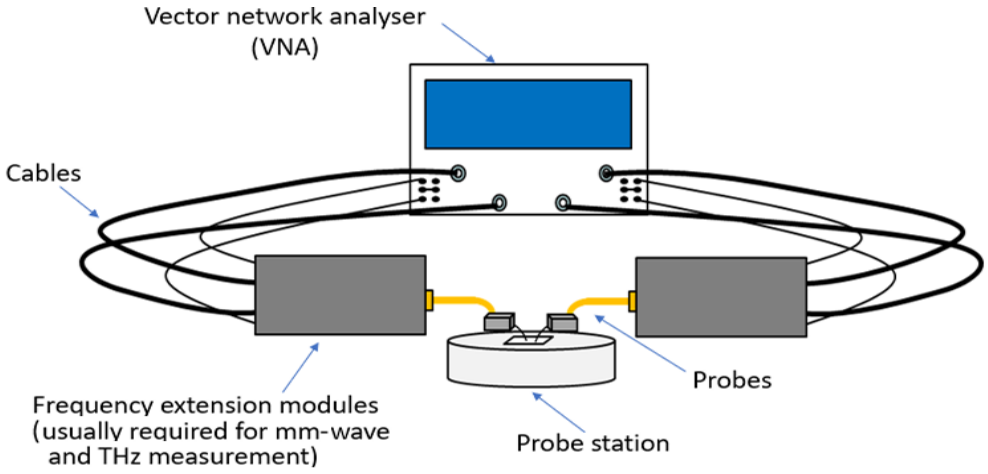

Figure 3. 7: Diagram of a typical on-wafer S-parameter measurement system [58]

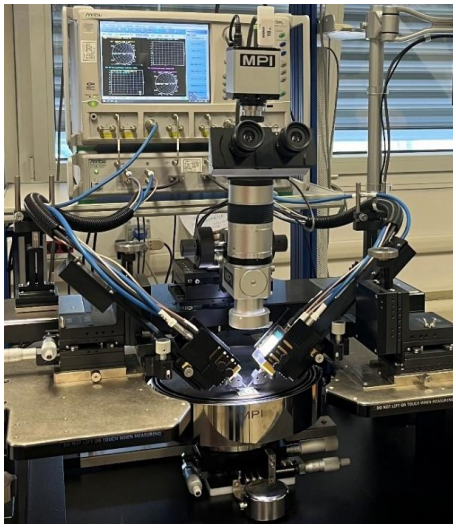

Figure 3. 8: Measurement test bench used for on-wafer small signal characterization, including VNA, probe station, and probes

Before performing S-parameter measurements, vector error correction, commonly known as calibration, must be applied. Calibration techniques play a key role in determining the accuracy of on-wafer measurements because they depend on the probe tip positions; therefore, it is necessary to accurately define the measurement reference plane.

Calibration involves characterizing the systematic errors inherent to the VNA by measuring well-defined reference devices, referred to as calibration standards. After identifying these systematic errors, their effects are mathematically removed from the raw measurement data.

Instrument calibration requires connecting known loads, or calibration standards, to the device under test (DUT) planes. Multiple calibration techniques and associated sets of calibration standards exist, each tailored to specific applications and accuracy requirements.

Typically, a calibration procedure establishes the measurement reference planes at the ends of prob tips, which removes the influence of cables and connectors from the measured device response. Calibration can be performed on one or multiple ports, depending on the measurement requirements.

Modern calibration algorithms are designed to minimize the number of required physical connections while maintaining high accuracy. For example, in multiport measurements, connecting a through standard between every possible pair of ports is not necessary. Generally, depending on the type of test-port connectors used, one or more ports must be connected to reflection standards, followed by n − 1 through connections, where *n* represents the total number of measurement ports [59].

3.2.3 Calibration Methods

Two main calibration approaches are commonly adopted for on-wafer measurements. First approach, usually probe manufacturers specify calibration coefficients obtained using a commercial Impedance Standard Substrate (ISS) (off wafer) calibration. In the second approach, calibration is performed directly on the wafer using standards fabricated on the same substrate as the DUT.

It is important to understand the strengths and limitations of each calibration technique; therefore, the following sections provide a detailed explanation of each method.

• Short-Open-Load-Thru (SOLT): it requires short, open, load and thru calibration standards as it is in Figure 3. 9 defined at the characteristic system. The exact values of these standards, determined by their mechanical dimensions, are loaded into the VNA prior to calibration. The point at which the calibration standards are connected, such as the analyzer port, the end of a cable, or inside a test fixture, defines the reference (measurement) plane. The point where the calibration standards are applied defines the reference (measurement) plane, meaning the electrical location to which the measured S-parameters are referred after calibration.

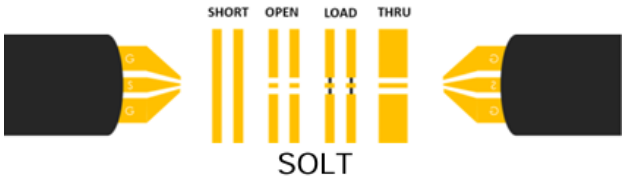

Figure 3. 9: SOLT calibration standards [58]

Any component used during calibration but removed during the actual measurement introduces systematic error.

Several variants exist within the SOLT family. Response calibration is the simplest and fastest, but it only corrects for forward and reverse tracking errors and is equivalent to compensating for frequency-dependent path loss. A one-port calibration uses short, open, and load standards on a single port and is suitable for measurements such as antenna return loss. An enhanced one-port calibration performs a full one-port calibration on port one and uses a through connection to characterize port two, which is common in T/R architectures where no source is present on the second port. Full two-port SOLT calibration applies short, open, and load standards to both ports and concludes with the thru measurement [60].

The SOLT requires accurate and well-defined calibration standards. While the method is robust when standard definitions are accurate, the calibration coefficients are valid only for a specific probe placement (i.e., the reference plane is at the probe tip planes). As a result, SOLT is relatively sensitive to probe placement errors, which are unavoidable in microwave probing environments[58].

• Thru-Reflect-Line (TRL): The standards shown in Figure 3. 10 is one type in a family of two-port calibrations that better support noncoaxial environments, such as on-wafer measurements and test fixturing. In this family, the calibration name is an acronym that identifies the calibration standards.

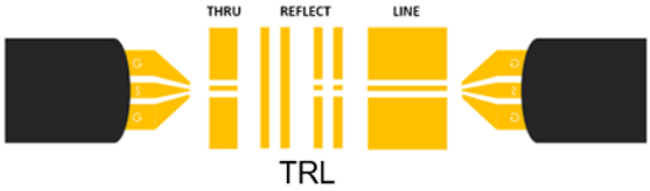

Figure 3. 10: TRL calibration standards [48]

Fewer calibration standards, typically three, are required for this family of calibrations, compared to SOLT calibrations. In noncoaxial environments, although standards are more difficult to obtain, they are generally easier to fabricate than implementing coaxial calibration and measurement setups. Calibration accuracy strongly depends on the quality and repeatability of these standards.

TRL is a calibration technique that uses fewer standards and requires less a priori knowledge of their electrical characteristics. It is particularly well-suited to noncoaxial environments, where conventional calibration standards are difficult to fabricate and accurately characterize. Although TRL requires high-quality and repeatable standards, much of the standard characterization is extracted directly from the measurements, reducing reliance on predefined models. The usable frequency range is limited by the need to distinguish standards based on their phase relationships, but this constraint can be extended by introducing additional standards. TRL generally provides higher accuracy than SOLT, as it avoids dependence on mechanical standard models.

In this method, the reference plane is usually set at the centre of the Thru standard, but it can be easily shifted if needed. Reflect standard can be either Short or Open, but identical reflects are required on both ports. Line standard (with electrical phase around 20° ~ 160° at test frequencies) provides information about the characteristic impedance of the transmission line. Each LINE standard can only cover a limited frequency range; hence, multiple lines are required for broadband measurements

• Multi-Line TRL (MTRL): developed by NIST, has become established as a reference calibration technique. MTRL involves multiple lines and uses all lines, to some extent, in the

frequency range. Varying weighting is applied to all the LINE data to resolve the problem of band breaks of conventional TRL [58].

• Line-Reflect-Match (LRM): this method is similar to TRL; the characteristic impedance is determined by the Match standard (equivalent to an infinitely long reflectionless line). The reference plane is set at the middle of the LINE standard. The REFLECT standard can be either SHORT or OPEN, as shown in Figure 3. 11; however, it should again be 2 identical on both ports. LRM does not need knowledge about parasitic capacitance of OPEN or parasitic inductance of SHORT. However, the behaviour of the MATCH needs to be well understood [58].

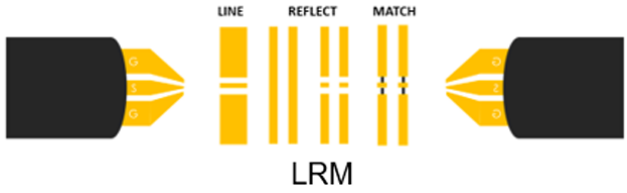

Figure 3. 11: LRM calibration standards [58]

• Line-Reflect-Reflect-Match (LRRM): the reference plane of LRRM is usually set at the middle of the LINE. REFLECT does not require known OPEN or SHORT; however, it must be equal at both ports. MATCH standard could have known resistance and unknown inductance (assumed constant with frequency). MATCH inductance is calculable using OPEN. LRRM requires one MATCH standard, as shown in Figure 3. 12; whereas LRM needs two. LRRM requires the same set of standards as SOLT, but requires less information about the standards. This can give better results than SOLT and is less sensitive to small errors in probe placement [58].

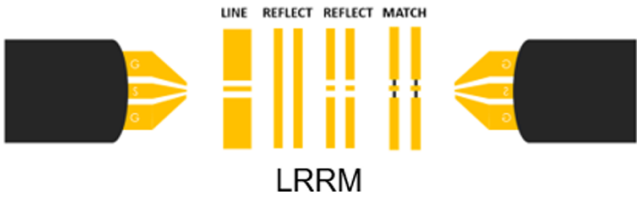

Figure 3. 12: LRRM calibration Standard [58]

Line-Reflect-Match (LRM), Line-Reflect-Line (LRL), and Thru-Reflect-Match (TRM) calibrations derive error terms for the same 12-term error model as SOLT calibrations. Additional information about the port match of the hardware is required to the correct perfect-match assumptions used to derive these calibration models [58].

The methods use combinations of through, line, reflection, and match standards, as summarized in Table 3. 1. Among the described methods, MTRL offers the best performance for on-wafer millimeter-wave calibration. The implementation of multiple transmission lines extends the valid bandwidth while maintaining the high accuracy of TRL.

Technique	Standards	Bandwidth	Accuracy (on wafer)	Key advantage	Main drawback
SOLT	Short, Open, Load, Thru	Wide	Low at mm-wave	Simple, fast	Open/load parasitics
TRL	Thru, Reflect, Line	Limited	High	Accurate at mm-wave	Narrowband per line
LRM	Line, Reflect, Match	Moderate	Medium	Layout-friendly	Load quality sensitive
LRRM	Line, Reflect, Reflect, Match	Moderate	Medium–High	Better reflect modeling	Increased standard count
MTRL	Reflect, multiple Lines	Wide	Very high	Broadband mm-wave	Higher complexity

Table 3. 1: comparison between conventional calibration techniques

A MTRL calibration is used work this work. This approach is motivated because a significant fraction of the measurement error is introduced downstream of the probe tips, which cannot be eliminated by off-wafer or factory calibration alone. For precise and accurate characterization, which is essential for model extraction, it is necessary to move the measurement reference plane to the DUT level and remove the parasitic effects of pads and launchers. Additional considerations for accurate millimeter-wave on-wafer measurements are outlined below.

1. Removal of Systematic and Drift Errors

The primary purpose of VNA calibration is to eliminate systematic and drift errors, which become particularly critical at high frequencies. On-wafer calibration corrects these errors directly within the measurement environment of the DUT.

2. Matching the Reference Plane

On-wafer calibration places the calibration reference plane at the same location as the DUT, ensuring the extracted S-parameters represent the intrinsic device behavior, free from probe, pad, and transition effects.

3. Mitigating Launch Differences

At millimeter-wave frequencies, electromagnetic boundary conditions, such as the chuck or supporting material beneath the wafer, significantly influence transmission-line behavior. On-wafer calibration ensures these effects are consistently accounted for.

This is caused by differences in pad layouts, substrate dielectric constants, and substrate thicknesses.

4. Accounting for Testing Boundary Conditions

At millimeter-wave frequencies, electromagnetic boundary conditions strongly influence measurement accuracy. A metallic chuck may excite spurious modes and alter the characteristic impedance and phase constants of the transmission lines. On-wafer calibration ensures these effects are consistently accounted for, as the calibration standards and DUT experience the same measurement environment.

5. Managing High-Frequency Parasitic Effects

Measurement accuracy is also affected by factors like crosstalk between probes and coupling with neighbouring structures. On-wafer calibration helps manage these parasitic effects because the standards are subject to the same proximity effects and coupling as the DUT.

3.3 Degradation test (Stress measurement)

To use the low-frequency system to investigate device degradation, we used the control software that is mentioned before. It can perform DC stress, where the bias point is applied to the DUT for a certain amount of time and DC currents are sampled at regular intervals, but it can also perform large signal low-frequency stress, where not only the bias point is applied to the DUT, but it is also excited with an input signal and terminated on the proper load impedances at fundamental and harmonics. Both the DC currents and the input and output voltage and current waveforms are periodically sampled, providing a complete overview of the evolution of the transistor dynamic behaviour vs time.

Stress measurements are typically divided into multiple sessions, as shown in Figure 3. 13. In each stress session, a specific operating condition is applied to the DUT for a defined duration (e.g. 4 hr as shown in the Figure 3. 13), while the main electrical parameters are periodically monitored and sampled with customizable sampling time. The stress sessions are interspersed with control measurements, which are conducted under operating conditions different from those used for stress, to monitor variations in other relevant device parameters. These control measurements may include conventional DC I-V characterizations as well as other low-frequency measurements, enabling the investigation of device behavior under different operating conditions.

To enable the investigation of microwave device degradation using a low-frequency measurement system, a dedicated control software was developed to automate the stress measurements. The software enables DC stress measurements, where a fixed bias point is applied to the DUT for a defined period, and DC currents are sampled at regular intervals. Additionally, the system supports low-frequency stress measurements, in which the DUT is both biased and excited by an input signal while terminated with suitable load impedances. In this configuration, both DC currents and the input and output voltage and current waveforms are periodically sampled, offering a comprehensive assessment of the temporal evolution of the transistor's dynamic behaviour.

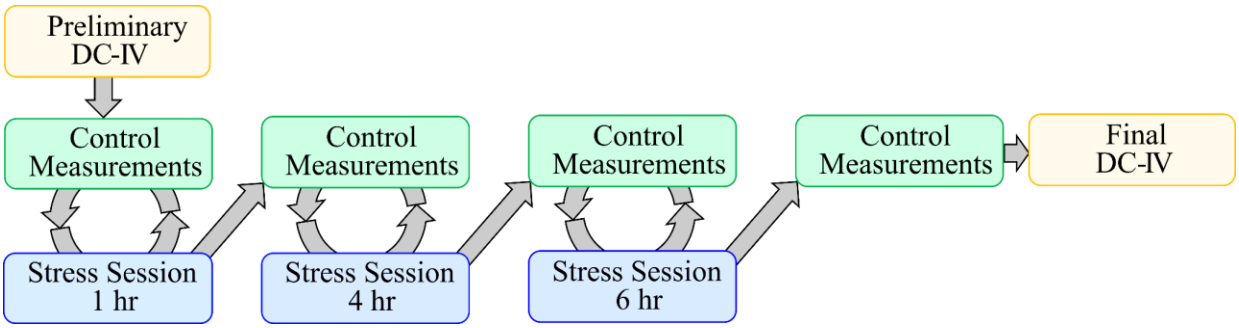

Figure 3. 13: Block diagram of Stress measurement

The stress sequence applied to the DUT is schematically represented in the diagram. The initial state of the device was first established through a preliminary measurement of the complete current–voltage (I–V) characteristics. This full I–V characterization was repeated at the end of the stress sequence to enable a direct comparison with the initial device condition. Following the preliminary assessment, the measurement protocol proceeds with alternating control measurements and stress sessions.

For control measurements, the Id–Vg transfer characteristic was used to monitor potential variations in threshold voltage, while the Ig–Vd characteristic was employed to assess changes in sub-threshold gate current. The stress condition was applied across multiple sessions, resulting in a total cumulative stress duration of 24 hours.

In summary, the stress measurement procedure comprises multiple stress sessions interleaved with control measurements conducted under conditions distinct from the stress bias. This methodology enables monitoring of various device parameters and supports the use of both conventional DC and low-frequency measurements to investigate different operating regimes.

3.3.1 Low-frequency stress

A large-signal operating condition at a low frequency is applied to the DUT for a time T_{stress}, during which both average currents and voltages, as well as the incident and reflected waveforms, are periodically measured. The sampling time for the DC quantities (Ts, DC) and for the waveforms (Ts, AC) can be different. The motivation for employing large-signal measurements is explained in the following section.

The available control measurements are:

DC measurements: DC I/V characteristics are measured over a predefined grid of bias points.

Low-frequency measurements: a large-signal low-frequency characterization is carried out on the DUT. The investigated condition can differ from the one used for stress measurement, and the user can choose between a single load line and a power and load sweep.

The stress measurement has been carried out on a fresh device sample with a 6x40 µm periphery. The stress condition has been set by applying a realistic class-AB load line at 2 MHz under a drain bias voltage of 3 V, and a corresponding current of 26 mA. The synthesized load is 37.7 Ω at fundamental with shorted harmonics, resulting in an output power of 17.16 dBm and a drain efficiency of 47.7%. This stress condition was maintained on the transistor for 24 hours at a carrier temperature of 80 °C, with periodic monitoring of input and output waveforms to evaluate device performance, as shown in Figure 3. 14. The black segment represents the initial stage of the stress measurement, while the red segment corresponds to the later stage as the stress measurement progresses toward the end of the experiment. A minor reduction in output power is observed (approximately -0.1 dB after 24 hours), while efficiency remains largely unchanged, as shown in Figure 3. 14. Data collected prior to the stress test are represented by black lines, and data collected afterward are represented by red lines. Using the same setup, DC measurements were conducted before and after the 24-h stress test to check for significant degradation effects, such as the shift of the threshold voltage and the breakdown walkout [57]. The results of this DC measurement are shown Figure 3. 15. The data indicate excellent device stability, with minimal variation in measured performance metrics.

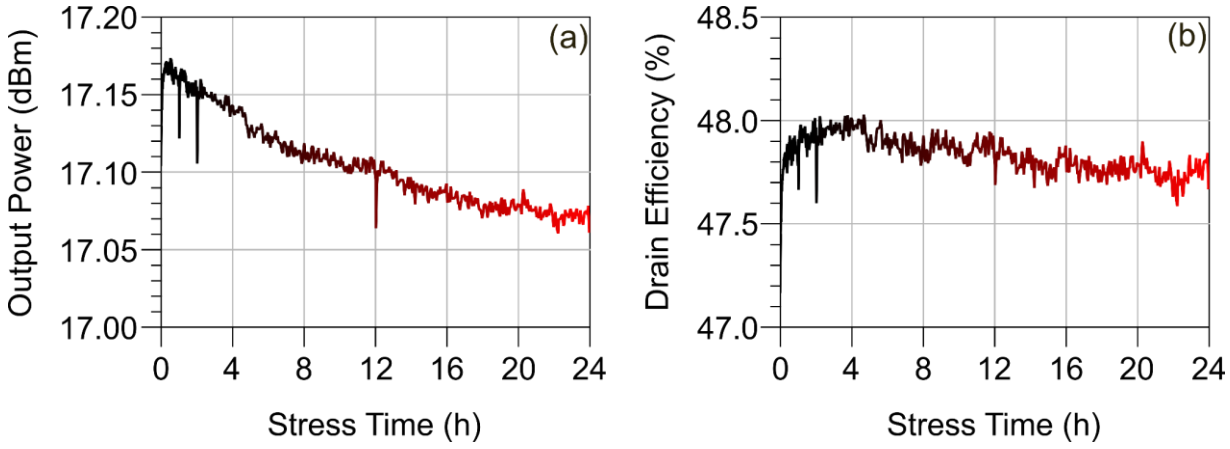

Figure 3. 14: Stress measurement results: on the left, output power, on the right, drain efficiency vs. stress time

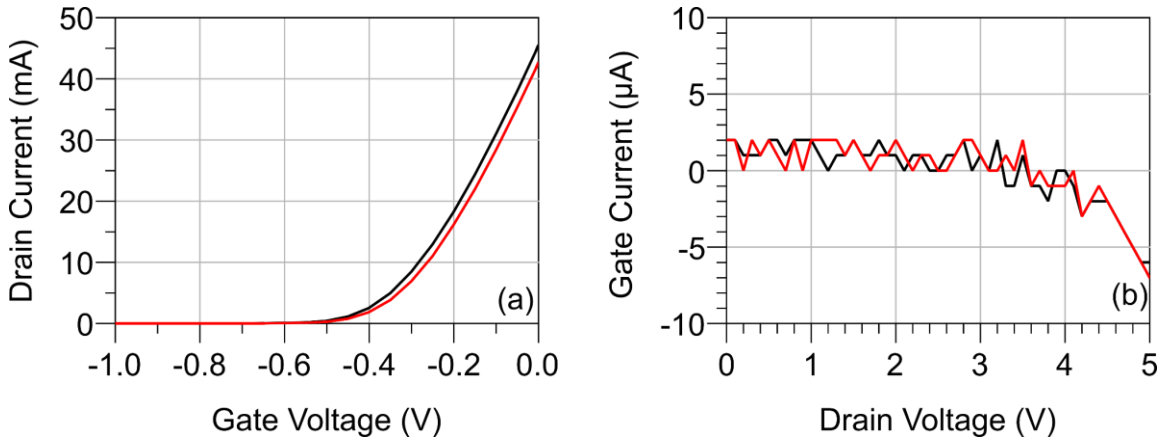

Figure 3. 15: DC characteristics before and after the stress. (a) ID-VG transcharacteristic at VD = 3 V; (b) IG-VD transcharacteristic at VG = -1 V. Data acquired before (black lines) and after (red lines) the 24-h stress measurement are reported

A slight change in the load line after the stress is reported in Figure 3. 16, perhaps due to the small shift in the threshold voltage, visible in Figure 3. 15(a) which is estimated to be approximately 20 mV.

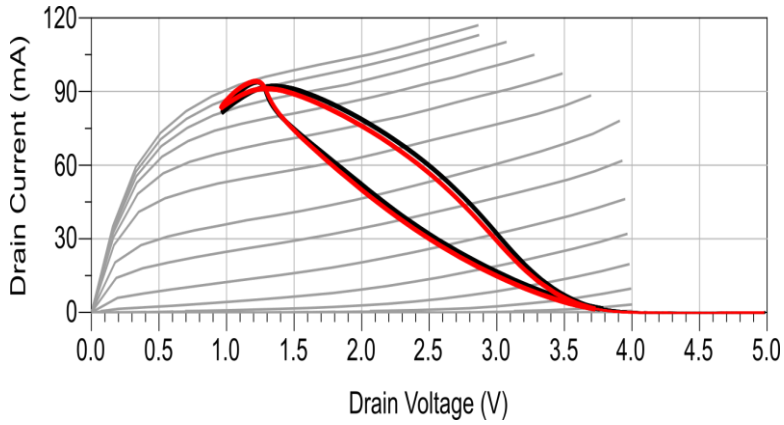

Figure 3. 16: Class-AB stress load line at 2 MHz and DC Preliminary before (black lines) and after (red lines) stress

Figure 3. 15(b) also demonstrates the technology's stability by showing the sub-threshold gate current. Although this parameter is sensitive to device degradation, no significant changes are observed after the 24-hr stress. These results confirm the robustness of the technology and support the accuracy and representativeness of the subsequent characterization campaign.

3.4 Performance Evaluation

Following confirmation of technology stability, comprehensive characterization was conducted.

3.4.1 Static DC I-V Characterization

Direct current (DC) characterization was performed on a fresh 6 × 40 µm device from the same wafer. The measured DC I_D-V_D, presented in Figure 3. 17(a) were obtained at 30 °C (blue curves) and 80 °C (red curves) for a range of V_{GS} from -1 V to 0.8 V with a 0.1 V step size. As anticipated, the drain current decreases with increasing temperature. I_D-V_G characteristics are shown in (b). Variations in gate current remain negligible, as shown in Figure 3. 17, which further supports the robustness of the technology and aligns with the stress test results. This behaviour suggests that thermal effects have only a moderate influence on the current-voltage (I–V) characteristics. It is worth mentioning that under static operation, each point of the I/V characteristics has a different trap occupation state (which depends on the electric field between the gate and the drain).

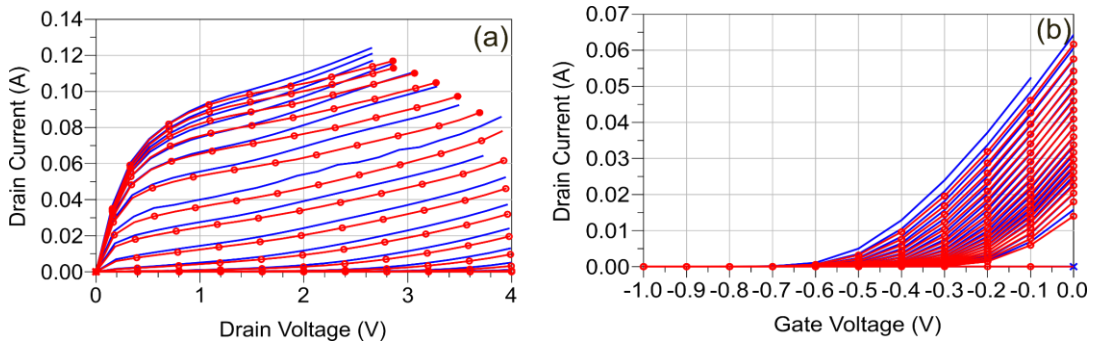

Figure 3. 17: DC I-V characteristics in different Temperatures: 30 °C (blue lines) and 80 °C (red lines)

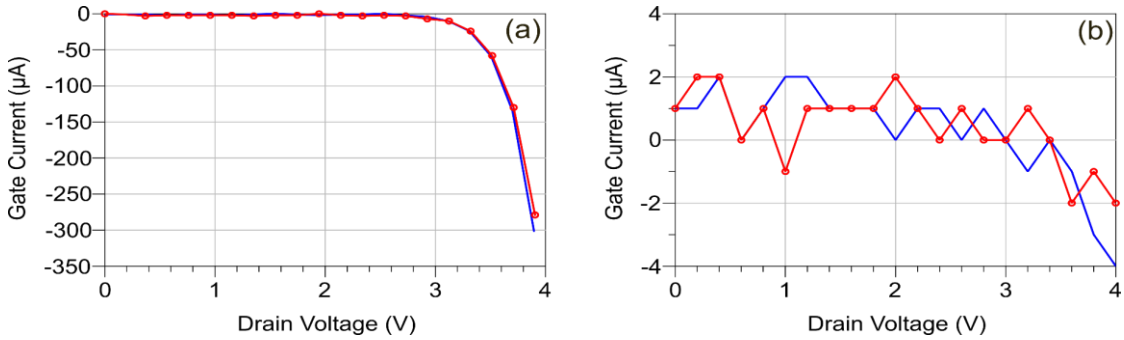

Figure 3. 18: DC characteristic Gate Current a) VG = -1V, b) VG = 0.1V in different Temperatures: 30 °C (blue lines) and 80 °C (red lines)

3.4.2. large-signal low-frequency (LSLF)

It is of crucial importance to characterize the transistor behavior under different operating regimes and at different temperatures. To this end, large-signal characterization at low frequency is performed using the setup that is presented in Figure 3. 4.

The motivation for large-signal low-frequency (LSLF) measurements lies in different points, which will be explained in this part in detail, starting from the most important one:

Consistency with Microwave Operation: the MHz range is specifically chosen because it sits above the cut-off frequency of low-frequency dispersion phenomena, such as self-heating (thermal effects) and trapping. Consequently, the data gathered at these frequencies is directly consistent with how the device will behave under actual microwave (GHz) operation.

Negligible Reactive Effects: In the megahertz range, all the linear and nonlinear reactive effects can be considered negligible. This allows researchers to treat the transistor as an approximately resistive component and directly observe the intrinsic active part of the device, as the current-generator and the Schottky junction.

Direct Monitoring of the Gate Current: The instantaneous resistive gate current is a sensitive indicator of device degradation and reliability. While reactive currents at higher frequencies mask it, LSLF measurements allow clear acquisition of gate current waveforms, revealing whether the device is experiencing critical forward or reverse conduction.

Realistic vs. DC Stress Testing: Unlike DC stress tests, which may fail to trigger degradation mechanisms like the hot-electron effect, LSLF conditions are consistent with realistic RF stress tests.

Accurate Modeling and Design: LSLF characterization allows exhaustive characterization of the resistive core, capturing thermal and trapping effects that DC measurements cannot gather and that can be used for accurate modeling of the current generator. Moreover, LSLF can be used for waveform engineering, where we can shape

voltage and current waveforms directly at the current-generator plane to achieve theoretical classes of operation such as Class F, inverse Class F, or Class E.

In addition to their technical advantages, large-signal low-frequency (LSLF) setups significantly reduce experimental cost and complexity. These setups use relatively simple instrumentation, such as oscilloscopes and arbitrary waveform generators, for device characterization in this study. LSLF setups also eliminate the need for costly large-signal microwave measurement systems, complex calibration procedures, and the strict power-handling requirements associated with high-frequency characterization of large-periphery transistors.

Figure 3. 19 presents the output power measured at LSLF on the DUT (i.e., the 6x40 µm) under the bias conditions VG = -0.25 V, VD = 3 V, and ID = 11 mA by sweeping the load and the input power. At f_0= 2 MHz, the maximum output power and drain efficiency are approximately 17 dBm and 60 %, respectively, as shown in Figure 3.19 and in Figure 3. 20 respectively.

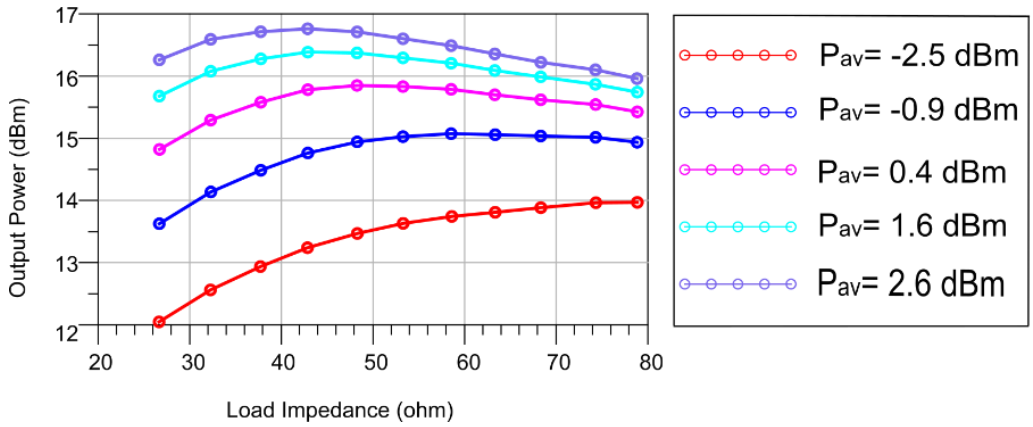

Figure 3. 19: Output power measured on the 6x40-µm GaAs pHEMT at f_0 = 2 MHz, V_G = -0.25 V, V_D = 3 V, I_D = 11 mA by sweeping the load impedance from 25 Ω to 80 Ω and input power from -16 dBm to -0.8 dBm.

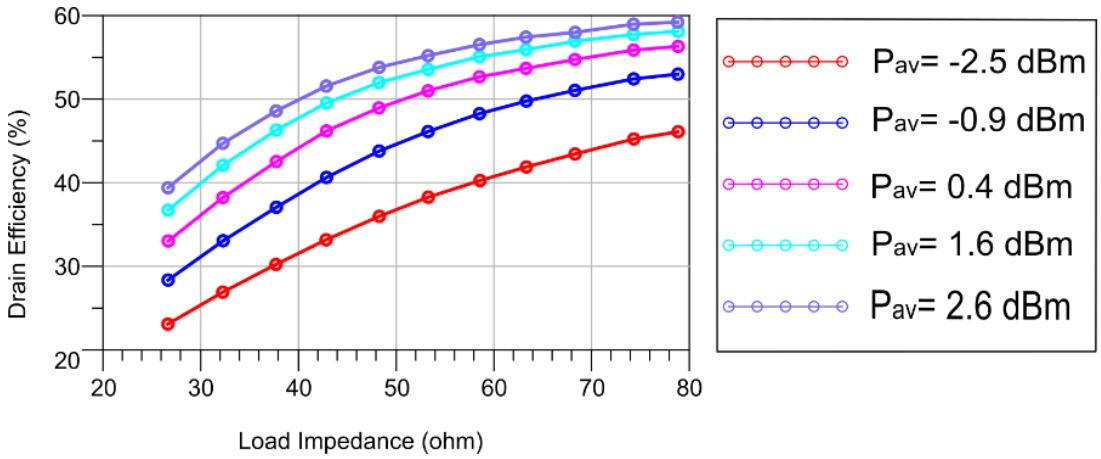

Figure 3. 20: Drain Efficiency measured on the 6x40-µm GaAs pHEMT at f_0 = 2 MHz, V_G = -0.25 V, V_D = 3 V, I_D = 11 mA by sweeping the load impedance from 25 Ω to 80 Ω and input power from -16 dBm to -0.8 dBm.

Figure 3. 21 shows the load lines and the drain and gate time-domain waveforms measured at the highest input power level, $P_{\text{av}} = 2.6$ dBm, corresponding to a peak gate voltage of 0.3 V. The measurements were performed at $f_0 = 2$ MHz with bias conditions $V_G = -0.25$ V, $V_D = 3$ V, and $I_D = 11$ mA. Under the constant input power of -0.8 dBm, the load impedance was swept from 28 Ω to 80 Ω.

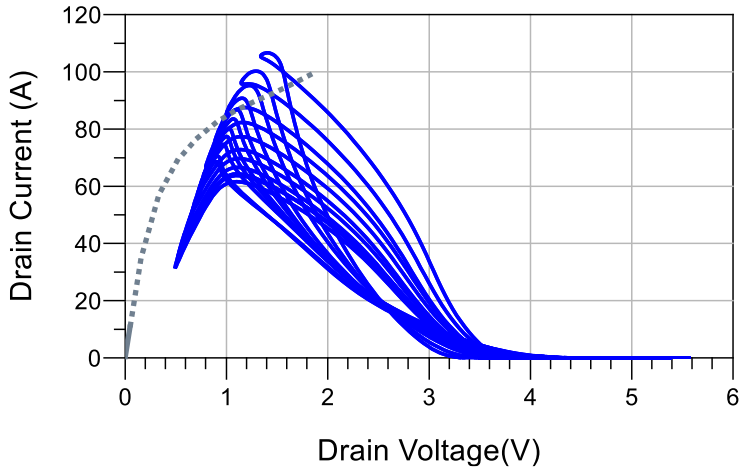

Figure 3. 21: Load Lines (blue lines) measured on the 6x40-µm GaAs pHEMT at f_0 = 2 MHz, V_G = -0.25 V, V_D = 3 V, I_D = 11 mA for the constant input power -0.8 dBm, by sweeping the load impedance from 25 Ω to 80 Ω. DC I-V characteristic at VG = 0.3 V is superimposed on the load lines (grey dotted line).

A slight knee walkout is evident in Figure 3. 21, which also presents the DC I-V characteristic at VG = 0.3 V.

3.4.3 S- parameter characterization

S-parameter characterization has been carried out by means of the Anritsu Vector Network Analyzer (VNA), shown in Figure 3. 8. The frequency range under investigation is 1-120 GHz, imposed by the custom on-wafer TRL calibration kit designed for this work. The measurements were acquired on the same bias grid as the DC I-V characteristics. Figure 3. 22 shows the measured S-parameter at a constant drain bias of 3 V and a gate bias from -0.6 V to 0.6 V in 0.1 V steps, over the frequency range from 1 GHz to 120 GHz.

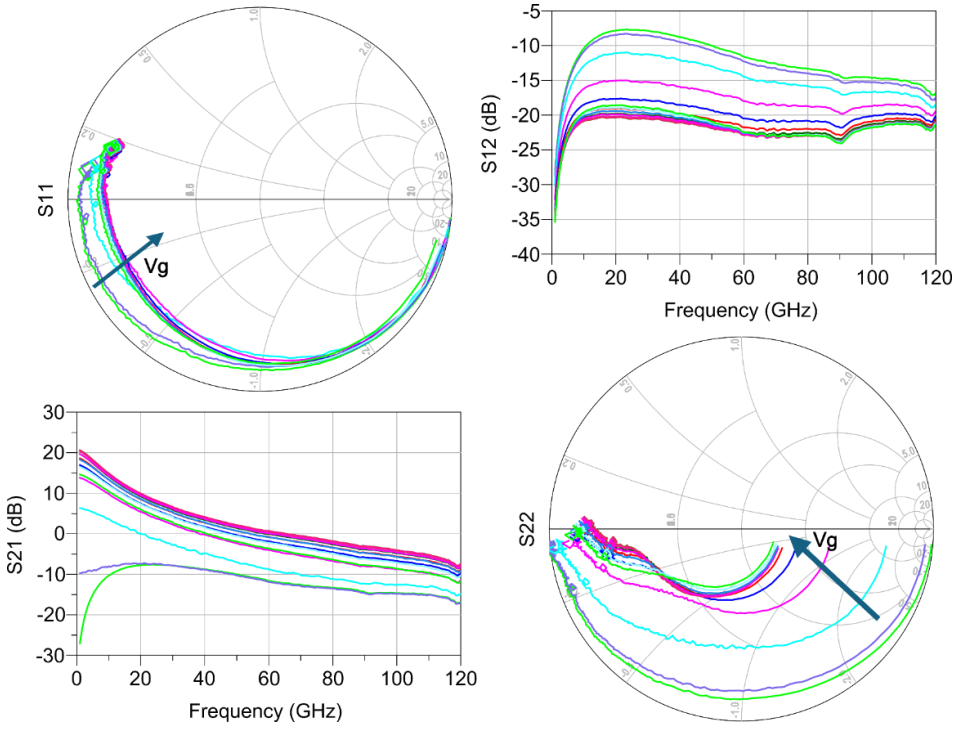

Figure 3. 22: Measured S-parameters for the 6x40-µm pHEMT from 1 GHz to 120 GHz, VG = -0.6 V ÷ 0.6 V step 0.1 V, VD=3 V.

There is also an evaluation of the temperature effect on the S-parameter, as shown in Figure 3. 23. The temperature dependence of the measured characteristics follows the expected trend: the blue curves correspond to 30 °C, while the red curves correspond to 80 °C. The observed behavior is consistent with previous results, further confirming the robustness of the technology.

The input matching exhibits negligible sensitivity to temperature variations. As evidenced by the nearly overlapping trajectories at 30 °C and 80 °C of S_{11}, the input impedance remains essentially unchanged with temperature. This is expected, as the input network is dominated by

passive elements and gate-related capacitances, which are minimally influenced by thermal effects and are not strongly affected by dispersive phenomena.

In contrast, the output side shows a clear temperature-induced shift, with the red curves deviating more noticeably from the blue ones, indicating changes in the output impedance. This behavior is consistent with the temperature dependence of channel transport parameters, such as carrier mobility and drain conductance, which directly affect S_{22} and power transfer.

The small-signal gain S_{21} systematically decreases as temperature increases, as shown by the downward shift of the red curves, due to reduced carrier mobility and increased channel resistive losses. Likewise, S_{22}exhibits a stronger temperature dependence than S_{11}confirming the higher thermal sensitivity of the output-side parameters.

Overall, these trends are physically consistent: the weak variation of S_{11}confirms stable input matching, while the temperature sensitivity of S_{21} and S_{22} reflects channel-related mechanisms, supporting the robustness of the technology over the investigated temperature range. Although mobility degradation is expected to primarily reduce S_{21}through a decrease in transconductance, the pronounced variation observed in S_{22} indicates that stress also affects the output admittance. This behavior can be attributed to a decrease of average drain current induced by device degradation, as well as changes in output conductance and in the coupling between forward and reverse transmission terms. As a result, the impact of stress is reflected not only in gain reduction but also in a slight modification of the output matching condition.

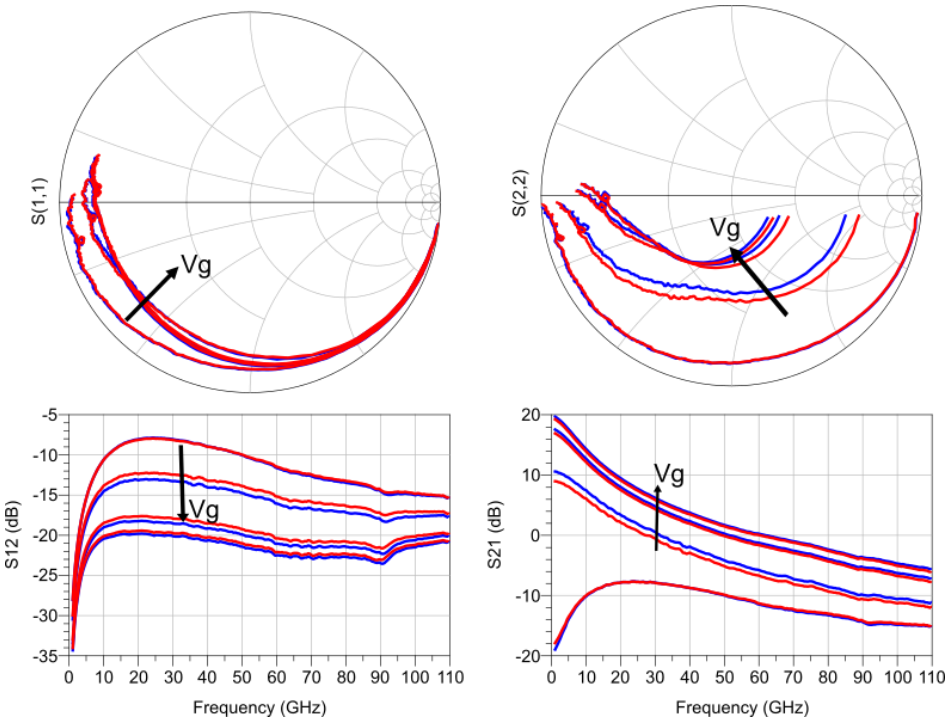

Figure 3. 23: Temperature effect on the S-parameter; the blue curves correspond to 30 °C, and the red curves correspond to 80 °C

This chapter has detailed a systematic characterization procedure for evaluating 0.1-µm GaAs pHEMTs. The methodology integrates stress testing with DC, small-signal, and large-signal low-frequency measurements, which enables a comprehensive assessment of device stability, dispersive effects, and power performance. The results indicate excellent stability under stress conditions, limited low-frequency dispersion, and competitive figures of merit in terms of gain, output power, efficiency, and cut-off frequency. Given the consistency and repeatability observed throughout the characterization campaign, it can be concluded that the investigated technology is robust and suitable for reliable millimeter-wave circuit and power amplifier design.

3.5 Device Modeling

The use of models that accurately mimic actual device behaviour is an important tool for designers. However, this remains an open issue, as conventional modeling solutions may not be suitable for new technologies. For example, low-frequency dispersion induced by device thermal and trap states causes significant degradation in device performance in new technologies.

3.5.1 Small-Signal Model

In computer-aided RF circuit design, small-signal models (SSMs) are essential for linear analysis of active devices. Accurate SSMs for microwave transistors such as MESFETs, HEMTs, and HBTs are critical not only for achieving a cost-effective and reliable amplifier design process, but also for gaining insight into device behavior through the physical significance of individual model elements [61]. Although SSM is used to analyse the nonlinear behaviour of the device by using linear equations. Therefore, the small-signal model is also called a linear model [62]. Several reviews of small-signal modelling [63] have shown that a conventional small-signal equivalent circuit is sufficient to accurately describe the small-signal behavior of HEMTs for a fixed bias. Consequently, established modeling methodologies for microwave transistors can be directly applied to GaAs pHEMT devices. The overall modeling procedure typically involves the extraction of extrinsic and intrinsic parameters, followed by model tuning and optimization. Figure 3. 24 presents the complete small-signal modeling flow for GaAs pHEMTs. This process consists of six main steps required for accurate model extraction. Figure 3. 25 shows the flow chart of a typical optimization process; the error function is defined according to the optimization goal, which is to minimize the discrepancy between the calculated and measured S-parameter values. A detailed formulation of this type of error function is presented in the following section. Extracting models directly from S-parameters provides preliminary estimates of model parameters. These initial values serve as inputs for numerical optimization routines that fit model equations to experimental time-domain waveforms. Accurate modeling of intrinsic capacitances, such as Cgs and Cgd, requires consideration of the parasitic network. S-parameter measurements facilitate the extraction of access resistances (Rs and Rd) and other reactive parasitic elements, thereby ensuring that the model is governed by the appropriate intrinsic voltages.

Figure 3. 24: Flow Chart of Small-Signal Model Extraction Procedure of GaAs pHEMT device

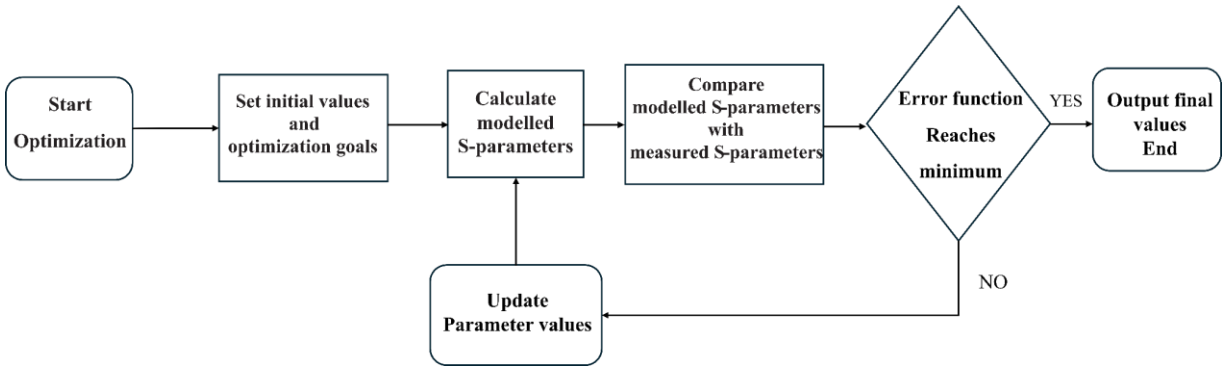

Figure 3. 25: A flow chart for the iterative optimization process[64]

The small signal or linear models of pHEMT are mainly classified into two types: physical modeling and empirical modeling. The physical model predicts the response of the transistor in small signal using its physical and structural parameters, as well as the development of an analysis of quantum electronics, which uses physical laws. This type of model is complex and requires a lot of information from the manufacturing process of the transistors, which is not always accessible[65]. To fully exploit the performance of an HEMT device in circuit design, an accurate model integrated into a circuit simulator is required. Empirical compact models offer a fast and flexible approach, providing high accuracy when properly extracted, as evidenced by the excellent agreement between measured and modeled bias-dependent DC characteristics and S-parameters.

The pHEMT small-signal equivalent circuit with the extrinsic and intrinsic parameters is shown in Figure 3. 26.

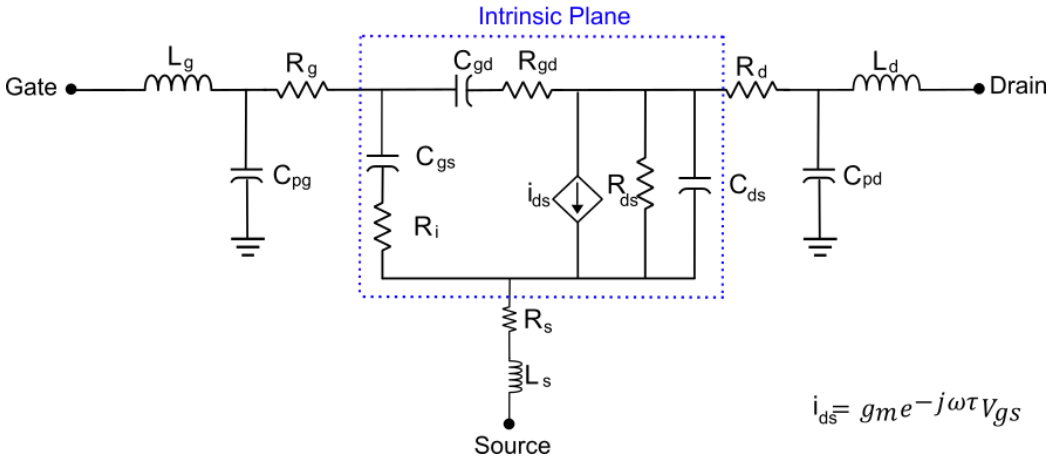

Figure 3. 26: Small-signal equivalent circuit of pHEMT

The equivalent circuit model is classified into two parts: intrinsic elements, shown within the blue dashed outline in Figure 3. 26 as g_m,C_{gd} ,C_{gs} (which includes, in fact, the drain-gate parasitic), C_{ds} , R_i , and τ (Transconductance delay) that accounts for the fact that the transconductance does not respond instantaneously to variations in the gate voltage; the charge under the gate requires a finite time to redistribute, which is a function of the biasing conditions (bias dependent), and extrinsic elements that represent the physical access structures of a device, such as pad metallization and ohmic contacts (C_{pg} ,C_{dp}, L_g, L_d, L_s, R_g, R_d and R_s) which are independent of the biasing conditions[66]. As they are bias-independent, some articles refer to them as a linear parasitic network.

3.5.1.1 Extrinsic parameters Extraction

These elements typically include resistances as R_d and R_s , contact resistances of ohmic contact, and R_g for metallization resistance of Schottky contact; inductances (L_g, L_d and L_s) for the inductive effects associated with metallization; pad capacitances (C_{pg} and C_{pd}) account for capacitive couplings between gate-source and drain-source contacts. All the effects induced by these elements must be accurately determined and "de-embedded" from measured data to isolate the intrinsic behaviour of the transistor. Extrinsic parameter extraction is typically performed using analytical methods or under cold-FET (pinch-off) conditions [67]. The most adopted approach for determining extrinsic parasitic elements is the cold-FET technique, in

which S-parameters are measured with the drain-to-source voltage set to zero and the gate biased below the pinch-off voltage ($V_{gs} \ll V_{th}$). In this condition the channel conductivity is suppressed, allowing the controlled current source I_{DS} to be neglected (the parameters $g_m$and τdo not contribute) and the intrinsic circuit reduces to a simple capacitive network as shown in Figure 3. 27. Moreover, the device becomes reciprocal, such that $S_{21} = S_{12}$ enabling the reliable analytical extraction of the remaining extrinsic elements [68]. This condition is ideal for extracting parasitic pad capacitances (C_{pg} and C_{pd}), which are typically obtained at relatively low frequencies (e.g., 1–10 GHz), where inductive and resistive effects are negligible, and, after that, extracting the parasitic inductances and resistances using a higher frequency range. This procedure considers the hypothesis that the intrinsic Cold-FET model is a π-type topology, as shown in Figure 3. 27.

The extrinsic elements can be de-embedded from measurements by applying a systematic sequence of matrix transformations, resulting in the set of equations to retrieve the intrinsic elements as reported in (3. 3) to (3. 10). In practice, the measured S-parameters are first converted into admittance parameters (Y-parameter). Within the admittance domain, the shunt (parallel) pad capacitances are de-embedded. The resulting admittance matrix is then transformed into impedance parameters (Z- parameters), which enables the removal of series parasitic resistances and inductances. The impedance matrix is subsequently converted back to admittance form to yield the intrinsic admittance matrix Y_{int}, which represents the intrinsic device behavior.

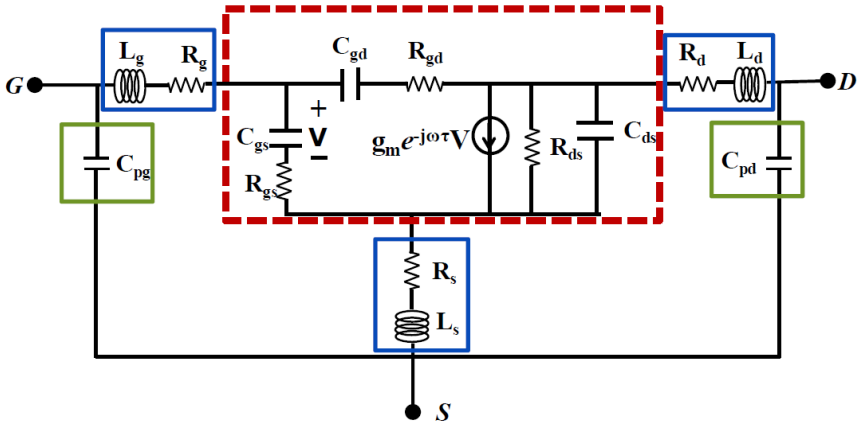

Figure 3. 27: Linear Parasitic Network Identification schematic

$$S_{measured} \Rightarrow \mathrm{Y} \tag{3. 1}$$

$$Y_{(de-C)} = \begin{bmatrix} Y_{11} - j\omega C_{pg} & Y_{12} \\ Y_{21} & Y_{11} - j\omega C_{pd} \end{bmatrix} \tag{3. 2}$$

$$Y_{(de-C)} \Rightarrow Z_{(de-C)} \tag{3. 3}$$

$$Z_{int} = \begin{bmatrix} Z_{11(de-c)} - R_g - R_s - j\omega L_S & Z_{12(de-c)} - R_S - j\omega L_S \\ Z_{21(de-c)} - R_S - j\omega L_S & Z_{22(de-c)} - R_d - j\omega L_S \end{bmatrix} \tag{3. 4}$$

$$Z_{int} \Rightarrow \mathrm{Y}_{int} \tag{3. 5}$$

3.5.1.2 Extrinsic Parasitics Extraction of GaAs pHEMT CS Topology

In this thesis, the small-signal model of GaAs pHEMT for the common-source configuration is extracted. The measurements under cold FET operation were carried out on a GaAs pHEMT (L = 0.1 μm, Z = 4 × 40 μm) in a common-source configuration. The device was biased under pinch-off, with Vg = −2 V and Vd = 0 V (Vg < Vth). Under these conditions, the intrinsic transistor is effectively turned off and can be approximated as in Figure 3. 27, allowing the measured response to be dominated by parasitic elements; this configuration is therefore used for accurate extraction of the extrinsic network parameters. To obtain the values of the extrinsic network elements, the optimizer in ADS is employed. The optimization is performed by defining error functions based on the absolute difference between the real and imaginary parts of the measured and simulated S-parameters, namely:

$$Error_{Re} = abs\ (Re(S_{ij})\_measured - Re(S_{ij})\_simulated) \tag{3. 6}$$

$$Error_{Img} = abs\ (Img(S_{ij})\_measured - Img(S_{ij})\_simulated) \tag{3. 7}$$

In Equations (3. 6) and (3. 7), i = 1, 2, and j = 1, 2. Optimum model parameters were obtained when the error function of optimization goals reached its minimum.

After completing the above steps, the extrinsic parameters are extracted together with the intrinsic capacitances in cold-FET operation. The resulting values are summarized in the Table 3. 2 below.

Extrinsic Parameters							
$C_{pd}\,(fF)$	$C_{gp}\,(fF)$	$R_g(\Omega)$	$R_d(\Omega)$	$R_s(\Omega)$	$L_g(pH)$	$L_d(pH)$	$L_s(pH)$
0	0.87	0.848	2.9	0	22.25	0	6.4

Table 3. 2: Extrinsic Parameters under cold FET operation

Under cold-FET conditions, no electrons flow between the source and drain; therefore, the controlled current generator I_{DS} can be neglected, means parameters as g_m and τ do not contribute. Moreover, the device becomes reciprocal, such that $Y_{21} = Y_{12}$, as shown by Figure 3. 28.

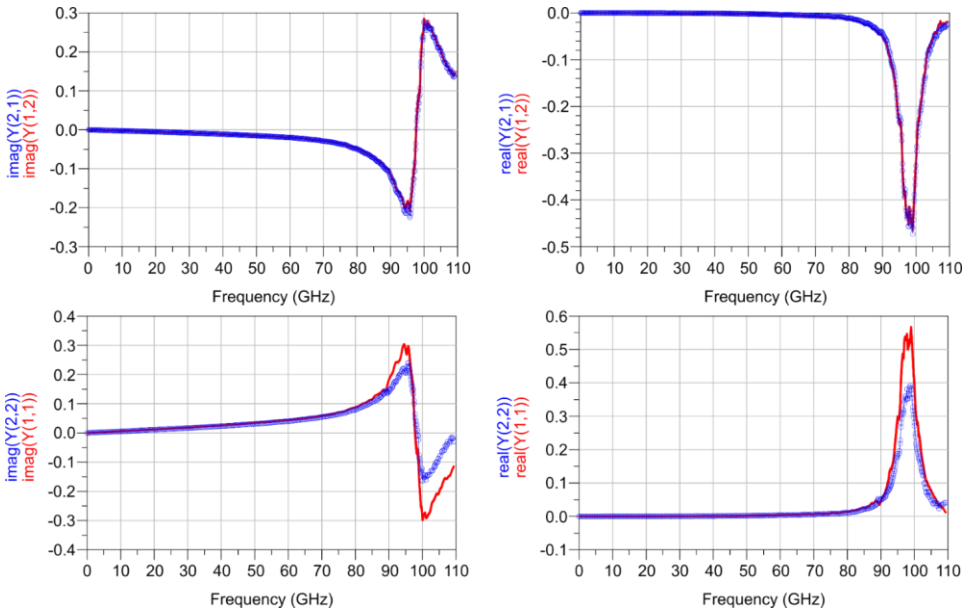

Figure 3. 28: Measured Y-parameters for the 4x40-µm pHEMT from 1 GHz to 110 GHz, under COLD FET bias condition, V_g= -2 V and V_d = 0V

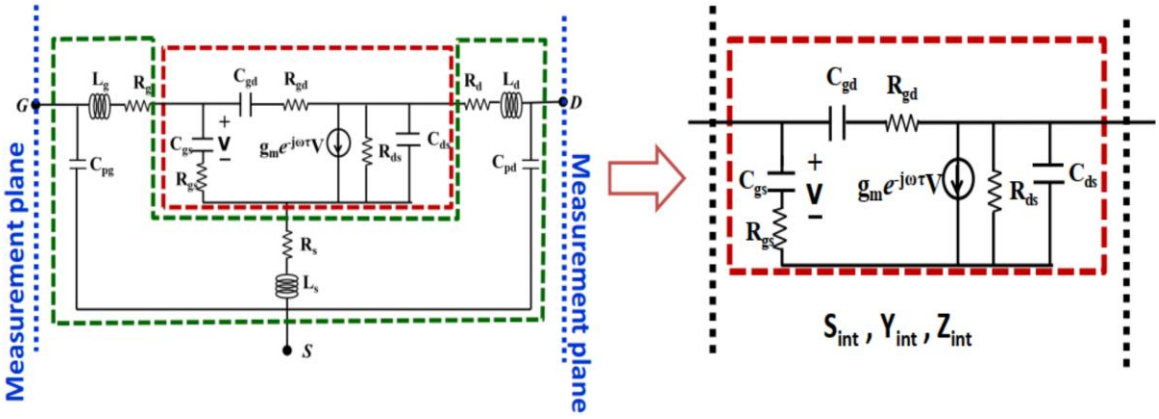

Figure 3. 29: Schematic representation of linear parasitic network de-embedding

Once the extrinsic parasitic network (EPN) has been extracted, its known linear contribution can be removed through a de-embedding procedure. Starting from the measurements referred to the extrinsic planes, and for the bias condition of interest, the reference planes are shifted from the extrinsic ports to the intrinsic device terminals, thereby enabling the extraction of the intrinsic transistor parameters under that specific operating condition. The de-embedding procedure is schematically illustrated in Figure 3. 29. After de-embedding, the device is conveniently analyzed in the admittance domain. In particular, the imaginary part of the Y-parameters are especially useful for intrinsic parameter extraction, since they are mainly associated with the reactive components of the transistor, namely the intrinsic capacitances. Because these terms exhibit a linear dependence on angular frequency, parameters such as C_{gs}, C_{gd}, and C_{ds}can be directly identified from the frequency behavior of $\mathrm{Im}(Y_{ij})$. In contrast, the real part of the Y-parameters is primarily related to the conductive contributions and are therefore used to extract parameters such as $g_m$and g_{ds}.

Figure 3. 30 and Figure 3. 31 illustrate the Y parameters before and after the de-embedding for pinch off and the Nominal bias condition (V_g= -0.1 V and V_d = 3V), respectively. The blue curves correspond to the measured device, including the contribution of the extrinsic network, while the red curves represent the intrinsic Y-parameters obtained after the de-embedding (removing the extrinsic network effect). The strong resonant features observed in the blue curves (i.e., extrinsic plane) are removed after de-embedding. The resulting intrinsic Y-parameters are smooth and physically meaningful across the frequency range. This behavior confirms the

accuracy of the extracted EPN and that the de-embedding procedure successfully shifts the reference planes to the intrinsic device.

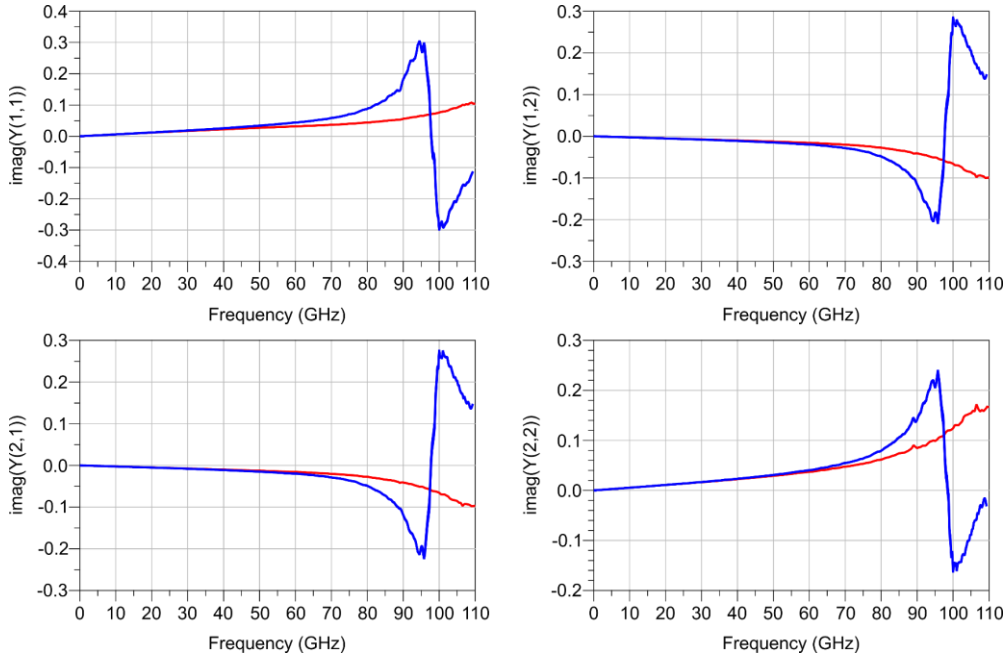

Figure 3. 30: Extrinsic vs. Intrinsic Y-parameters for the 4x40-µm pHEMT from 1 GHz to 110 GHz, under COLD FET bias condition, Vg= -2 V and Vd = 0V intrinsic is (red) and extrinsic is (blue)

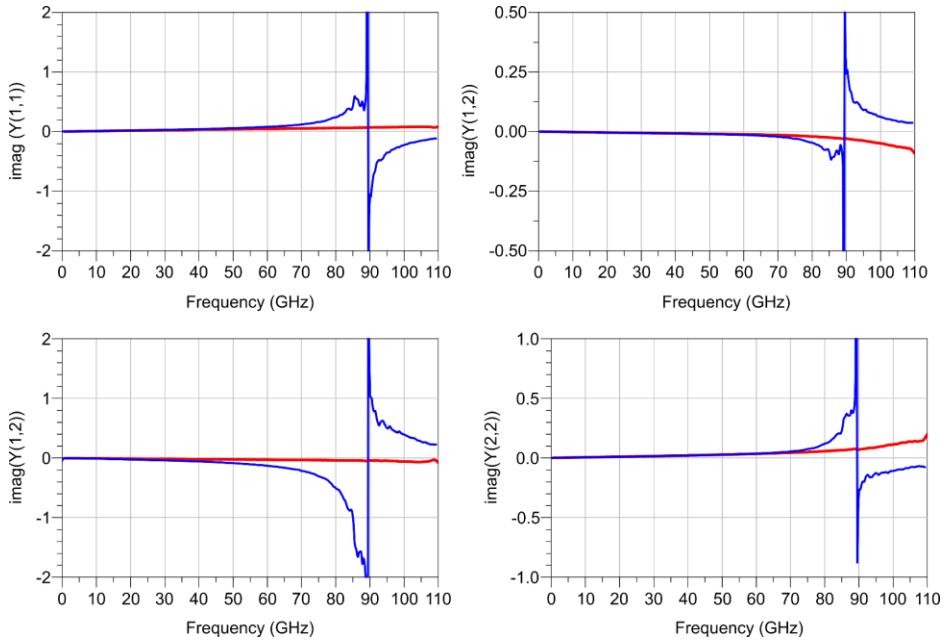

Figure 3. 31: Extrinsic vs. Intrinsic Y-parameters for the 4x40-µm pHEMT from 1 GHz to 110 GHz, under Nominal bias condition, Vg= -0.1 V and Vd = 3V intrinsic is (red) and extrinsic is (blue)

After extracting the extrinsic parameters, the next step is the extraction of the intrinsic parameters. In contrast to the extrinsic parameters, which are bias-independent, the intrinsic parameters are extracted under specific bias conditions, depending on the intended application. Figure 3. 32 shows the intrinsic parameters which are introduced previously.

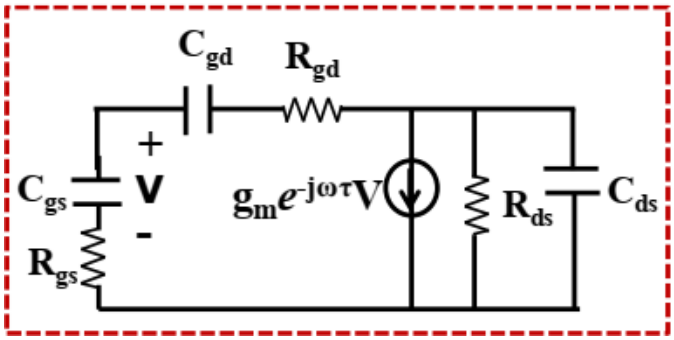

Figure 3. 32: Intrinsic network of the device

After all extrinsic parameters are extracted and de-embedded from measurements, the intrinsic parameters can be determined using the equations below. In these equations, $Y_{ij\ int}$ is the intrinsic Y parameters where i = 1, 2, and j = 1, 2.

$$R_{gd} = -Re\left(\frac{1}{Y_{12int}}\right) \quad (3.\ 8)$$

$$R_{gs} = Re\left(\frac{1}{Y_{11int} + Y_{12int}}\right) \quad (3.\ 9)$$

$$R_{ds} = \frac{1}{\mathrm{Re}(Y_{22int} + Y_{12int})} \quad (3.\ 10)$$

$$C_{gd} = \frac{1}{\omega Im\left(\frac{1}{Y_{12int}}\right)} \quad (3.\ 11)$$

$$C_{gs} = -\left(\frac{1}{\omega Im\left(\frac{1}{Y_{11int} + Y_{12int}}\right)}\right) \quad (3.\ 12)$$

$$C_{ds} = -\left(\frac{Im\left(\frac{1}{Y_{22int} + Y_{12int}}\right)}{\omega}\right) \quad (3.\ 13)$$

$$g_m = \left|\frac{(Y_{11int}+Y_{12int})(Y_{21int}-Y_{12int})}{Im(Y_{11int}+Y_{12int})}\right| \quad (3.\ 14)$$

$$\tau = -\frac{1}{\omega}\ phase\left\{(Y_{21int} - Y_{12int})\left[1 + j\frac{Re(Y_{11int}+Y_{12int})}{Im(Y_{11int}+Y_{12int})}\right]\right\} \quad (3.\ 15)$$

The bias point that is used for this extraction was $V_{GS} = 0\ V$ and $V_{DD} = 3\ V$ which corresponds to class AB operation.

Intrinsic Parameters							
$C_{gd}\ (fF)$	$C_{gs}\ (fF)$	$C_{ds}\ (fF)$	$R_{gd}(\Omega)$	$R_{gs}(\Omega)$	$R_{ds}(\Omega)$	$g_m(S)$	τ(ps)
33	100	35	0	0	104	0.115	1

Table 3. 3: Intrinsic parameter under class AB operation

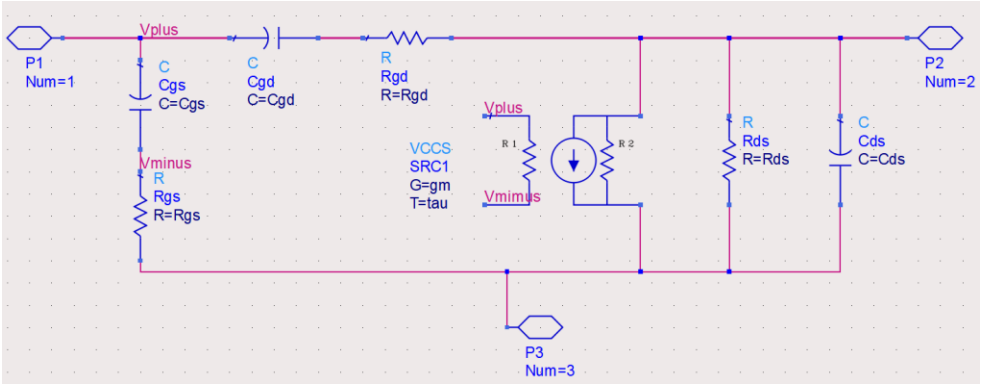

Figure 3. 33: Schematic of the intrinsic Small-Signal model of CS configuration

The results demonstrate strong agreement between measurements and simulations, which confirms the effectiveness of the proposed modeling procedure. Predictions from the three-terminal foundry model are also presented in Figure 3. 34. However, this model does not accurately reproduce the CS measurements.

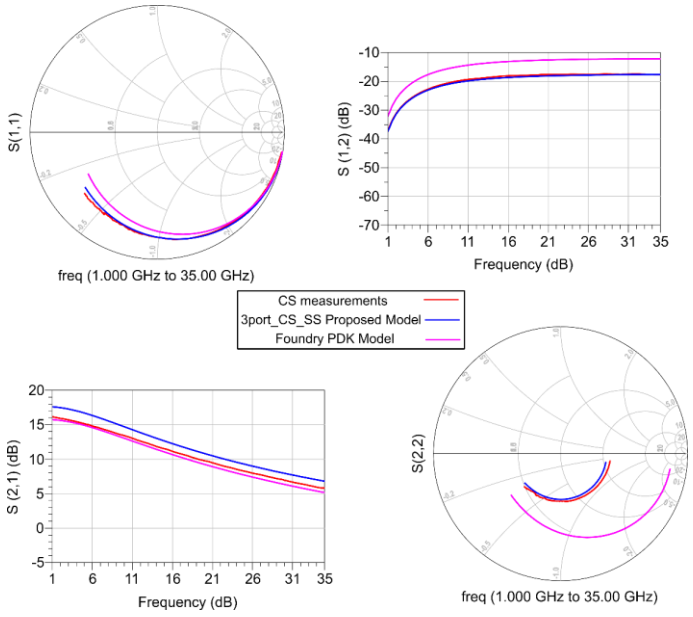

Figure 3. 34: Measured and simulated S-parameters from 1 GHz to 35 GHz at the nominal bias point for the common source configuration

3.6 Common Gate Model Extraction

The aim of this work is to design and validate a stacked-cell power amplifier architecture. In a stacked cell, a common-source (CS) stage is cascaded with one or more common-gate (CG) stages (further details are provided in Chapter 4). In practice, however, foundry process design kits (PDKs) typically do not provide a dedicated CG transistor model, and only two- or three-terminal compact models for the CS configuration are available. Consequently, CS-based models are often reused to represent CG devices, which inevitably introduces modeling inaccuracies, as they do not accurately capture the electrical behavior of a transistor operating in a common-gate configuration. Figure 3. 35 presents the micrograph and corresponding layout of the common-source (CS) and common-gate (CG) configurations, with the measurement reference plane (RP) also indicated.

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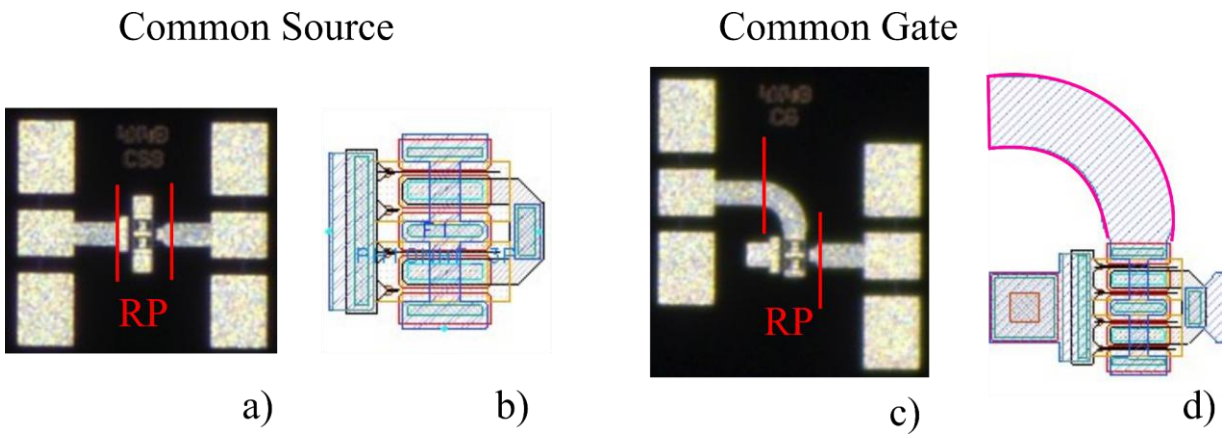

Figure 3. 35: (a) common-source and (b) common-gate configurations, (c), (d) correspondent layout

The main reason for inaccuracies in predicting CG behavior by the CS model is that, in the CS, the extrinsic parasitic network of the transistor (defined at the intrinsic gate-source and drain-source reference planes) could be very different from that of the CG. To address this issue, we propose a procedure to extract a custom model of the CG transistor starting from the small-signal model of the CS transistor (extrinsic parasitic network, intrinsic capacitances, and current generator parameters).

Afterward, we use the CS intrinsic model (which whose extraction procedure was described in the previous section) as the intrinsic model also of the CG transistor, whereas for the linear

EPN, we relied on EM simulations have been performed in the ADS Momentum environment. of the CG access structures, which were properly simulated and then connected to the intrinsic common-gate model to build the complete small-signal CG model, as shown in Figure 3. 36.

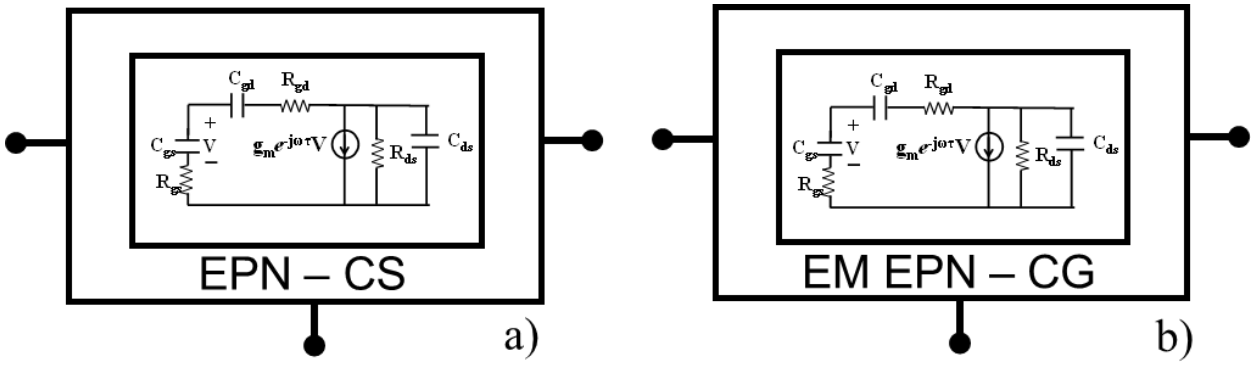

Figure 3. 36: a. CS small signal model b. CG small signal model

After that, EM simulations of the access structure of the CG, including the "half-curve" used to connect the source, which is indicated in pink in Figure 3. 35 (d), are performed up to 35 GHz. In particular, we split the access structures into three distinct sub-blocks: the gate manifold, the drain manifold, and the via–finger region. The corresponding S-parameters (i.e., snp files) resulting from the simulations were then directly used in the schematic together with the intrinsic small-signal model of the CS to build the CG small-signal model.

The comparison between measurements and simulations is shown in Figure 3. 37 . A crucial point to note regarding the measurements: port 1 of the VNA is connected to the source, and port 2 is connected to the drain of the CG transistor. This means that the S11 is the reflection coefficient looking into the source terminal.

As can be observed, a good agreement between measurements and simulations is achieved, which confirms the effectiveness of the proposed modeling procedure. The three-terminal foundry model predictions are also reported in Figure 3. 37. It is evident how such a model is not able to accurately reproduce the CG measurements. The proposed CG model is therefore adopted for the design of the stacked-cell power amplifier, which will be discussed in the next chapter.

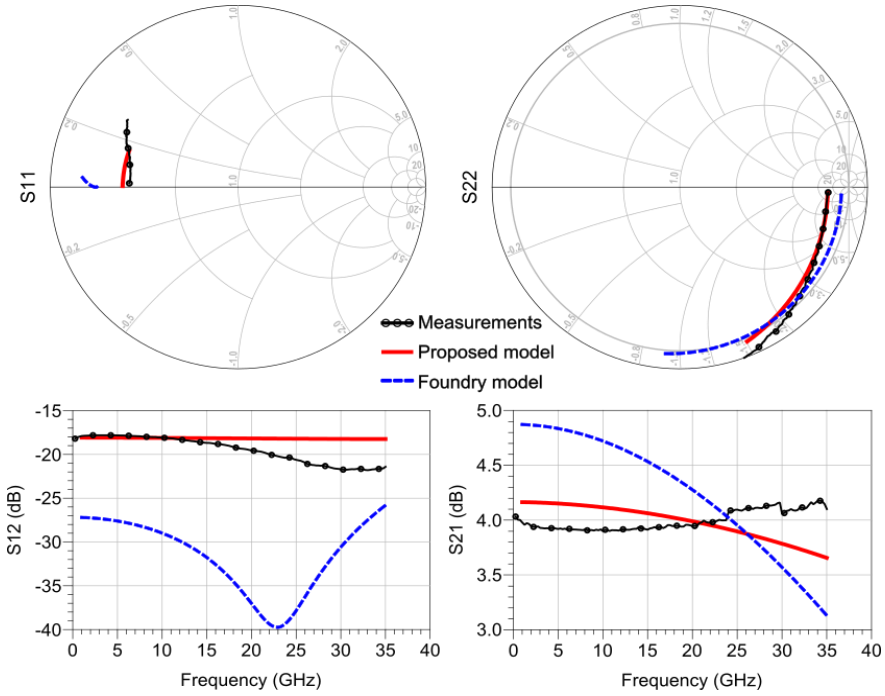

Figure 3. 37: Measured and simulated S-parameters from 1 GHz to 35 GHz at the nominal bias point for the common gate configuration

Chapter 4

Design and Implementation of Stacked Cell Power Amplifier

4.1 Introduction

Power-combining techniques are commonly adopted to overcome the output power limitations of single-transistor amplifiers. One widely used approach is the parallel combination of multiple transistors, which increases the total output current while maintaining the same drain–source voltage. Despite its effectiveness, this technique introduces several drawbacks, including lower output impedance, higher DC current consumption, and an increased influence of parasitic effects as the number of devices increases. Furthermore, parallel architectures demand higher input drive power to excite all devices simultaneously, which can negatively impact the overall efficiency.

In single-transistor amplifier design, particularly for GaAs technology, one of the main limitations is the restricted drain voltage swing, which arises from the low breakdown voltage and the relatively high knee voltage of the device [69]. These limitations directly constrain the maximum output power that a single device can deliver. A straightforward approach to increase output power would be to scale the transistor size. However, increasing the transistor size too

much is generally undesirable, as it leads to increased device parasitic effects and more complicated matching networks due to the resulting reduction in input and output impedances. As a result, simply enlarging the transistor does not represent an efficient or scalable solution.

For these reasons, power-combining techniques are commonly adopted to overcome the output power limitations of single-transistor amplifiers. One widely used approach is the parallel combination of multiple transistors, which increases the total output current while maintaining the same drain–source voltage. Despite its effectiveness. The use of parallel transistors does this by summing up the current contributions, at fixed VDS (Drain-Source voltage), but it shows some disadvantages, such as the reduction in the output impedance and the increase in DC Drain current. Moreover, in parallel, the effect of parasitic capacitances will be stronger depending on the number of devices. Finally, this solution requires increasing the input power in order to feed all the transistors.

An alternative solution is represented by the stacked amplifier [70] Figure 4.1 shows a simple N-device stacked configuration. The stacked PA architecture, first developed in silicon technologies, is now becoming a strong alternative to traditional parallel power-combining techniques in compound semiconductor platforms. This approach is gaining particular importance in GaAs technologies [71], [72], and is also extending to scaled GaN processes, where improved voltage handling and device scaling enable its practical implementation. The growing interest in stacked PAs reflects a broader shift toward architectures capable of delivering high output power without relying on very large transistors or complex multi-branch combining networks. As well compared to conventional parallel power combination, the stacked approach reduces routing losses, minimizes chip area, and eliminates the need for complex power splitters and combiners, resulting in a more compact and efficient amplifier solution.

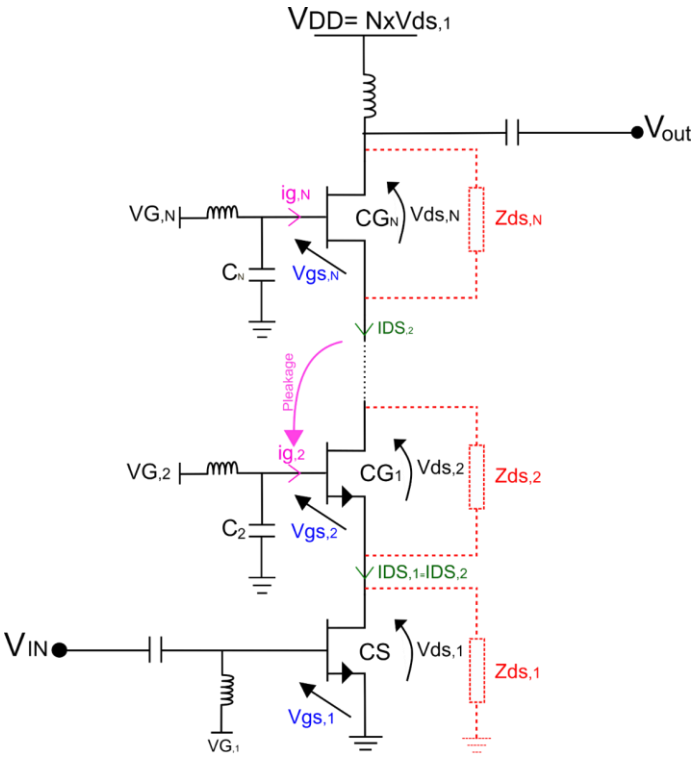

Figure 4. 1: The N-device stacked PA shows the device matching condition highlighted in red with a dashed line

The stacked PA is composed of two basic stages: a CS stage (the first stage) and (N − 1) pseudo-CG stages. The latter differs from a standard CG configuration in the role of the gate capacitance ($C_{g,n}$) which does not simply provide a short circuit at the operating frequency, as in cascode PAs; instead, it plays a crucial role in the inter-stage device matching; the details about $C_{g,n}$ will be discussed in the following section. The biasing network, including voltage and current distribution among the stacked devices, will also be discussed in detail in the following section.

As shown in Figure 4. 2 the CG stage is modelled using a simplified equivalent intrinsic circuit that neglects all parasitic elements except C_{gs}. This forms a capacitive voltage divider with the intrinsic input capacitance, allowing for device inter-stage matching and voltage waveform alignment.

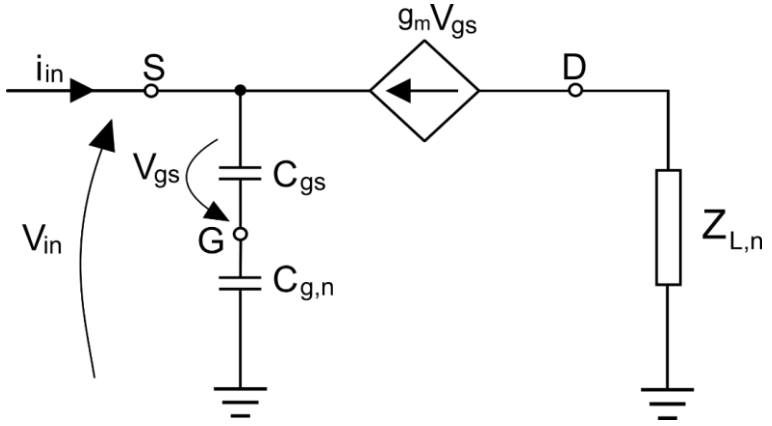

Figure 4. 2: Simplified intrinsic equivalent of the nth CG stage[73]

Maximum output power is achieved when the load seen by each nth transistor between its drain and source terminals equals its optimum value ($Z_{ds,n}$= Z_{opt}). Equivalently, the output load from drain to ground is $Z_{L,n}$= $Z_{in,(n+1)}$= N× Z_{opt}. The input and drain-source impedances of each nth common-gate (CG) stage are determined by the external gate capacitance ($C_{g,n}$) as described by the equations below [73].

$$Y_{in,CGn} = \frac{1}{Z_{in,CGn}} = \frac{i_{in}}{V_{in}} = \frac{g_m}{A_n} + j\omega\frac{C_{gs}}{A_n} \tag{4.1}$$

$$Z_{ds,CGn} = \frac{v_{ds}}{i_{ds}} = Z_{L,n} - \frac{A_n}{g_m} \tag{4.2}$$

$$A_n = (1 + \frac{C_{gs}}{C_{g,n}}) \tag{4.3}$$

Note that $Z_{ds,CGn}$ remains independent from the impedance connected at the source terminal. In contrast, $Z_{in,CGn}$ does not depend on the output load $Z_{L,n}$ in the simplified circuit; however, when additional parasitic elements are considered, $Z_{in,CGn}$ becomes dependent on $Z_{L,n}$ because the transistor is no longer unilateral. To provide maximum output power, the device must be loaded at the intrinsic drain-source plane by the optimum load (R_{opt}) that simultaneously maximizes voltage and current swings. By posing $Z_{ds,n}$ = R_{opt} and $Z_{L,n}$ = nR_{opt}, we obtain $C_{g,n}$.

$$C_{g,n} = \frac{C_{gs}}{(n-1)g_m R_{opt} - 1} \tag{4. 4}$$

That is the classical design equation of the stacked PA [70]. From (4. 1), we can note that this value of $C_{g,n}$ also provides matching for the real part of $Y_{in,CGn}$ in (4. 5)

$$Re(Y_{in,CGn}) = \frac{g_m}{A_n} \tag{4. 5}$$

In addition, a non-zero imaginary term arises, which is directly proportional to the operating frequency f.

$$Y_{in,CGn} = \frac{1}{(n-1)R_{opt}}\left(1 + j\omega\ \frac{C_{gs}}{g_m}\right) \approx\ \frac{1}{(n-1)R_{opt}}(1 + j\frac{f}{f_T}) \tag{4. 6}$$

The device cut-off frequency is approximated as $f_T \approx \frac{g_m}{2\pi C_{gs}}$. By inserting Equation (4.6) into Equation (4.2) we obtain:

$$Z_{ds,n} = Z_{L,n+1} - (n-1)R_{opt} =\ R_{opt}(1 - n\frac{1 + j\frac{f}{f_T}}{1 + j\frac{f^2}{f_T^2}}) \tag{4. 7}$$

For a constant operating frequency, the mismatch caused by C_{gs} is dependent on n and becomes progressively more significant along the stacked configuration. Additionally, a non-zero imaginary component in the load $Z_{ds,n}$ results in phase misalignment between current and voltage, which restricts the maximum current swing and consequently reduces the maximum achievable power.

At very high frequencies, the contribution of the device output capacitance becomes non-negligible and typically requires inductive compensation [74]. In addition, the combined effects of parasitic elements and phase rotation along the interconnection lines lead to waveform misalignment between stages. As a result, an additional inter-stage matching network is required to achieve proper impedance matching, compensate for phase mismatch, and guarantee correct operation of the stacked devices. For inter stage matching network design, two different approaches are possible: a theoretical approach, where the analysis of the structure is carried out considering parasitic elements in order to find adequate design guidelines, as in [74], [75], [76]or

a load-pull approach, where the complex optimum extrinsic load (Z_{opt}), from load-pull simulations, is adopted for the design.

In the theoretical inter-stage matching network design approach, accurate knowledge of device parasitic elements is required, typically obtained through simulations or measurements[77]. To simplify, assumptions are often introduced, such as neglecting some parasitic elements (e.g., inductive components) and, more critically, ignoring their nonlinear dependence on input power, particularly nonlinear capacitances. As a result, this approach remains approximate and typically requires optimization based on using nonlinear device models.

In contrast, the load-pull-based approach directly exploits the nonlinear device models, inherently accounting for both linear parasitic elements and nonlinear effects, with a level of accuracy that depends only on the model itself. Since accounting for parasitic effects at high frequencies is not feasible, the load-pull method is employed in this study.

4.2 Gate Power Leakage and Maximum Number of Stacked Transistors

As depicted in Figure 4. 1, the $C_{g,n}$ indicates that a portion of the output signal of the preceding stage is diverted to the gate of the subsequent one in order to drive it. This behavior is widely known as gate leakage or gate power leakage, since it degrades the effectiveness of the power combination in the fundamental stacked PA structure [78].

Since $i_{d,n} = i_{s,n} - i_{g,n}$, the current gain of the n^{th} CG stage can be expressed as

$$\beta_{CS} = \frac{|i_{d,1}|}{|i_{s,1}|} = \frac{g_m V_{gs}}{2\pi C_{gs} V_{gs}} = \frac{f_T}{f} \tag{4. 8}$$

$$\beta_{CG,n} = \frac{|i_{d,n}|}{|i_{s,n}|} = \frac{1}{1 + \frac{|i_{g,n}|}{|i_{d,n}|}} = \frac{1}{1 + \frac{1}{\beta_{CS}}} = \frac{f_T}{f_T + f} \tag{4. 9}$$

Consequently, every CG stage added to the stack contributes to a loss in the overall current gain, which directly limits the achievable output power.

The number of stages (N) determines the overall achievable output power, as given in Equation (4. 10), where $P_{out,CS}$ is the power (in Watt) delivered by the transistor cell in CS configuration.

$$P_{out} = N\, V_{DS,1} \,.\, \beta_{CG,n}^{(N-1)} I_{D,1} = \; N \;\beta_{CG,n}^{(N-1)}\, P_{out,CS} \qquad (4.\ 10)$$

For a specified operating frequency f, the maximum number of devices that can be stacked is determined by substituting Equation (4. 9) into Equation (4. 10) as shown in Equation (4. 11) [73].

$$N_{max} = \left[\frac{1}{\ln\left(1 + \frac{f}{f_T}\right)} \right] \qquad (4.\ 11)$$

Equation (4. 11) has been proposed in [79] with reference to Voltage-Controlled Oscillators (VCOs) based on stacked FETs and has then been applied to the case of PAs as well [80].

With the technology used in this thesis (i.e. 0.1 μm GaAs), at 27 GHz, it is possible to stack maximum 3 devices; However, in this work, only two devices are adopted due to practical limitations. In particular, stability concerns, impedance-matching challenges, and potential degradation in gain and efficiency must be carefully considered. Moreover, the maximum achievable output power may also be reduced, especially when wideband operation is targeted. Therefore, the designed stacked cell consists of CS stage and one CG stage, and its drain bias voltage (V_{DD}) and optimum output termination (under the assumption of ideal series combination) are twice those of the CS stage alone (Z_{opt}). The motivation of limiting the number of CG cells is also to obtain an "elementary cell" that can be used as "brick" in more complicated power amplifiers architectures.

4.3 DC Bias Point

Figure 4. 1 illustrates an N-device stacked power amplifier (PA), in which the gate–source bias voltages of all transistors, $V_{GS1}, V_{GS2}, \ldots, V_{GSN}$, are identical. Although the drain–source voltage of each individual device remains essentially unchanged to avoid breakdown, the total achievable drain–source voltage can be significantly increased, reaching $N \times V_{DS1}$, where N is the number of stacked transistors. As a result, the output power increases proportionally with N [73]. Furthermore, it can be shown that the DC characteristics of an ideal stacked amplifier are equivalent to those of a single-transistor stage, with the drain voltage simply scaled by a factor of N . Under these conditions, each transistor in the stack can deliver its maximum output power, leading to a proportional increase in both the total output power and gain. Each stage of the stacked PA is characterized by identical electrical quantities, including V_{DS} , V_{GS} , and the corresponding drain current. Consequently, all stages are designed to operate at the same quiescent bias point, ensuring the generation of in-phase V_{DS}voltage swings.

Since the stages share the same DC current, each transistor should have the same V_{GS}. In order to satisfy this requirement, the corresponding gate voltage for the CS stage is $V_{G1} = V_{GS1}$ then, in order to obtain the same voltage drop, the gate voltage of the i[th] CG stage must be set to [80].

$$V_{G,i} = V_{DD}^{(i-1)} + V_{GS}^{i} = \frac{V_{DD}}{n}(i-1) + V_{GS1} \qquad (4.\ 12)$$

where n corresponds to the total number of stacked stages, and i indicates the actual stage.

The gate bias voltage can be supplied externally at the required level, although this approach needs an appropriate feed network for each device. A more efficient alternative, known as self-bias, will be discussed in the following section.

Figure 4. 3 presents the DC characteristics of the selected 4 × 40 µm GaAs device in a common-source (CS) configuration. The IDS versus VGS plot at VDS = 3 V indicates that the maximum current reaches 85 mA. To achieve high efficiency at saturation while maintaining very low power dissipation in the absence of RF input, the bias point is set to Class AB. The quiescent current is 15 mA, with a corresponding gate-source voltage of -0.15 V, as indicated in the IDS vs VGS characteristic.

According to the theory of FET stacking [69] a key design concern is ensuring equal distribution of both RF and DC voltages among the FETs[81]. Gate bias voltages are set to keep DC drain-source voltages nearly equal. The drain of the second stage (CG) is biased at VDD = 6V, while $V_{DS,1}$ = 3 V, and the gate bias for the CG stage is determined by Equation (4.12); they are less than their respective breakdown voltages. Gate bias voltages are set to keep DC drain-source voltages nearly equal.

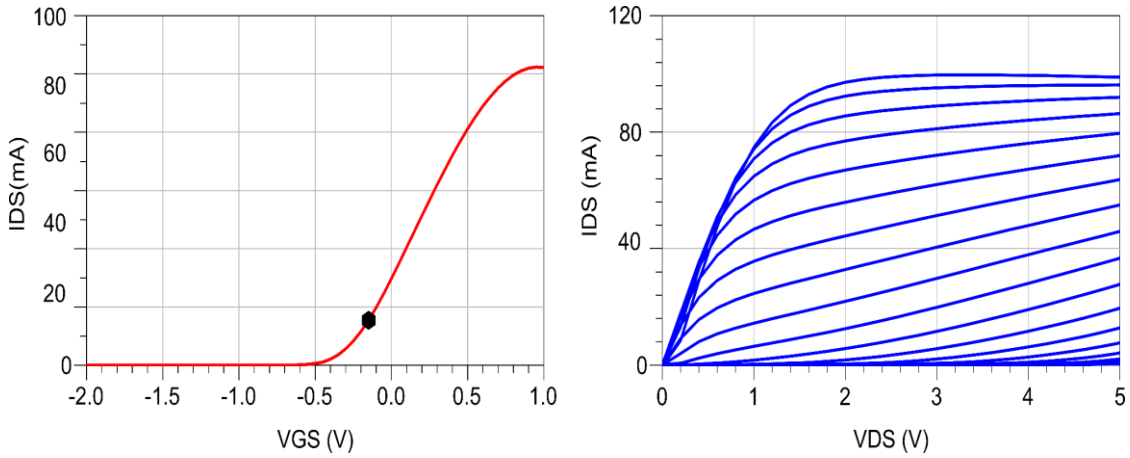

Figure 4. 3: On the left is the CS stage, IDS vs VGS, and on the right, IDS vs VGS simulated characteristics

4. 4 Small-Signal Analysis

The S-parameter simulation results up to 100 GHz are shown in Figure 4. 4. The red curve corresponds to the naked CS configuration, and the blue dashed line shows results after employing the stability network (SN). From the red plot of Figure 4. 4 it is evident that the device exhibits potential instability at the operating frequency, as the two-port stability criterion based on the Rollet factor is not satisfied, K≤1 @ 27 GHz. Moreover, the same plot indicates that the device is inherently unstable also at higher frequencies up to 62 GHz.

Stabilization is required not only at the operating frequency but also outside the band of interest. In particular, the device must be stabilized at low frequencies, from DC up to the design bandwidth, to avoid out-of-band oscillations. In this frequency range, the load conditions are uncontrolled; in this condition, the FET has a high gain and is potentially unstable. To stabilize the CS stage, a dissipative network including a resistive element is introduced. Some other

reactive elements allow a series resistor bypass, so the gain is reduced only below the band of interest.

At the operating frequency, the maximum available gain (MAG) should remain as close as possible to its original value within the stable region, since any gain degradation is undesirable. For this reason, the stabilization network (SN) is designed to enforce unconditional stability across the entire frequency range, with particular emphasis on low-frequency behavior, while minimizing in-band performance degradation.

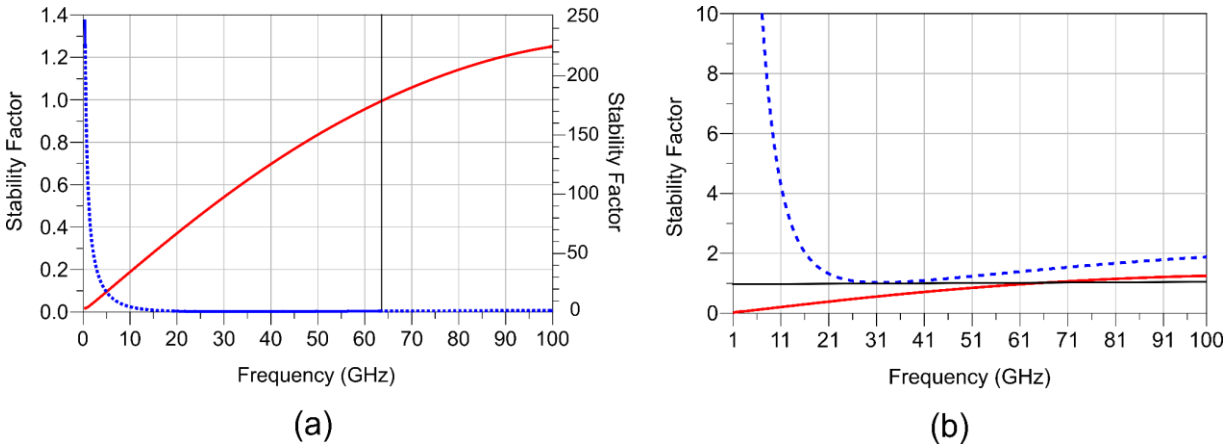

Figure 4. 4: Stability (K) factor vs Frequency for the common-source (CS) stage 4 × 40 µm device size: (a) Full-scale frequency response of stability factor. (b) Zoomed-in view of the stability factor

Various stability network (SN) topologies were designed and evaluated with the aim of preserving the maximum gain (MAXG) as much as possible within the desired frequency band, as shown in Figure 4. 5. The effect of stability network design on the maximum gain over frequency is illustrated in Figure 4. 6.

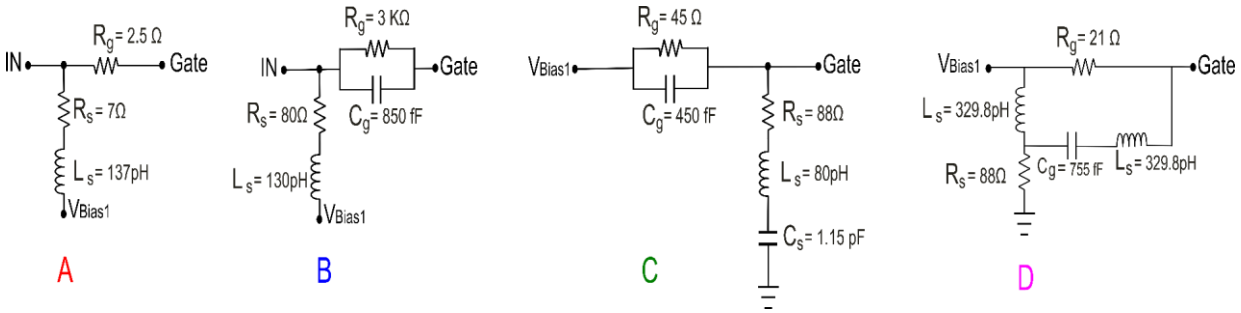

Figure 4. 5: Different Stability Network topologies

Figure 4. 5 A and B correspond to the red and blue curves in Figure 4. 5, respectively, and illustrate bias subcircuits in which the stability network (SN) is embedded to reduce circuit complexity and chip area. While C and D correspond to the green and pink curves in Figure 4. 6, respectively in these SN and require an additional bias network for the gate bias which is called (V_{Bias1}). All of these parameters are manually swept in order to have stability factor ($K \geq 1$) and to maximize the MAG.

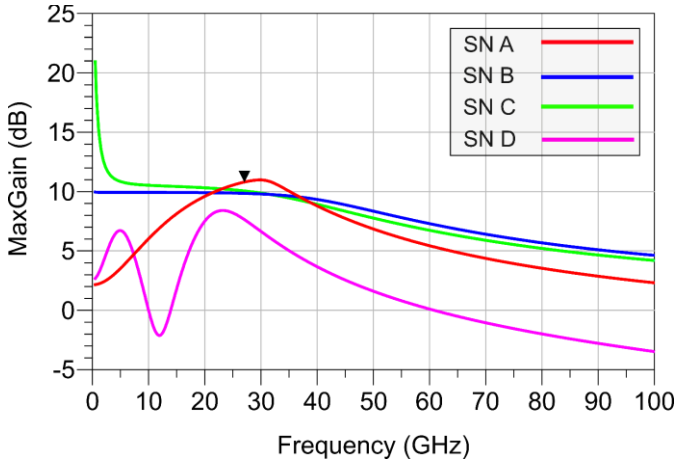

Figure 4. 6: MAXGain vs Frequency for different stability Network shown in Figure 4.5

In Figure 4. 6 shows that the red curve illustrates how the use of subcircuit A (from Figure 4. 5) maintains maximum gain within the target frequency band and suppresses gain outside this range. Suppressing out-of-band gain directly enhances unconditional stability. Complete stabilization from DC to 27 GHz results in significant gain degradation.

4. 5 Load Pull Analysis

In the following, a load-pull analysis is performed on the selected device.

To do that, all possible loads (within a given range) are simulated by sweeping both the real and imaginary parts of the load and identifying the 1 dB gain compression point. At this operating point, the main performance metrics (P_{out}, Gain, and PAE) are computed, and corresponding contours are evaluated.

Figure 4. 7 presents load-pull simulation results for the 4 × 40 µm device at 27 GHz, under the selected bias point corresponding to VD = 3 V and VG = -0.15 V. Considering the high operating frequency and the stacked architecture, implementing a tuned-load or harmonic-tuning approach is not feasible. As a result, the load-pull analysis is performed assuming a constant load at all harmonic frequencies. Different optimal load impedances can be identified depending on whether maximum output power, gain, or PAE is targeted. As shown in Figure 4. 7, the gain and the Pout are maximized by approximately the same load, while it is quite different in the PAE case. Thus, the adopted load is $Z_{opt,CS}$= (24.7 + j23.1) Ω, selected to have a good trade-off among all the performance parameters.

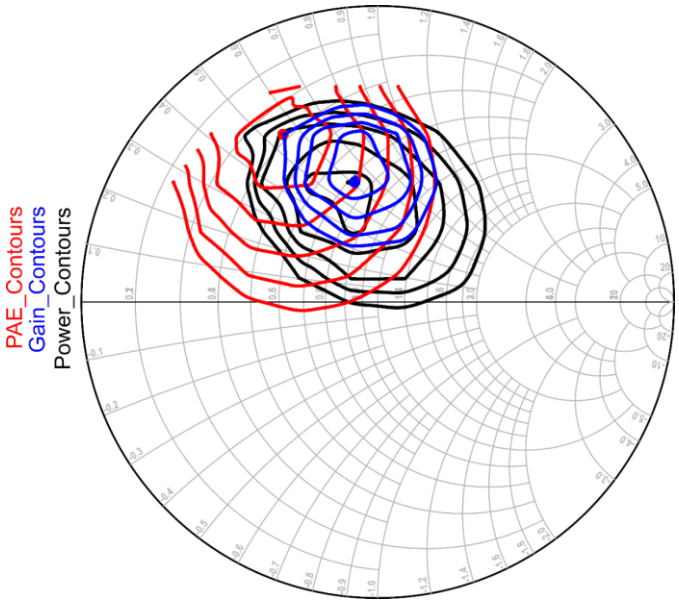

Figure 4. 7: Output power (black), Gain (blue) and PAE (red) load-pull contours at 1dB Gain Compression Point simulated at 27 GHz on the 4x40-µm device

The simulation results of the large-signal continuous-wave (CW) Harmonic Balance (HB) simulation with power sweep under the selected optimal load are presented in Figure 4. 8. The maximum PAE is 37 %, the saturated output power is 17 dBm, while the associated gain is 9.4 dB.

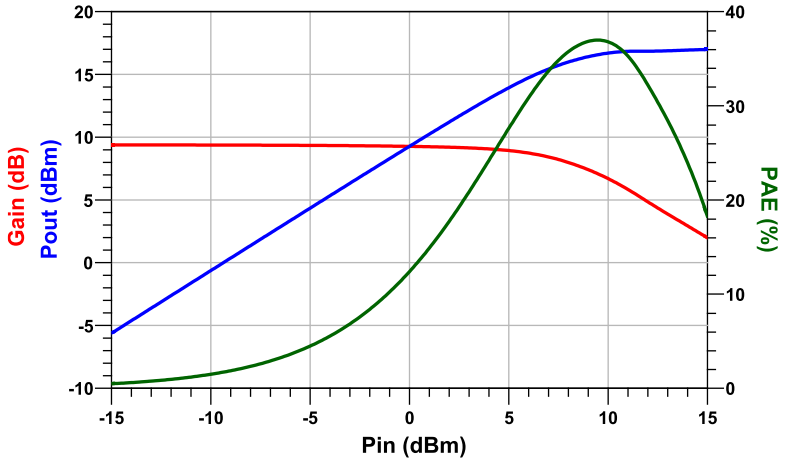

Figure 4. 8: HB simulation with power sweep and with the selected optimum load for 4x40-µm for 4x40-µm CS configuration at 27 GHz: output power (blue), power gain (red), PAE (green)

4.6 Two-Stage Stacked Amplifier

As discussed in previous sections, the stacked PA requires biasing so that both stages operate at an identical operating point. Consequently, a supply voltage of VDD = 6 V is applied to achieve a drain–source voltage of $V_{DS,1}$ = 3 V for each device.

Once the supply voltage is established, the gate voltage must be applied, and the bias networks for both common-source (CS) and common-gate (CG) transistors should be designed, as previously discussed. The bias network for the CS configuration is integrated with the stability network; therefore, only the CG bias network remains to be designed. To provide the appropriate biasing voltage to the CG transistor, there are two main options:

• Use an independent biasing network for each Gate terminal, requiring three separate voltages supplied externally, one for the drain and two for the gates (voltages to be provided externally)

• Use a single DC pad for CG, VDD = 6 V, reduced through voltage dividers to the required values.

The first method is not considered because it requires an additional voltage source and a separate DC pad.

The second method, illustrated in Figure 4. 9, is adopted in this work.

A resistive voltage divider is used to supply the DC bias for the CG transistor, requiring the addition of two resistors. This configuration enables imposing VG2 = 2.85 V, given $V_{DS,1}$ = 3 V and VDD = 6 V.

An initial assumption of R2 = 1 kΩ is made, and R2 is subsequently calculated using the voltage division principle between two resistors, resulting in R2 = 1.108 kΩ. Current flowing in the bias network remains negligible compared to the drain current.

For simplicity, in design, the n-th stage is given by $Z_{opt,n}$ = N × $Z_{opt,CS}$[80] corresponding to the theoretical optimum when both devices are individually perfectly matched [73]. Consequently, the optimum load for the overall stacked PA is $(48 + j27)$ Ω. However, after terminating the common-gate (CG) stage with this impedance, a further load optimization is performed to achieve optimal overall performance. Because $Z_{opt,n}$ = N × $Z_{opt,CS}$ is only a first-order theoretical assumption. In the real stacked cell, parasitics, the finite CG gate impedance, and CS–CG interaction change the effective load seen by each device. Consequently, after applying the theoretical load, further re-optimization is required

Moreover, the CS device should be matched to $Z_{opt,CS}$, found from the load-pull simulations.

The custom model is used for the common-gate stage to have an accurate assumption of the parasitic elements.

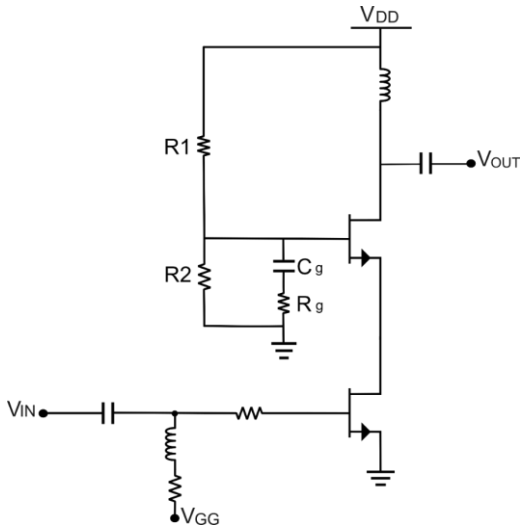

Figure 4. 9: Stacked cell with resistive self-bias

As the CS stage load is represented by the input impedance of the CG, to obtain $Z_{opt,CS}$ must provide the proper value of the gate capacitance C_g.

4.6.1 Cg evaluation

The gate capacitance (Cg) value is selected to present a finite impedance at the gate, allowing an appropriate amount of RF voltage swing. Because the gate voltage is in phase with the drain voltage, the maximum drain-gate voltage swing is reduced to maintain reliable operation and prevent drain-gate voltage breakdown.

In addition, due to the high drain voltage, the gate loading of the CG transistor must be carefully designed to guarantee a balanced voltage swing between the drain and source terminals. The gate capacitance, therefore, plays a key role in shaping the voltage distribution across the device.

At frequencies well below the cut-off, the optimum load is purely real, and the CG input reactance due to C_{gs} is low. In this range, the gate capacitance C_g is sufficient for inter-stage matching. At higher frequencies, Z_{opt} becomes complex, and additional matching elements may be required. Consequently, the C_g value is optimized by simulation, hence taking into account all the parasitic effects, aiming at guaranteeing the best possible inter-stage matching, i.e., providing both the CS and the CG stages with a load impedance close to the optimum value, as shown in Figure 4. 10 (C_g = 145 fF). In this figure, the drain–source impedances of both the CS and CG devices are shown as the input power is swept from −15 dBm to 15 dBm.

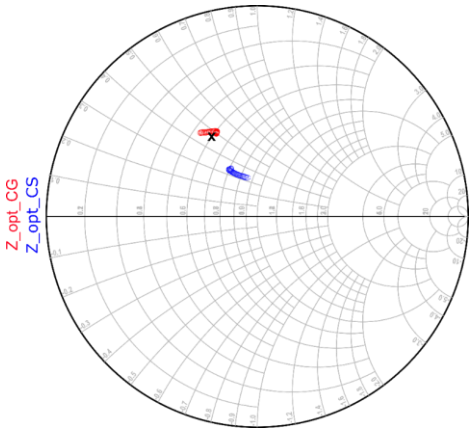

Figure 4. 10: Loads of the CS (blue circles) and CG (red circles) stages compared to the CS optimum load (black cross)

In Figure 4. 10 the black cross is ZoptCS, while the red and blue circles are CG and CS loads with power sweep, respectively.

4.6.2 Performance of two-stage stacked amplifier

When the stacked cell is terminated with the optimum load, as illustrated in Figure 4. 11. is achieved, a saturated output power of 19.6 dBm, a power gain above 12 dB, and a maximum power-added efficiency (PAE) of 41.3% at the schematic level. The observed increases in output power and gain with respect to the single CS device are close to the theoretical value of 3 dB, confirming the effectiveness of the device-stacking approach.

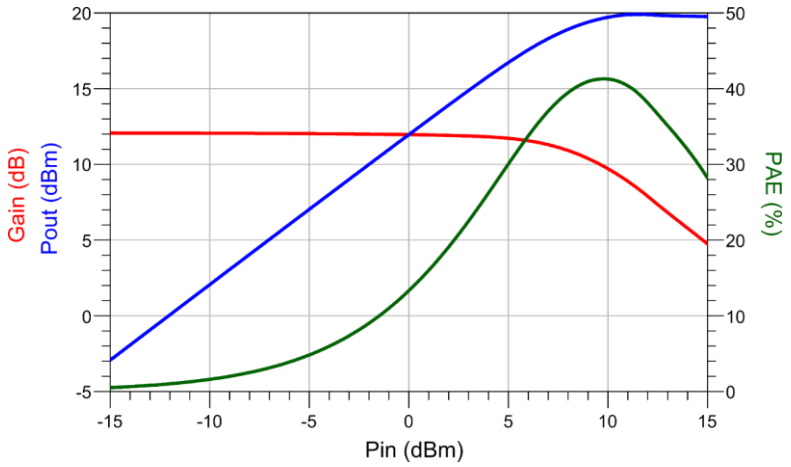

Figure 4. 11: HB simulation at 27 GHz of the 2-stage stacked cell at 27 GHz: output power (blue), power gain (red), PAE (green)

The S parameter vs Frequency of the stacked cell when terminated with the ideal optimum load is shown in Figure 4. 11.

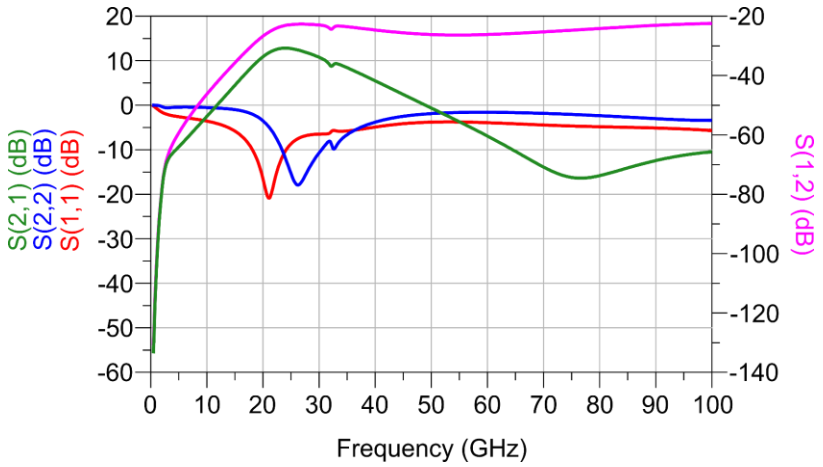

Figure 4. 12: S-parameter vs Frequency for Stacked cell

4.6.2 Implementation and Layout Constraints

To draw the layout of the Stacked PA, it is first necessary to replace ideal components with components provided by the foundry PDK, which are physically achievable within this technological process (UMS). Obviously, since the devices are now real, they will not show ideal behavior; for example, the measured impedance of capacitors will have a real part, and they will exhibit inductive effects. It is worth noting that all the simulations in the previous sections were performed using PDK elements (real components).

Each technology is subject to a well-defined set of layout design rules that must be rigorously adhered to; any deviation necessitates formal authorization from the foundry (e.g., UMS). These constraints are specified within the process design kit (PDK), and a comprehensive treatment lies beyond the scope of this chapter.

At millimeter-wave frequencies, the transformation of the schematic into a highly compact and performance-optimized physical layout, followed by thorough electromagnetic (EM) refinement, constitutes a critical phase of the design methodology.

To improve modeling accuracy and ensure reliable performance prediction, EM simulations using Keysight ADS Momentum are conducted on critical layout regions. This enables the extraction of layout-dependent parasitic effects, which are not captured in conventional schematic-level analyses.

The first and most important one is the interconnection between the two transistors, as shown in Figure 4. 13 by white arrow, the complete layout of the stacked cell, including the matching networks and input and output pads.

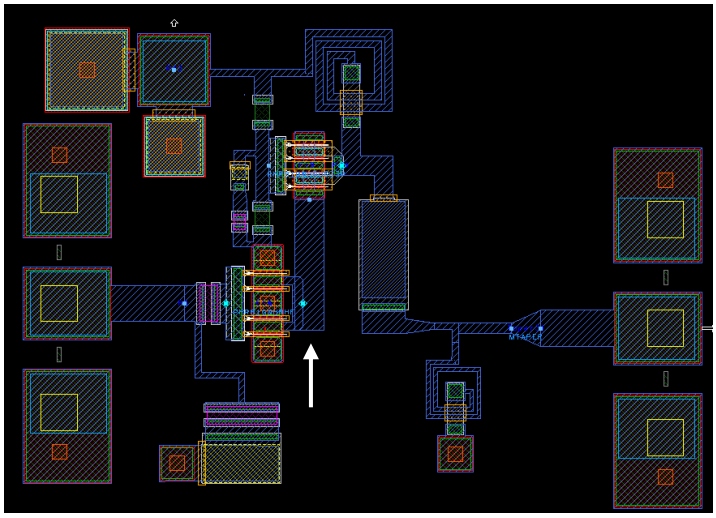

Figure 4. 13: 2-stage Stacked-Cell Amplifier Layout including matching and biasing networks

Figure 4. 13 illustrates that the two transistors are connected by a rectangular interconnection. The parasitic effects introduced by this interconnection meet our needs in terms of an interstage matching network, and incorporating the effects of this interconnection into the stacked-cell schematic, it could approximately match the impedance that is needed for interstage matching.

Subsequently, the stability network introduced in the previous section must account for inductive parasitic elements, as it requires a specific inductor value. After conducting several trials with a foundry inductor, the structure presented in Figure 4. 14 was selected as a stability network.

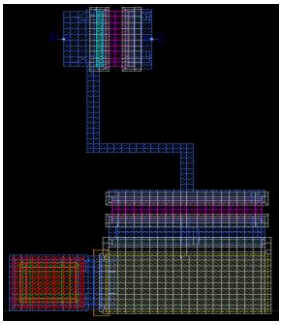

Figure 4. 14: Stability Network layout

Following that, we also need to design a proper output matching network. It is important to note that, although S-parameters are frequently reported in the literature, the impedance required for power matching in a power amplifier often differs from the small-signal matched impedance. As a result, the impedance that maximizes conjugate matching based on S-parameters does not generally coincide with the optimum load impedance required for optimum power. In a power amplifier, the optimum load is instead determined by large-signal behavior and is typically extracted through load-pull analysis, as described in the previous section. For this reason, in this work, a compromise between power matching and small-signal matching is adopted. Figure 4. 15 presents the layout of the designed matching network. The metal connection between the capacitor and the DC feed (inductor) was one bottleneck in this matching network design. The size and shape of this connection substantially influence the characteristics of the matching network as well as the bandwidth.

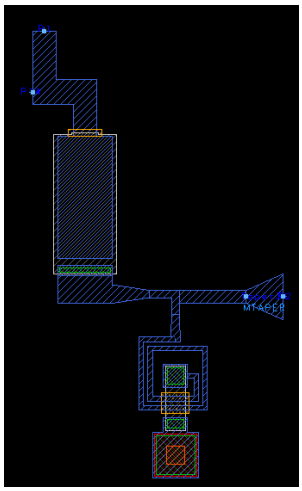

Figure 4. 15: Layout of Output Matching Network

Figure 4. 16 shows the output power performance versus frequency obtained from EM-based simulations, from which it can be inferred that the adopted stacked cell matching network provides a bandwidth of 7.3 GHz, defined by a 0.5 dB drop in output power over the frequency rang.

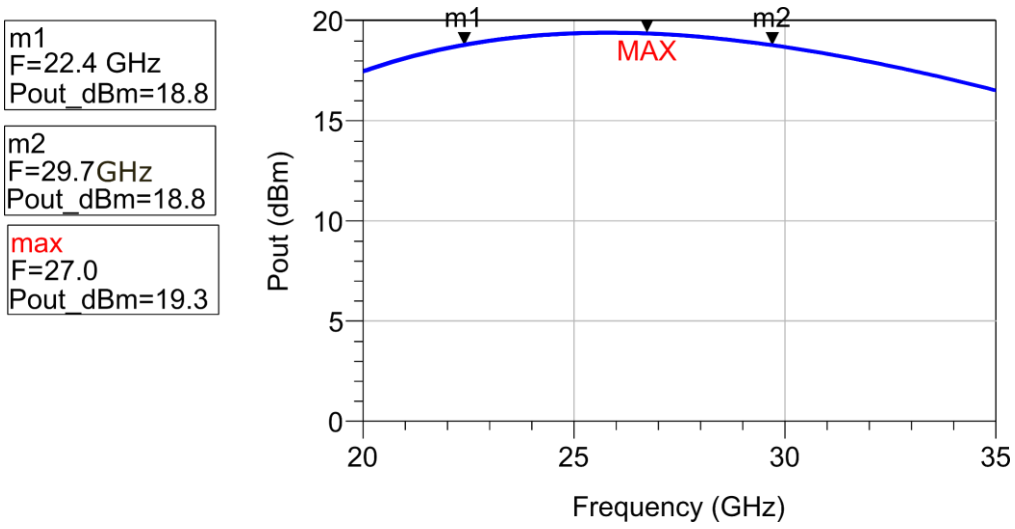

Figure 4. 16: Output power vs frequency at 1dB Gain compression point

The S-parameters of the complete stacked-cell amplifier after EM simulations are reported in Figure 4. 17, providing a realistic assessment of the layout-level performance.

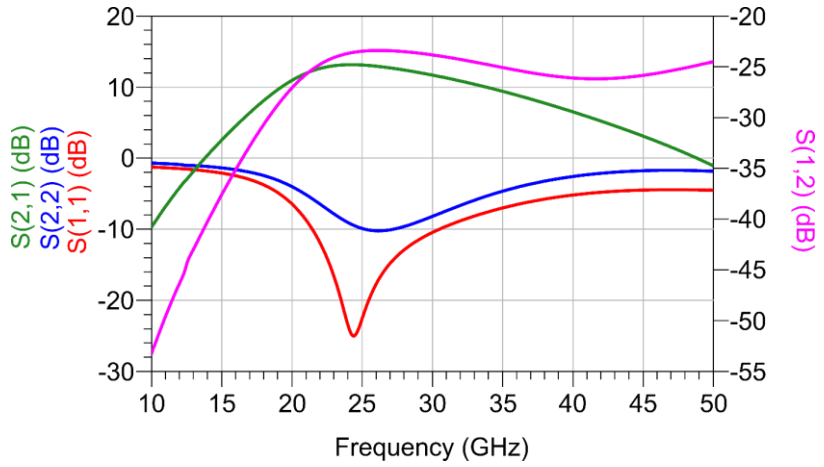

Figure 4. 17: S-parameter of full stacked cell after EM simulation; S_{11} (Red), S_{12} (Pink), S_{21} (Green) and S_{22} (Blue)

Figure 4. 17 shows that the main design targets are met. The input and output reflection coefficient S_{11} and S_{22} respectively are below −10 dB around the operating frequency, which indicates acceptable input and output matching, while S_{21} provides sufficient gain over the target band. The reverse isolation S_{12} remains low, ensuring stable operation. Overall, the specifications are satisfied, with only minor performance degradation.

Figure 4. 18 presents a micrograph of the fabricated stacked-cell MMIC implemented in 0.1 µm GaAs technology, acquired using an optical microscope.

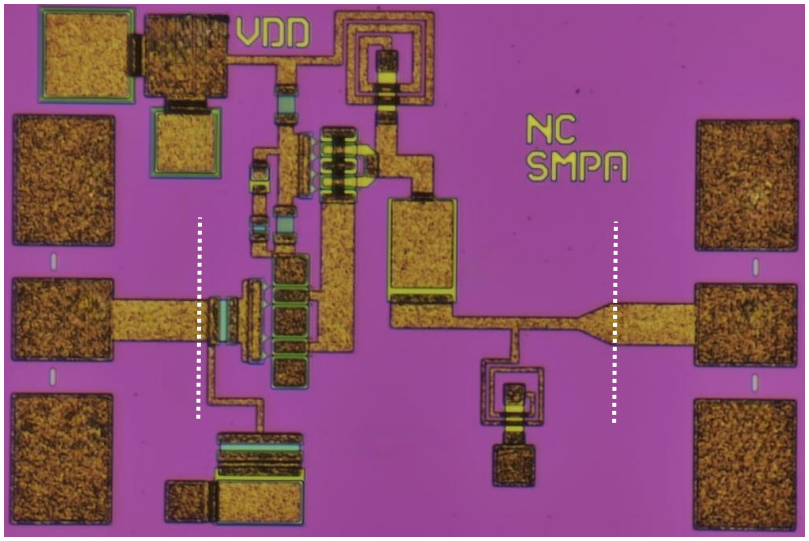

Figure 4. 18: Micrograph of the produced Stacked cell

6.7 Chip Measurement Analysis

The fabricated cell was characterized as an on-wafer cell using the setup shown in Chapter 3. The measurements have been carried out using on-wafer TRL calibration to remove the effects of pads and access lines, as shown by dashed lines in Figure 4.18.

The measured S-parameters are shown in Figure 4. 19 compared to simulation results. The simulation predicts the cell behavior quite well, but the small-signal gain is underestimated. This effect has been found to be related to the active device 3-port model, which underestimates transconductance. A more accurate large-signal model is under development based on ad-hoc common-source and common-gate test structures.

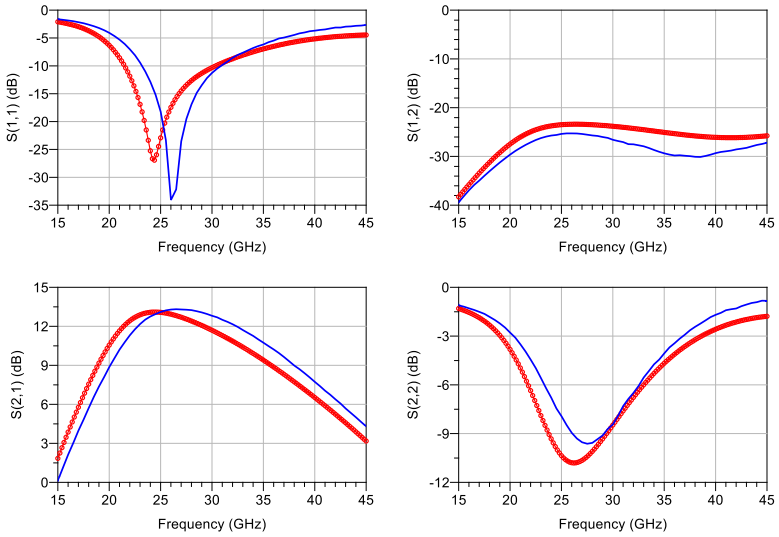

Figure 4. 19: S-parameter measurements and simulation comparison; the blue solid line is measured, and the red symbol line is the simulation.

Figure 4. 20 shows the power gain at 27 GHz as a function of the input power. The 1 dB compression point (P1dB) of the designed circuit was characterized at 27 GHz using a VNA, under the nominal bias conditions of V_{DD} and Id = 18.3 mA. During the measurement, the input power was swept over a defined range while monitoring the gain response. As the input power increased, the gain progressively deviated from its linear small-signal behavior, indicating the onset of nonlinear operation. The P_{1dB} was determined as the input power level at which the gain dropped by 1 dB from its linear extrapolated value. This measurement provides an effective assessment of the amplifier large-signal behavior and represents a key indicator of its linearity at high frequency. EM simulation overestimated the losses, so, based on the measurements, the achieved gain compression is higher.

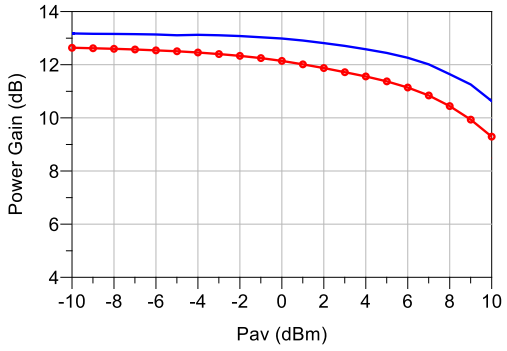

Figure 4. 20: Gain compression versus input power, the blue solid line is measured, and the red symbol line is the simulation at VDD = 6V and Id = 18.3 mA at 27 GHz.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

This thesis explored the characterization and modeling of GaAs pHEMT technology jointly with the design and implementation of millimeter-wave power amplifiers, focusing on stacked-cell architectures to address the inherent voltage and power constraints of conventional single-transistor and parallel-combined amplifiers. The research is driven by the increasing demand for high-performance, efficient, and compact RF front ends in modern wireless communication, radar, and space systems. GaAs technology is still favored for its maturity, linearity, reliability, and proven performance in high-frequency uses.

A primary contribution of this thesis is the development of a comprehensive methodology encompassing device-level characterization and modeling through to circuit-level design and layout-aware implementation of a stacked-cell MMIC power amplifier at 27 GHz. Instead of treating device modeling and circuit design as isolated processes, a unified approach was adopted in which measurement-based device characterization informs model extraction, and validated models are subsequently utilized in technology-aware circuit design. This integrated

framework ensures physical consistency, predictive accuracy, and robustness across multiple abstraction levels.

At the device level, detailed experimental characterization of 0.1 μm GaAs pHEMTs was performed to evaluate performance and reliability. Large-signal low-frequency measurements were used to study the device's current-generator behavior under realistic RF-like stress, allowing observation of voltage and current waveforms without interference from high-frequency parasitic effects. This method gave useful insights into power capability, drain efficiency, and dynamic behavior, and served as a practical, cost-effective alternative to complex microwave measurements. Additional DC and small-signal S-parameter measurements up to millimeter-wave frequencies were used to check temperature effects, dispersion, and stability, confirming the technology's robustness for high-frequency power amplifier design.

These measurements enabled the development of a reliable and compact small-signal modeling framework. By extracting extrinsic parasitic elements and intrinsic device parameters, the models could accurately reproduce measured S-parameters across different frequencies and biases, forming a strong base for later circuit simulations. Special attention was given to modeling parasitic capacitances and access networks, which greatly affect performance at millimeter-wave frequencies. The final models matched experimental data well and were useful for stability analysis, impedance matching, and large-signal simulations.

This thesis goes beyond standard modeling by providing a focused analysis of common-gate (CG) device behavior in stacked-cell architectures. Although stacked power amplifiers are well known, their use at millimeter-wave frequencies is often limited by challenges in inter-stage matching, voltage distribution, and gate power leakage. Here, the CG gate capacitance was studied closely, showing its dual role in inter-stage impedance transformation and voltage waveform alignment. Analytical relationships between gate capacitance, device transconductance, operating frequency, and optimal load impedance were discussed and evaluated considering real-world parasitic effects. The analysis showed that higher frequencies and more stacked devices increase mismatch and reduce current gain, setting a practical limit on how many devices can be stacked for a given technology.

These theoretical insights directly guided the design choices for the stacked-cell power amplifier presented in this thesis. Considering the selected GaAs technology and the target frequency of 27 GHz, a two-stage stacked configuration consisting of one common-source (CS) device and one pseudo-common-gate stage was identified as the most suitable compromise between achievable output power, gain, stability, and bandwidth. Stability analysis based on the K-factor revealed the intrinsic tendency of the device toward instability at high frequencies, motivating the systematic design and comparison of different stabilization network topologies. The adopted solution successfully suppressed out-of-band gain while preserving in-band performance, demonstrating the importance of stability-aware design at both schematic and layout levels.

Large-signal load-pull simulations were then employed to determine the optimum load impedances for power, gain, and efficiency, recognizing that these values typically differ from those derived through small-signal conjugate matching. By balancing power and small-signal matching, the design achieved performance suitable for broadband operation. Harmonic balance simulations at the schematic level confirmed the advantages of device stacking, showing approximately 3 dB improvements in output power and gain relative to a single-device configuration, in close agreement with theoretical expectations. The stacked architecture achieved a saturated output power near 20 dBm, a power gain exceeding 12 dB, and a peak power-added efficiency (PAE) above 40% under ideal load conditions, thereby validating the proposed approach.

A significant aspect of this work is the layout-aware implementation and electromagnetic (EM) co-simulation of the stacked-cell MMIC. Given that layout-induced parasitic elements can substantially impact millimeter-wave performance, critical interconnections, matching networks, and stability elements were meticulously designed using foundry-specified components and guidelines. EM simulations were used to account for coupling, parasitic inductances, and metal interconnect effects not shown in schematics. The results showed that bandwidth and matching are highly sensitive to layout details, particularly in inter-stage connections and DC feed structures, underscoring the importance of EM-driven design for high-frequency power amplifiers.

The final outcome of this work is the fabrication of a complete GaAs stacked-cell MMIC, whose micrograph confirms the feasibility of integrating the proposed architecture within a realistic chip area and technology platform. While post-fabrication RF measurements are outside the current scope, the design flow, modeling strategy, and simulation results collectively provide strong confidence in the expected performance and establish a solid basis for future experimental validation.

In summary, this thesis demonstrates that GaAs pHEMT stacked-cell power amplifiers continue to represent a viable and competitive solution for millimeter-wave applications, especially when supported by accurate device modeling, careful stability control, and layout-aware design methodologies. This work bridges the gap between device physics and circuit implementation, providing both theoretical insights and practical design guidance for next-generation millimeter-wave power amplifiers.

5.2 Future Work

Several directions for future research arise from this work. First, experimental RF characterization of the fabricated MMIC is essential to validate the proposed modeling framework and to assess the impact of layout parasitics under real operating conditions. Load-pull and large-signal measurements would provide further insights into efficiency, linearity, and robustness.

Second, the proposed methodology may be extended to greater stack depths and higher frequencies, particularly in advanced GaAs or scaled GaN technologies, where enhanced cut-off frequencies may relax some of the limitations identified in this study. Hybrid stacking strategies that integrate stacked cells with load-modulated or Doherty architectures may further improve efficiency under power back-off conditions.

The proposed GaAs stacked-cell power amplifier concept warrants further investigation within advanced, efficiency-enhancing architectures, particularly the Doherty power amplifier (DPA). The Doherty architecture is widely adopted in modern wireless transmitters due to its capacity to significantly improve average efficiency under power back-off conditions, which is critical for signals with high peak-to-average power ratios.

At millimeter-wave frequencies, the implementation of Doherty power amplifiers in GaAs technologies is challenging due to limited breakdown voltages and low optimal load impedances of single transistors. These constraints result in high impedance transformation ratios and increased losses in the Doherty output combiner, ultimately limiting bandwidth and efficiency. In this context, stacked-cell power amplifiers can function as high-voltage, high-impedance macro-devices, thereby mitigating these limitations.

By employing stacked cells in the carrier amplifier, the effective voltage swing and output impedance can be increased, relaxing the design requirements of the Doherty load modulation network. This approach has the potential to improve both saturated efficiency and back-off efficiency while preserving compact layout and manageable device stress. Furthermore, the improved voltage distribution inherent to stacked architectures can enhance reliability when operating under dynamically varying load conditions, as commonly encountered in Doherty operation.

From a modeling and design perspective, the framework developed in this thesis offers the necessary tools to support such extensions. Specifically, the accurate modeling of common-gate device behavior, inter-stage matching via gate capacitance optimization, and stability-aware design can be directly applied to the analysis of stacked-cell Doherty amplifiers. Future research should incorporate dynamic load modulation effects, phase alignment between carrier and peaking paths, and broadband stability considerations within the stacked configuration.

Overall, the integration of stacked-cell architectures with Doherty operation represents a promising research direction for achieving highly efficient, broadband, and linear millimeter-wave power amplifiers in GaAs technologies. This approach could substantially enhance the competitiveness of GaAs-based solutions in next-generation communication and space-qualified systems, where efficiency, linearity, and technological maturity are all essential.

Finally, the modeling insights developed for the common-gate stage may be further refined to incorporate nonlinear capacitance behavior, thermal coupling, and memory effects, thereby enabling more accurate prediction of large-signal performance in wideband and high peak-to-average power ratio (PAPR) applications.

In conclusion, this thesis establishes a comprehensive foundation for further exploration of stacked-cell power amplifiers and contributes significant advances to the design of efficient, high-frequency RF power devices.

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