SCUOLA DI DOTTORATO
UNIVERSITÀ DEGLI STUDI DI MILANO-BICOCCA

Department of **Materials Science**

Ph. D. program in **Materials Science and Nanotechnology**

Highly Sensitive CMOS-Based Current Readout for Nanopore Sensing

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Academic Year 2025/2026

Abstract

This dissertation presents the design, implementation, and experimental validation of an ultra-low-noise continuous-time CMOS current readout system for nanopore-based single-molecule sensing. The work addresses the fundamental challenge of simultaneously achieving sub-femtoampere noise resolution, wide DC dynamic range, and reset-free continuous operation within a fully monolithic standard CMOS implementation — a combination that existing transimpedance amplifier (TIA) architectures cannot jointly satisfy due to inherent trade-offs between feedback element noise, signal dynamic range, and circuit complexity.

The first contribution is a novel TIA topology in which the intrinsic drain–bulk PN junction of a MOSFET is exploited as the feedback element by deliberately suppressing channel conduction through appropriate gate biasing. Under this operating condition, both flicker noise and channel thermal noise are eliminated at the device level; the residual noise of the feedback element is governed solely by junction shot noise, which at pA-level bias currents is equivalent to the thermal noise of a passive GΩ–TΩ resistor. The TIA core employs complementary anti-parallel PN junction pairs for bipolar operation, a ratiometric current amplifier for linearisation of the nonlinear junction impedance, and pole-zero compensation for independent bandwidth control.

The second contribution is a DC-compensated readout architecture that augments the TIA core with a dedicated DC-servo feedback loop. The loop continuously diverts the large open-pore baseline current — inherent to nanopore sensing — away from the TIA signal path, decoupling the DC operating point from the AC signal chain and restoring near-ideal low-noise conditions regardless of the baseline magnitude. This architecture enables a DC dynamic range of $\pm 50\,\mathrm{nA}$ to be accommodated simultaneously with sub-pA AC resolution, without periodic reset or operator intervention.

Both architectures are implemented as a dual-channel monolithic ASIC in $0.35\,\mu\mathrm{m}$ X-Fab CMOS and validated on a dedicated PCB-based readout platform. Experimental characterisation of the fabricated circuit demonstrates an input-referred noise density of $1.5\,\mathrm{fA}/\sqrt{\mathrm{Hz}}$ and integrated RMS noise of 240 fA over 10 kHz, 2.6 pA over 100 kHz, and 38.2 pA over 1 MHz, confirming theoretical noise predictions and shot-noise-dominated operation. Measurements with a solid-state SiN_x nanopore device, conducted at the Keyser Lab, University of Cambridge, demonstrate continuous single-molecule λ-DNA translocation detection under biologically relevant conditions, validating the complete sensing platform from nanopore chip to digital output.

Keywords: CMOS integrated circuits, transimpedance amplifier, nanopore sensing, current readout, single-molecule detection, low-noise analog front-end, PN junction feedback, DC compensation, ASIC, biosensor interface.

Acknowledgements

I would like to express my gratitude to my supervisors, Dr. Federico Thei, my industrial supervisor at Elements Srl, and Prof. Sergio Brovelli, my academic supervisor at the University of Milano-Bicocca, for their time and guidance throughout my doctoral research.

I am also grateful to Prof. Francesco Montalenti, coordinator of the PhD program, for his guidance and support throughout my doctoral studies.

My thanks go to my colleagues at Elements Srl, especially Marco Bennati and Michele Biondi, for their valuable discussions and technical support throughout the development of the data-acquisition system and the complete readout platform.

I would like to thank Prof. Ulrich Keyser and the members of the KeyserLab at the Cavendish Laboratory, University of Cambridge, for providing the opportunity to carry out the nanopore experiments and for their valuable assistance during the experimental validation of this work.

I am grateful to Prof. Xin Yin and the IDLab research group at Ghent University for hosting me during my research secondment and for the stimulating research environment throughout my stay.

My sincere thanks also go to Prof. Marco Crescentini at the University of Bologna, Cesena Campus, for his valuable comments, suggestions, and careful feedback during the preparation of the manuscripts arising from this work.

I gratefully acknowledge the DYNAMO Doctoral Network, which has received funding from the European Research Executive Agency (REA) under the European Union's Horizon Europe research and innovation programme through the Marie Skłodowska-Curie Actions Doctoral Networks, Grant Agreement No. 101072818. I am grateful for the research, training, international mobility, and collaboration opportunities made possible through the project.

Finally, I would like to express my deepest gratitude to my family. I am especially thankful to my father and mother for their unconditional love, encouragement, and sacrifices throughout my life, and to my sister for her constant encouragement and affection. Last but not least, I am deeply grateful to my wife, who has always encouraged me to move forward and stood by me throughout this journey. In moments of disappointment and difficulty, she was always there to motivate me, support me, and remind me to keep going.

List of Publications

Journal Article:

- Minimizing the Noise in Low-Current Sensing by MOSFET p-n Junction Diode Feedback
  Ehsan Semsar Parapari, Marco Bennati, Michele Biondi, Marco Crescentini, and Federico Thei
  IEEE Solid-State Circuits Letters, vol. 9, pp. 162–165, 2026.
  DOI:10.1109/LSSC.2026.3692971

Patents:

- Improved Low-Noise Current Amplifier and Operation Method Thereof
  Ehsan Semsar Parapari, Marco Bennati, Michele Biondi, and Federico Thei
  European Patent Application, filed 2025.
- AC–DC Splitting Current Amplifier
  Ehsan Semsar Parapari, Marco Bennati, Michele Biondi, and Federico Thei
  European Patent Application, filed 2025.

Contents

List of Figures

List of Tables

List of Acronyms

AAF	Anti-Aliasing Filter
ADC	Analog-to-Digital Converter
AFE	Analog Front-End
ASIC	Application-Specific Integrated Circuit
CAPPOLY	Poly-Poly Capacitor (X-Fab process module)
CBD	Controlled Dielectric Breakdown
CDS	Correlated Double Sampling
CMOS	Complementary Metal-Oxide-Semiconductor
CT	Continuous-Time
CV	Coefficient of Variation
DAC	Digital-to-Analog Converter
DMIM	Double Metal-Insulator-Metal capacitor
DNA	Deoxyribonucleic Acid
DRC	Design Rule Check
DSM	Delta-Sigma Modulator
DT	Discrete-Time
EDA	Electronic Design Automation
FIB	Focused Ion Beam
FPGA	Field-Programmable Gate Array
GBW	Gain-Bandwidth Product
I–V	Current–Voltage
ISOMOS	Isolated MOSFET (X-Fab process module)
LDO	Low-Dropout Regulator
LNA	Low-Noise Amplifier
LVS	Layout-Versus-Schematic
MEPR	Multi-Element Pseudo-Resistor
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS	N-channel MOSFET
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PMOS	P-channel MOSFET
PMMA	Poly(methyl methacrylate)
PR	Pseudo-Resistor
PSD	Power Spectral Density

QFN	Quad Flat No-lead (package)
RMS	Root-Mean-Square
RNA	Ribonucleic Acid
SCK	Serial Clock
SDI	Serial Data Input
SDO	Serial Data Output
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
SQNR	Signal-to-Quantisation-Noise Ratio
TEM	Transmission Electron Microscopy
TIA	Transimpedance Amplifier
USB	Universal Serial Bus

Chapter 1

Introduction

1.1 Electrical Current Readout

Electrical current measurement is one of the most fundamental modalities in scientific instrumentation. Many physical, chemical, and biological processes either generate electrical currents directly or can be transduced into current signals, making current readout a universal interface between sensing phenomena and electronic systems. In electrochemistry, Faradaic currents produced by oxidation and reduction reactions at electrode surfaces provide information about analyte concentration, reaction kinetics, and interfacial charge transfer [1, 2]. In solid-state physics, nanoscale transport phenomena such as tunneling currents and Coulomb blockade are accessed through precise current measurements [3]. In neuroscience, the patch-clamp technique introduced by Neher and Sakmann [4] enabled the direct observation of pA-level ionic currents flowing through single ion channels embedded in lipid membranes [5]. Across these diverse disciplines, electrical current signals provide a direct and quantitative representation of the underlying physical processes.

A major trend in modern sensing is the transition from ensemble measurements toward nanoscale and single-entity investigations. Unlike conventional approaches that average over large molecular populations—thereby obscuring heterogeneity, stochastic behavior, and rare events—modern nanoscale science increasingly aims to observe individual molecules, nanoparticles, and single biological entities directly. This transition has been enabled by advances in nanotechnology, molecular biology, and bioelectronics.

As the scale of observation decreases, the associated electrical signals become progressively smaller. In single-molecule electrochemistry, nanoscale biosensing, and quantum-scale devices, relevant steady-state or transient currents frequently fall within the pA and sub-pA ranges [6, 7]. Individual binding events, conformational changes, and charge-transfer processes may produce transient current variations below 1 pA, with durations ranging from microseconds to milliseconds [8, 9]. The progressive reduction of signal amplitude in nanoscale experiments has therefore imposed increasingly stringent demands on measurement instrumentation.

1.2 Nanopore Sensing

Among the sensing platforms that have most successfully exploited sensitive electrical current measurement, nanopore-based sensors have emerged as one of the most powerful approaches for label-free single-molecule analysis. By monitoring the ionic current modulation produced by the translocation of individual molecules through a nanometer-scale aperture, nanopore sensors provide direct, real-time access to molecular identity, size, charge, and structure [10–12]. The operating principles, applications, and instrumentation requirements of nanopore sensing are introduced in the following subsections.

1.2.1 Principles

A nanopore is a nanometric aperture—typically 1 nm to 20 nm in diameter—formed in an ultrathin membrane separating two electrolyte-filled compartments, conventionally designated as the *cis* and *trans* chambers [13, 14]. When a DC voltage bias is applied across the membrane, ionic transport through the nanopore establishes a steady open-pore current I_0, as illustrated in Fig. 1.1(a) [15]. When a charged analyte—such as a DNA molecule, a protein, or a small-molecule species—translocates through the pore, it partially occludes the ionic pathway and reduces the current, as illustrated in Fig. 1.1(b). The resulting transient current blockade is characterized by an amplitude $\Delta I = I_0 - I$ and a dwell time τ, as shown in Fig. 1.1(c) [8, 16]. These parameters are characteristic of the translocating molecule and, at sufficient measurement resolution, encode information about its size, charge, and molecular structure.

A defining attribute of nanopore sensing is that the measurement is inherently single-molecule, label-free, and performed in real time [8]. No fluorescent labeling, amplification, or surface immobilization is required. This enables the observation of molecular heterogeneity, transient conformational states, and rare events inaccessible to ensemble-averaging techniques [17]. Because each translocation event generates a discrete, time-resolved electrical signal, nanopore sensing is also naturally amenable to the statistical analysis of large molecular populations within a single measurement session.

1.2.2 Applications

The application landscape of nanopore sensing has expanded substantially since the seminal demonstration by Kasianowicz *et al.* in 1996 [18], which established translocation-based detection of individual polynucleotides through an α-hemolysin channel. The following areas represent its most impactful domains to date.

DNA and RNA sequencing. The most commercially mature application is third-generation sequencing, in which sequence-dependent current modulations produced as a DNA strand is ratcheted through a protein nanopore are decoded directly, without amplification or optical detection [11, 14]. Oxford Nanopore Technologies has

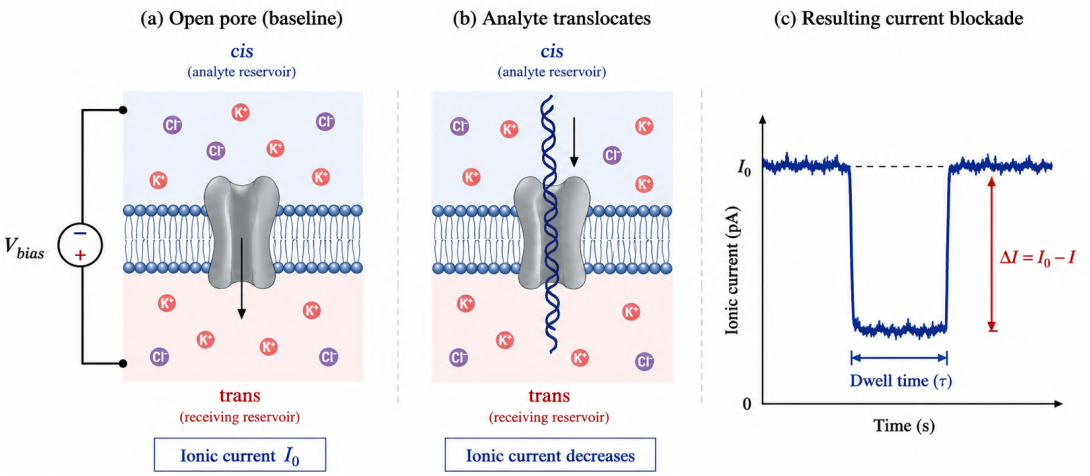


Figure 1.1: Principle of nanopore sensing: (a) open-pore ionic current I_0, (b) DNA translocation through the nanopore, and (c) the resulting current blockade characterized by amplitude $\Delta I = I_0 - I$ and dwell time τ.

commercialized this approach, enabling portable, real-time, long-read sequencing with broad impact in genomics, clinical diagnostics, and environmental monitoring [16].

Protein sensing and sequencing. Extending nanopore sensing to proteomics—encompassing the direct electrical readout of protein identity, conformational states, and post-translational modifications—is a frontier of intense current research [10]. Engineered biological nanopores have demonstrated discrimination of individual amino acids and detection of post-translational modifications at the single-molecule level [8, 16].

Single-molecule kinetics and binding studies. The time-resolved nature of the nanopore signal makes it well suited to the study of molecular interactions, including protein–ligand binding, enzyme kinetics, and nucleic acid hybridization. Direct observation of individual binding events provides access to energy landscapes and mechanistic details inaccessible to bulk assays [8, 17].

Clinical diagnostics. The label-free, portable, and low-cost nature of nanopore platforms makes them attractive for point-of-care diagnostics, pathogen detection, and liquid biopsy [10, 19].

1.2.3 Nanopore Types

Two principal categories of nanopores are employed in sensing applications, each presenting distinct characteristics and trade-offs [15].

Biological Nanopores

Biological nanopores are protein ion channels—most notably *α-hemolysin* (αHL), *MspA*, and *CsgG*—reconstituted into lipid bilayer membranes [15, 16]. Their well-

defined, genetically tunable geometry and high interprotein reproducibility make them the platform of choice for high-resolution sensing and sequencing. They exhibit moderate open-pore currents—typically 50 pA to 300 pA at 100 mV—and low intrinsic noise, and they underpin current commercial nanopore sequencers. Their primary limitation is the mechanical fragility of the lipid bilayer substrate, which complicates integration with solid-state fabrication and constrains accessible experimental conditions.

Solid-State Nanopores

Solid-state nanopores are fabricated in inorganic membranes—silicon nitride (SiN_x), silicon dioxide (SiO_2), graphene, or molybdenum disulfide (MoS_2)—using focused ion beam (FIB) milling, transmission electron microscopy (TEM) drilling, controlled dielectric breakdown (CBD), or chemical etching [13, 14]. Their mechanical robustness, compatibility with CMOS fabrication, and tunability of pore geometry and surface chemistry make them well-suited for large-scale integration and operation across a wide range of conditions. Compared with biological nanopores, they exhibit higher open-pore currents and higher current noise, the latter arising primarily from dielectric loss and elevated membrane capacitance [15]. Nucleotide-level discrimination resolution currently remains inferior to that of engineered protein pores, although progress continues through surface functionalization and membrane engineering [14].

1.2.4 Electrical Model and Readout Requirements

From the perspective of the electronic readout interface, the nanopore–electrolyte–electrode system is represented by the equivalent circuit shown in Fig. 1.2. The ionic conductance of the pore is modeled as R_{pore} in series with the electrolyte access resistances $R_{\text{electrolyte}}$ on each side of the membrane [15]. The insulating membrane contributes a shunt capacitance C_{mem}, while in solid-state devices, the supporting substrate introduces additional parasitic elements C_{sub} and R_{sub}, which are absent in biological nanopore systems. For thin SiN_x membranes on silicon substrates, the aggregate device capacitance can reach tens to hundreds of pF depending on geometry [15].

This electrical environment gives rise to a set of demanding and often conflicting requirements for the readout interface. The ionic signal consists of a steady DC baseline I_0 generated by the open-pore conductance, superimposed with transient blockade events ΔI induced by molecular interactions. The baseline current may reach hundreds of pA in biological nanopores and tens of nA in solid-state nanopores, whereas the current blockades typically constitute only a small fraction of the baseline [15]. This combination imposes stringent dynamic range requirements: the front-end must simultaneously accommodate the large DC baseline while resolving the small, fast AC-like blockade components superimposed on it.

Beyond dynamic range, the signal current ΔI may be as small as a few pA, requir-

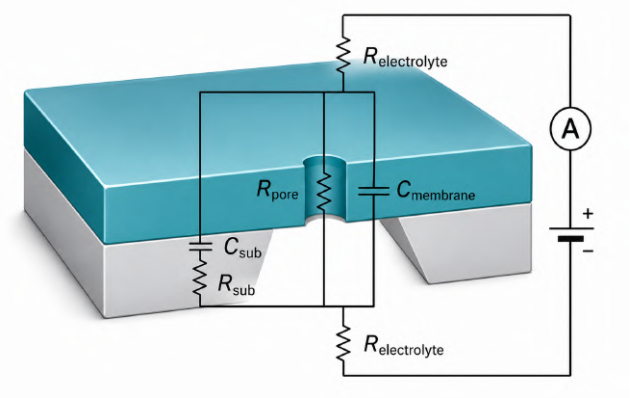


Figure 1.2: Equivalent circuit of a solid-state nanopore device: pore resistance R_{pore}, membrane capacitance C_{mem}, substrate parasitics C_{sub} and R_{sub}, and electrolyte access resistances $R_{\text{electrolyte}}$. The ammeter (A) represents the current readout instrument.

ing a front-end with a sufficiently low noise floor to resolve it. A DC voltage bias must be applied across the membrane to drive ionic transport; any noise or instability on this bias directly appears as current noise at the readout input, imposing an additional constraint on the voltage source quality [20]. Translocation events occur on microsecond-to-millisecond timescales, demanding adequate measurement bandwidth. Furthermore, parasitic capacitance at the input node elevates the high-frequency noise floor, fundamentally limiting measurement resolution [8, 15, 20]. These requirements—low input-referred noise, wide dynamic range, and sufficient bandwidth—define the design space for nanopore readout electronics and directly motivate the survey of existing architectures presented in the following section.

1.3 State of the Art in Readout Systems

To meet the requirements outlined in the previous section, several current-readout architectures have been developed. The analog front-end is the core of a current-readout system, as it directly determines the achievable noise, bandwidth, and dynamic-range performance. Among the available approaches, transimpedance amplifiers (TIAs) are widely adopted, converting the sensor current into a measurable output voltage while maintaining a low input impedance at the sensing node. From an architectural perspective, current-readout approaches can be broadly divided into discrete-time (DT) and continuous-time (CT) implementations. DT architectures commonly rely on capacitive feedback and a reset mechanism, whereas CT architectures maintain a continuous feedback path through DC-compensation or resistive-feedback schemes [21]. The following subsections review these approaches and their main trade-offs.

1.3.1 Discrete-Time Current Readout

Discrete-time (DT) current-readout architectures are commonly based on capacitive-feedback TIAs. The most direct architecture is a current integrator, in which the input current is integrated onto a feedback capacitor, generating a ramping output voltage proportional to the accumulated charge. In the presence of a DC input current, charge continuously accumulates on the feedback capacitor and eventually drives the amplifier output toward saturation. The capacitor must therefore be periodically reset to remove the accumulated charge and restore the initial operating condition. The reset operation interrupts the measurement and introduces non-idealities such as kT/C noise, charge injection, and transient disturbances, which limit the minimum detectable signal. In addition, the integration time determines the achievable bandwidth, leading to a sensitivity–bandwidth trade-off: longer integration improves the resolution of small currents, but reduces temporal resolution and bandwidth. One approach to mitigate the non-idealities associated with the reset operation is correlated double sampling (CDS). Bennati *et al.* employed this technique in a CMOS current-readout circuit to suppress reset-related errors and low-frequency noise [22]. The integrator output is sampled immediately after reset and again at the end of the integration interval. By subtracting the two samples, correlated components associated with offset, low-frequency noise, and reset-induced disturbances are largely suppressed. The same reset–integrate–sample principle has also been adopted in more recent highly integrated systems. Dawji *et al.* demonstrated a scalable DT CMOS readout array for nanopore sensing, combining a capacitive-feedback current integrator with correlated double sampling and in-pixel SAR conversion [23]. The front-end supports bandwidths up to 100 kHz, although the minimum noise floor of approximately 4 fA/$\sqrt{\text{Hz}}$ is obtained at lower-bandwidth operating conditions, reflecting the trade-off between integration time, noise, and bandwidth. To relax the bandwidth limitation of the simple current integrator, integrator–differentiator architectures have been proposed. In this approach, the input current is first integrated and the resulting signal is subsequently differentiated, reconstructing an output proportional to the input current. This allows the output sampling frequency to be decoupled from the integrator reset frequency, so that the signal bandwidth is no longer directly determined by the integration interval. The integrator, however, still requires reset to prevent saturation. Crescentini *et al.* implemented this approach, achieving an input-referred noise floor as low as 4 fA/$\sqrt{\text{Hz}}$ while supporting acquisition bandwidths up to 100 kHz [24]. A comparable maximum bandwidth is provided by the Axopatch 200B, a widely used benchmark for low-current measurements, which also employs an integrator–differentiator architecture and reaches a noise floor as low as 0.7 fA/$\sqrt{\text{Hz}}$ [25]. This very low-noise performance is supported by an actively cooled headstage. Despite its excellent sensitivity, the Axopatch is a bulky and expensive instrumentation-level system and is therefore not suitable for monolithic integration or highly parallel acquisition platforms. In addition to the noise–bandwidth trade-off, the finite charge-storage capability of the feedback capacitor also limits the achievable dynamic range. Increasing the feedback capacitance allows a larger amount of charge to be accumulated before the integrator reaches saturation, thereby extending the maximum measurable

input current. However, for a given integration time, a larger feedback capacitor reduces the current-to-voltage conversion gain and therefore the sensitivity to small currents. Moreover, the increased capacitance can enhance the contribution of the amplifier voltage noise at high frequencies, further affecting the noise performance. Awan *et al.* proposed an asynchronous capacitive-feedback TIA in which the reset event is generated by a self-timed control network rather than by a fixed periodic clock [26]. The integrator is therefore reset according to the accumulated signal, allowing the readout to accommodate a wide range of input currents without relying on a fixed integration interval. Combined with time-domain quantization, the architecture achieved a reported dynamic range of 124 dB with an input-referred noise of 1 $\mathrm{pA_{rms}}$. Overall, capacitive-feedback DT architectures provide an attractive route to very low-noise current measurement, since the primary feedback element can be implemented without the thermal-noise penalty associated with a physical resistor. However, their performance remains strongly influenced by the reset operation, finite charge-storage capability, and the associated trade-offs among noise, bandwidth, and dynamic range.

1.3.2 Continuous-Time Current Readout

Continuous-time (CT) readout architectures enable uninterrupted current measurement without the reset-induced discontinuities and information loss that characterize DT implementations. Several approaches have been pursued to realize CT operation, each involving different noise, bandwidth, and implementation trade-offs. One approach is to retain the capacitive-feedback front-end while introducing an auxiliary DC-compensation path. This low-frequency feedback loop removes the DC or slowly varying component of the input current, preventing charge accumulation on the feedback capacitor and avoiding output saturation without interrupting the measurement. Ferrari and Sampietro implemented this concept in an integrator–differentiator TIA [27], accommodating DC currents of up to approximately ±10 nA while achieving a low-frequency input-referred noise floor of approximately 8 $\mathrm{fA}/\sqrt{\mathrm{Hz}}$ and a signal bandwidth of about 1.4 MHz. The additional feedback path, however, contributes its own noise to the TIA input and can therefore degrade the overall noise performance compared with an ideal purely capacitive-feedback implementation. To reduce this contribution, Ferrari *et al.* and Häberle *et al.* employed high-value active or pseudo-resistive elements in the DC-compensation path [28, 29]. The reported minimum input-referred noise floors were approximately 4 $\mathrm{fA}/\sqrt{\mathrm{Hz}}$ and 1.6 $\mathrm{fA}/\sqrt{\mathrm{Hz}}$, respectively. Despite these advancements, the dynamic range of the AC signal path remains limited by the finite output swing of the integrator. A further challenge is the stability of the additional low-frequency feedback loop, which must be carefully designed to preserve the desired signal bandwidth. An alternative and conceptually simpler CT implementation is the conventional resistive-feedback TIA, in which the input current is continuously converted into an output voltage through a feedback resistor. This inherently provides a DC path and therefore avoids the need for periodic reset or an auxiliary discharge mechanism, at the expense of the thermal-noise contribution of the feedback resistor, which is absent in an ideal

capacitive-feedback element. For high-sensitivity current sensing, a very large feedback resistance is required. For example, the Axopatch 200B employs a 500 MΩ feedback resistor in its resistive mode and achieves an input-referred noise floor of approximately 6 fA/$\sqrt{\text{Hz}}$ [25]. To approach the noise levels of capacitive-feedback architectures, GΩ-range feedback resistances are often required. However, such large physical resistors exhibit significant shunt capacitance, which limits the achievable bandwidth. Moreover, as the feedback resistance increases, the maximum measurable current is reduced by the finite output swing of the amplifier. Implementing such large resistance values in integrated CMOS technologies is also impractical because of the required silicon area and associated parasitic capacitance, which can significantly degrade the high-frequency noise performance [20]. Very large effective resistance values can instead be realized using MOS transistors, commonly referred to as pseudo-resistors (PRs), within a compact layout. These devices are typically operated in weak inversion (subthreshold), where the low current levels result in a very large effective resistance while maintaining a relatively low noise contribution [30]. However, the exponential current–voltage characteristic of subthreshold devices leads to strongly nonlinear behavior, which necessitates additional linearization techniques. Ferrari *et al.* exploited subthreshold MOS devices in the feedback path, achieving an input-referred noise floor as low as 500 aA/$\sqrt{\text{Hz}}$, while mitigating their nonlinear behavior through a matched double-MOS architecture [31]. Djekic *et al.* employed a multi-element pseudo-resistor architecture to improve PR linearity, achieving a minimum input-referred noise floor of approximately 5.5 fA/$\sqrt{\text{Hz}}$ [32]. In addition to linearity considerations, a further challenge is maintaining the PRs in weak inversion across operating conditions, since this regime is essential for preserving both the very large effective resistance and the low-noise performance. Despite these developments, the DC baseline current in resistive-feedback TIAs still consumes part of the available output swing, thereby limiting the remaining dynamic range for AC signal variations. Overall, CT architectures avoid the periodic reset required in DT readouts and enable uninterrupted current acquisition. However, the continuous feedback or DC-compensation path introduces additional input-referred noise, including white- and flicker-noise contributions depending on the implementation.

1.4 Goal of the Work and Major Achievements

The preceding sections have established the demanding requirements of nanopore current readout and the trade-offs associated with existing DT and CT architectures. Simultaneously achieving sub-pA current resolution, μs-scale temporal resolution, the capability to accommodate DC baseline currents in the tens-of-nA range while preserving sufficient dynamic range for small current variations, and compact CMOS integration remains challenging. The goal of this work is therefore to develop an integrated current-readout architecture capable of addressing these requirements for nanopore sensing.

The first contribution is a continuous-time TIA architecture that exploits the intrin-

sic drain–bulk PN junction of a MOSFET as the feedback element while suppressing channel conduction. This avoids the channel thermal- and flicker-noise contributions associated with subthreshold MOS feedback, while remaining fully compatible with standard CMOS technology. The intrinsic noise of the feedback element is primarily determined by PN-junction shot noise.

The second contribution extends the low-noise TIA core with a dedicated DC-servo loop. The servo diverts the large DC baseline current from the main signal path, allowing small AC current variations to be processed without consuming the available output headroom. By combining DC compensation with a resistive-feedback TIA core, the proposed architecture also benefits from simple and stable servo-loop dynamics.

The proposed architectures were implemented in a monolithic CMOS ASIC and integrated into a dedicated PCB-based readout platform. Experimental characterization was performed at both circuit and system levels, followed by validation with solid-state nanopores and DNA translocation measurements.

The major achievements of this work are summarized as follows:

- A novel continuous-time PN-junction-feedback TIA achieving a minimum input-referred noise density of 1.5 fA/$\sqrt{\text{Hz}}$, with a bandwidth of approximately 1 MHz.
- A DC-compensated readout architecture capable of handling large DC baseline currents while preserving the output range available for AC current variations. The implemented system supports DC currents up to approximately ±50 nA.
- A fabricated CMOS ASIC implementing the proposed readout architecture, together with complete experimental characterization of its noise, bandwidth, stability, and dynamic-range performance.
- A complete PCB-based readout platform integrating the ASIC, nanopore interface, bias generation, and data-acquisition circuitry.
- Experimental validation with solid-state nanopores, including the acquisition of a DC open-pore current of approximately 10 nA and the detection of individual DNA translocation events.
- Journal publications and patent applications arising from the proposed circuit architectures and their experimental validation.

1.5 Organization of the Dissertation

The remainder of this dissertation is organized as follows.

Chapter 2 establishes the theoretical background for low-noise current readout. The fundamental noise mechanisms relevant to CMOS analog circuits are introduced, followed by a detailed noise analysis of the principal TIA topologies—capacitive-feedback and resistive-feedback architectures—and a general analytical framework

for DC-compensated TIA design, covering noise, dynamic range, and stability trade-offs.

Chapter 3 presents the two original circuit-level contributions of this work. The first is a novel continuous-time TIA exploiting the intrinsic drain–bulk PN junction of a MOSFET as the feedback element, with channel conduction suppressed; the operating principle, noise analysis, linearization technique, bandwidth, and stability of the implemented TIA core are described in detail. The second contribution extends the TIA core with a dedicated DC-servo loop that continuously diverts the large DC baseline current inherent to nanopore sensing, enabling wide dynamic range operation while preserving the low-noise properties of the core. The servo-loop implementation, dynamic-range analysis, noise performance, and stability are derived and discussed.

Chapter 4 presents the CMOS ASIC implementation, covering the full chip architecture, circuit-level design details, layout considerations, and fabrication process.

Chapter 5 describes the system-level integration of the ASIC into a complete readout platform, including the PCB hardware architecture, bias and control circuitry, and the experimental characterization of the integrated system.

Chapter 6 presents the experimental results obtained with nanopore devices, demonstrating single-molecule detection and evaluating the system performance under biologically relevant sensing conditions.

The dissertation closes with a summary of the main contributions and directions for future research.

Chapter 2

Fundamentals of Low-Noise Current Readout

2.1 Noise in Electronic Circuits

In any electronic measurement system, noise refers to unwanted random fluctuations superimposed on the signal of interest. Unlike deterministic interference—which originates from external sources and can in principle be suppressed by shielding or filtering—noise arises from fundamental physical processes within the circuit components themselves and therefore sets an irreducible lower bound on measurement resolution [33]. In low-current readout systems, where the signals of interest may be as small as a few pA, noise is the primary factor limiting the ability to detect and resolve individual events.

2.1.1 Noise Characteristics

Noise is a stochastic process and is therefore characterized statistically. A key descriptor is the *power spectral density* (PSD), $S_x(f)$, which quantifies the average power carried by the noise signal per unit bandwidth at each frequency [33]. More precisely, $S_x(f)$ is the average power of the noise contained in a 1 Hz bandwidth centered at frequency f, and is expressed in V^2/Hz or A^2/Hz. The square root of the PSD, expressed in $\mathrm{V}/\sqrt{\mathrm{Hz}}$ or $\mathrm{A}/\sqrt{\mathrm{Hz}}$, is referred to as the noise spectral density and is the quantity most commonly reported in circuit specifications.

A fundamental property of PSDs is that if a noise signal with spectrum $S_x(f)$ is applied to a linear time-invariant system with transfer function $H(s)$, the output spectrum is [33]:

$$S_Y(f) = S_x(f)\,|H(f)|^2 \tag{2.1}$$

This relation forms the basis of noise analysis in circuits: the noise spectrum of each source is shaped by the transfer function from that source to the output. A noise spectrum that is constant with respect to frequency is referred to as *white noise*. The total noise power over a measurement bandwidth B is obtained by integrating

the PSD:

$$P_n = \int_0^B S_x(f)\, df \qquad [\mathrm{V}^2 \text{ or } \mathrm{A}^2] \tag{2.2}$$

and the corresponding root-mean-square (RMS) noise is $\sqrt{P_n}$. This result shows that the measurement bandwidth must be limited to the minimum required value, as any excess bandwidth admits additional noise power without contributing to the useful signal.

2.1.2 Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the fundamental figure of merit for any measurement system, defined as the ratio of the signal power P_{sig} to the noise power P_{noise} [33]:

$$\mathrm{SNR} = \frac{P_{sig}}{P_{noise}} \tag{2.3}$$

The SNR is often expressed in decibels as $10\log_{10}(\mathrm{SNR})$. For a sinusoidal signal with peak amplitude A, $P_{sig} = A^2/2$, while P_{noise} is obtained by integrating the noise PSD over the measurement bandwidth according to (2.2). A high SNR is required for reliable signal detection; achieving it demands both maximizing the signal amplitude and minimizing the integrated noise power, which in turn requires that the measurement bandwidth be kept to the minimum necessary for the application.

2.1.3 Input-Referred Noise

In a readout system, the output noise arises from multiple internal noise sources, each shaped by a different transfer function to the output. For comparison and design purposes, it is convenient to refer all noise contributions to the input of the circuit, defining an equivalent noise source at the input that would produce the same output noise as the actual circuit [33]. This input-referred noise directly sets the minimum detectable signal and is therefore the primary figure of merit for any readout front-end. In general, the input-referred noise of a two-port circuit is fully characterized by a series voltage source and a shunt current source at the input [33], which together account for all internal noise contributions regardless of the source impedance.

2.1.4 Noise Analysis Procedure

Analyzing noise in a circuit requires determining how the noise generated by each individual component contributes to the total noise observed at the output. The standard procedure consists of the following steps [33]:

1. Each noisy element is replaced by its noiseless equivalent in series or parallel with an appropriate noise source, according to the models presented in Section 2.2.

2. The transfer function from each noise source to the output is computed independently, treating each noise source as a deterministic signal with all other noise sources set to zero.

3. The output noise PSD contributed by each source is calculated using (2.1): the noise PSD of the source is multiplied by the squared magnitude of its transfer function to the output.

4. Since noise sources in a circuit are generally uncorrelated, the individual output noise PSDs are summed to yield the total output noise PSD.

5. The total output noise is finally referred back to the input by dividing by the squared magnitude of the signal transfer function, giving the input-referred noise PSD that directly characterizes the resolution of the readout system.

2.2 Fundamental Noise Sources

Four fundamental noise mechanisms are relevant to CMOS low-current readout systems. Each has a distinct physical origin, frequency dependence, and dependence on operating conditions, as reviewed in the following subsections.

2.2.1 Thermal Noise

Thermal noise, also known as Johnson–Nyquist noise, arises from the random thermal agitation of charge carriers in any resistive element in thermal equilibrium. It is present in all resistors and in the conductive channel of MOS transistors across all regions of operation, from strong to weak inversion, although its spectral character differs depending on the operating regime, as discussed in the following.

Resistor

For a resistance R at absolute temperature T, the open-circuit thermal noise voltage PSD is [33]:

$$S_v(f) = 4k_BTR \qquad [\mathrm{V}^2/\mathrm{Hz}] \tag{2.4}$$

where $k_B = 1.381 \times 10^{-23}\,\mathrm{J/K}$ is Boltzmann's constant. Equivalently, modeling the noisy resistor as a noiseless element in parallel with a current noise source:

$$S_i(f) = \frac{4k_BT}{R} \qquad [\mathrm{A}^2/\mathrm{Hz}] \tag{2.5}$$

Thermal noise is *white*—its PSD is independent of frequency—and is fully determined by R and T. At room temperature, a resistance of $1\mathrm{G}\Omega$ produces a current noise density of approximately $4\,\mathrm{fA}/\sqrt{\mathrm{Hz}}$, illustrating why very large feedback resistances are required to achieve sub-pA noise floors in resistive-feedback TIAs.

MOSFET Channel

In a MOSFET, the conductive channel can be treated as a distributed resistive element. A general expression for the channel thermal noise is derived by considering an elementary section of the channel of length dx at position x, which has a resistance [34]:

$$dR = \frac{dV_{ch}}{I_D} = \frac{dx}{W\,\mu_n\,(-Q'_{inv})} \tag{2.6}$$

where μ_n is the carrier mobility, W is the channel width, and Q'_{inv} is the mobile inversion charge density per unit area. This elementary resistance produces a local thermal noise voltage with PSD $dS_{\Delta V_{ch}} = 4k_BT\,dR$, which results in a drain current noise PSD:

$$dS_{\Delta I_D} = g_{ch}^2 \cdot dS_{\Delta V_{ch}} = 4k_BT\,\frac{\mu_n}{L^2}\,W\,(-Q'_{inv})\,dx \tag{2.7}$$

where $g_{ch} = \mu_n(W/L)(-Q'_{inv})$ is the local channel conductance. Integrating (2.7) from source to drain yields the total drain current noise PSD, expressed in terms of a thermal noise conductance G_{Nth} [34]:

$$S_{\Delta I_D} = 4k_BT\,G_{Nth} \tag{2.8}$$

$$G_{Nth} = \frac{\mu_n}{L^2}\int_0^L W\,(-Q'_{inv})\,dx = \frac{\mu_n}{L^2}\,|Q_{inv}| \tag{2.9}$$

where $|Q_{inv}|$ is the total mobile inversion charge in the channel. Since no assumption has been made on the mode of operation, (2.9) is valid from weak to strong inversion, including the moderate inversion region [34].

Strong inversion. In strong inversion in saturation ($I_R \approx 0$), G_{Nth} reduces to [33, 34]:

$$G_{Nth} = \frac{2}{3}\,g_{ms} \tag{2.10}$$

where g_{ms} is the source transconductance. The noise factor γ is defined as $\gamma = G_{Nth}/g_m$, which gives $\gamma = 2n/3$ for long-channel devices in saturation, where n is the slope factor [34]. For $n \approx 1$, this yields the well-known result $\gamma \approx 2/3$ [33].

Weak inversion (subthreshold). In weak inversion, current transport occurs by diffusion of carriers over a potential barrier rather than by drift through a resistive channel. The thermal noise conductance in this regime becomes [34, 35]:

$$G_{Nth} = \frac{1}{2}(g_{ms} + g_{md}) = \frac{I_F + I_R}{2V_{th}} \tag{2.11}$$

where $g_{ms} = -\partial I_D/\partial V_S$ and $g_{md} = \partial I_D/\partial V_D$ are the source and drain transconductances, I_F and I_R are the forward and reverse current components, and $V_{th} = k_BT/q$ is the thermal voltage. The total drain current noise PSD remains thermal in nature, given by $S_{\Delta I_D} = 4k_BT\,G_{Nth}$, which upon substituting (2.11) yields:

$$S_{\Delta I_D} = 4k_BT \cdot \frac{I_F + I_R}{2V_{th}} = 2q\,(I_F + I_R) \tag{2.12}$$

In saturation ($I_R \approx 0$), this simplifies to:

$$S_{\Delta I_D} = 2q\, I_D \qquad \text{(weak inversion, saturation)} \tag{2.13}$$

It is important to note that the noise source remains thermal throughout all regions of operation. The expression $2q(I_F + I_R)$ arises as a mathematical consequence of evaluating $4k_BT\, G_{Nth}$ in the weak inversion limit—not as a physical transition to shot noise [34, 36]. An alternative interpretation in the literature describes this result as arising from two-sided shot noise due to forward and reverse diffusion currents across the channel barrier [36], emphasizing that stochastic carrier transport underlies both barrier-crossing fluctuations and channel-scattering events. While the two perspectives differ in their physical emphasis, they yield the same mathematical expression and are therefore consistent in their predictions of the noise power spectral density. The transition from strong to weak inversion is continuous and described by the EKV model interpolation function [34].

2.2.2 Flicker Noise

Flicker noise, commonly referred to as $1/f$ noise, is a low-frequency excess noise present in all active devices. In MOSFETs, it originates from the random trapping and release of charge carriers at defect states located at the Si–SiO_2 interface and within the gate oxide, causing fluctuations in the threshold voltage and hence in the drain current [33]. The PSD of the gate-referred flicker noise voltage is:

$$S_{v,1/f}(f) = \frac{K_f}{C_{ox}\, W\, L\, f} \qquad [\mathrm{V}^2/\mathrm{Hz}] \tag{2.14}$$

where K_f is a process-dependent flicker noise coefficient, C_{ox} is the gate oxide capacitance per unit area, and W and L are the transistor width and length, respectively [33, 37]. The factor K_f is strongly process-dependent; PMOS transistors generally exhibit lower K_f than NMOS devices due to buried channel conduction, which reduces the influence of interface traps, and are therefore preferred for low-noise input stages [33]. Increasing the gate area WL reduces the flicker noise contribution, at the cost of increased input capacitance.

2.2.3 Shot Noise

Shot noise arises from the discrete, statistically independent nature of charge carrier transport across a potential barrier. Unlike thermal noise, which reflects equilibrium fluctuations in a resistive medium, shot noise is a non-equilibrium phenomenon associated with the random arrival of discrete charge carriers crossing a barrier. It is the dominant noise mechanism in reverse-biased pn junctions and in any device where current transport occurs by diffusion across a potential barrier rather than by drift through a resistive channel. For a steady-state current I crossing such a barrier, the one-sided shot noise PSD is [33]:

$$S_i(f) = 2qI \qquad [\mathrm{A}^2/\mathrm{Hz}] \tag{2.15}$$

where q is the elementary charge. Shot noise is white and scales linearly with I. At very low current levels, the shot noise density becomes extremely small: for a current of 1 pA, $\sqrt{S_i} = \sqrt{2qI} \approx 0.57\,\mathrm{fA}/\sqrt{\mathrm{Hz}}$, substantially below the thermal current-noise density of a 1GΩ resistor at room temperature. This property makes devices whose noise is governed by shot noise at low currents—such as reverse-biased pn junctions—highly attractive as low-noise elements in current readout circuits.

2.2.4 kT/C Noise

kT/C noise, also referred to as reset noise or sampling noise, arises when a capacitor is charged or discharged through a resistive switch. During the switching phase, the switch resistance R_{sw} connects a capacitor C to a reference potential. The thermal noise of R_{sw} is low-pass filtered by the R_{sw}–C network and integrated over all frequencies, yielding a total stored voltage noise variance [38]:

$$\overline{v_n^2} = \int_0^\infty \frac{4k_BTR_{sw}}{1+(2\pi f R_{sw}C)^2}\,df = \frac{k_BT}{C} \qquad [\mathrm{V}^2] \tag{2.16}$$

This result is independent of R_{sw}: regardless of the switch resistance, the noise energy stored on C after each switching event is always k_BT/C. A larger capacitance therefore reduces the kT/C noise, while a smaller capacitance increases it. This mechanism is particularly relevant in sampled-data circuits and discrete-time readout architectures, where it represents a fundamental noise floor that cannot be reduced by slowing down the switching operation.

2.3 Noise in Transimpedance Amplifiers

As reviewed in Section 1.3, transimpedance amplifiers (TIAs) are by far the most widely adopted topology for the first stage of analog front-ends (AFEs) in current readout systems, owing to their straightforward implementation and favorable noise–bandwidth trade-off. Generally, a TIA is a current-to-voltage converter comprising an op-amp with a feedback element Z_f connected between its output and inverting input, as illustrated in Fig. 2.1(a). The non-inverting input is maintained at a fixed reference potential, while the inverting input receives the current to be measured, I_{in}. A capacitance C_{in} is present at the inverting input node, which in practice includes the input capacitance of the op-amp and any parasitic capacitances at the input node. Due to negative feedback, this node behaves as a virtual ground, forcing the entire input current to flow through the feedback impedance Z_f. The resulting voltage drop across Z_f produces the output voltage V_{out}, yielding a transimpedance gain of:

$$\frac{V_{out}}{I_{in}} = -Z_f \tag{2.17}$$

Depending on the nature of Z_f, TIA implementations are broadly classified into two categories: capacitive feedback and resistive feedback, as illustrated in Fig. 2.1(a).

The resistive feedback category encompasses both passive resistors and MOS-based pseudo-resistors (PRs).

To establish a unified noise analysis framework applicable to both feedback topologies, the feedback impedance Z_f is modeled as a resistance R_f in parallel with a capacitance C_f:

$$Z_f(s) = \frac{R_f}{1 + sR_fC_f} \tag{2.18}$$

This general model encompasses both topologies as limiting cases: in the capacitive-feedback TIA, R_f is effectively infinite, reducing Z_f to a pure capacitor C_f; in the resistive-feedback TIA, C_f represents the unavoidable stray capacitance in parallel with R_f.

The primary noise sources in this general TIA model are illustrated in Fig. 2.1(b): the current noise of the feedback element $\overline{i_f^2}$, and the intrinsic input-referred voltage noise of the op-amp $\overline{e_{op}^2}$. To evaluate the total input-referred noise, $\overline{e_{op}^2}$ is referred to the input as an equivalent current noise $\overline{i_{op}^2}$ through the impedances present at the inverting input node. Since the input capacitance C_{in} presents an impedance $Z_{in} = 1/j\omega C_{in}$, this conversion yields:

$$\overline{i_{op}^2} = \overline{e_{op}^2} \left| \frac{1 + Z_f/Z_{in}}{Z_f} \right|^2 = \overline{e_{op}^2} \left[\frac{1}{R_f^2} + \omega^2 \left(C_{in} + C_f \right)^2 \right] \tag{2.19}$$

where $\omega = 2\pi f$ is the angular frequency. The first term represents the low-frequency contribution governed by the feedback resistance R_f, while the second term reflects the high-frequency contribution growing as $(2\pi f)^2$ and scaled by the total capacitance $(C_{in} + C_f)$ at the input node. The total input-referred current noise of the TIA is then:

$$\overline{i_{n,\mathrm{TIA}}^2} = \overline{i_f^2} + \overline{i_{op}^2} = \overline{i_f^2} + \overline{e_{op}^2} \left[\frac{1}{R_f^2} + (2\pi f)^2 \left(C_{in} + C_f \right)^2 \right] \tag{2.20}$$

The current noise $\overline{i_f^2}$ is directly injected into the TIA input and depends on the type and conduction mechanism of the feedback element. Depending on whether the feedback is capacitive or resistive, the magnitude and spectral composition of this noise contribution differ significantly. The intrinsic voltage noise of the op-amp is dominated by the input differential pair and consists of both thermal and flicker components [20]:

$$\overline{e_{op}^2} = \frac{16kT}{g_m} + \frac{2K_f}{C_{ox}WL} \cdot \frac{1}{f} \tag{2.21}$$

Defining $\overline{e_{op,th}^2} = 16kT/g_m$ and $\overline{e_{op,fl}^2} = 2K_f/C_{ox}WL$ as the thermal and flicker noise coefficients of the op-amp, respectively, (2.21) can be written compactly as:

$$\overline{e_{op}^2} = \overline{e_{op,th}^2} + \frac{\overline{e_{op,fl}^2}}{f} \tag{2.22}$$

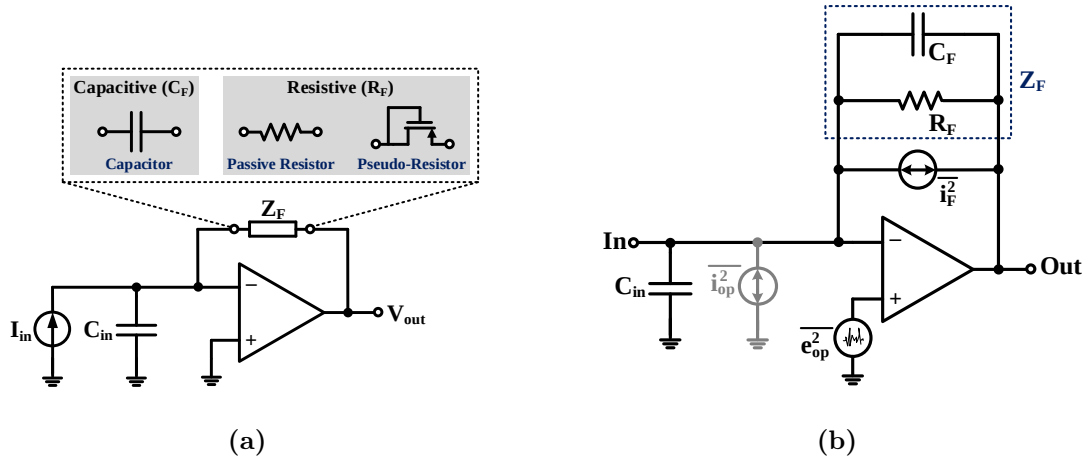


Figure 2.1: (a) General TIA configuration with feedback impedance Z_f. The feedback element is implemented either as a capacitor C_f (capacitive feedback) or as a resistor R_f (resistive feedback). C_{in} represents the total capacitance at the inverting input node. (b) Noise model of the TIA with general feedback impedance $Z_f = R_f \| C_f$, showing the feedback element current noise $\overline{i_f^2}$ and the op-amp input-referred voltage noise $\overline{e_{op}^2}$.

Similarly, the feedback element noise is decomposed into thermal and flicker components as:

$$\overline{i_f^2} = \overline{i_{f,th}^2} + \frac{\overline{i_{f,fl}^2}}{f} \tag{2.23}$$

Substituting (2.22) and (2.23) into (2.20) and separating the dominant frequency-dependent terms yields:

$$\begin{aligned}\overline{i_{n,\mathrm{TIA}}^2}(f) = &\underbrace{\left(\overline{i_{f,fl}^2} + \frac{\overline{e_{op,fl}^2}}{R_f^2}\right) f^{-1}}_{\text{flicker noise}} + \underbrace{\left(\overline{i_{f,th}^2} + \frac{\overline{e_{op,th}^2}}{R_f^2}\right)}_{\text{white noise}} \\ &+ \underbrace{\overline{e_{op,fl}^2}(2\pi)^2(C_{in}+C_f)^2\, f}_{\text{capacitive noise } (\propto f)} + \underbrace{\overline{e_{op,th}^2}(2\pi)^2(C_{in}+C_f)^2\, f^2}_{\text{capacitive noise } (\propto f^2)}\end{aligned} \tag{2.24}$$

The feedback path plays a crucial role in shaping the overall noise characteristics of the TIA. It directly contributes noise through $\overline{i_f^2}$—primarily flicker and white noise—but also governs how $\overline{e_{op}^2}$ propagates to the input. At low frequencies, the components of $\overline{e_{op}^2}$ are attenuated by R_f without frequency shaping, appearing as additional flicker and white noise contributions. At higher frequencies, they are modulated by $(C_{in} + C_f)$, giving rise to the frequency-rising capacitive noise terms. As illustrated in Fig. 2.2, this results in four distinct noise regions: a f^{-1} flicker region at low frequencies, a white noise floor at intermediate frequencies, and capacitive noise growing as f and f^2 at high frequencies. The f^2 dependence highlights the critical role of minimizing the total input capacitance $(C_{in} + C_f)$ in achieving low noise at high measurement bandwidths.

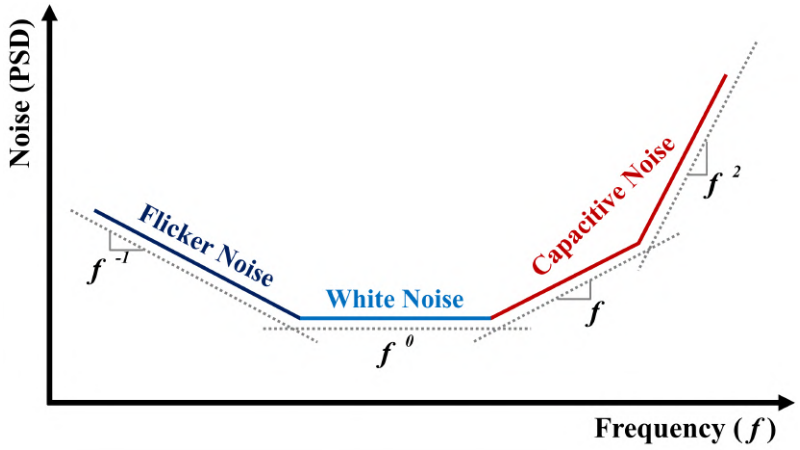


Figure 2.2: Typical input-referred current noise PSD of a TIA, showing the four frequency-dependent noise regions corresponding to the terms in (2.24).

Consequently, to minimize the input-referred noise of the TIA, the feedback element must satisfy two key requirements:

1. Contribute minimal direct noise $\overline{i_f^2}$ at the input.
2. Provide a high resistive component R_f, to suppress the low-frequency noise contributions, while introducing a minimal capacitive component C_f, to limit the high-frequency capacitive noise rise.

Additional noise reduction can be achieved by minimizing C_{in} and $\overline{e_{op}^2}$, as both significantly influence the high-frequency noise performance. While C_{in} can be reduced through monolithic integration of the sensor and readout circuit, lowering $\overline{e_{op}^2}$ requires careful op-amp design with low-noise input stages. However, in CMOS implementations, this often comes at the expense of increased transistor area and consequently higher input capacitance, which counteracts efforts to minimize C_{in}. These requirements directly point to the feedback element as the most critical design choice in a low-noise TIA, motivating a careful examination of the noise behavior of each feedback topology, as presented in the following subsections.

2.3.1 Capacitive-Feedback TIA

Recalling the two key requirements established in the previous section—minimal direct noise $\overline{i_f^2}$ and high R_f with minimal C_f—capacitive feedback appears, at first glance, to be an attractive candidate. An ideal capacitor contributes neither thermal nor flicker noise, satisfying the first requirement by setting $\overline{i_f^2} = 0$. Furthermore, since $R_f \to \infty$ for a pure capacitor, the term $1/R_f^2$ in (2.20) vanishes, and the total input-referred current noise simplifies to:

$$\overline{i_{n,\mathrm{TIA}}^2}(f) = \overline{e_{op}^2}\,(2\pi f)^2\,(C_{in} + C_f)^2 \tag{2.25}$$

This result confirms the fundamental noise advantage of capacitive feedback: the noise is governed entirely by the op-amp voltage noise $\overline{e_{op}^2}$ converted through the

total input capacitance ($C_{in} + C_f$), with no white noise floor and no flicker noise contribution from the feedback element itself.

Reducing C_f lowers the high-frequency capacitive noise; however, it simultaneously increases the transimpedance gain. In the capacitive-feedback TIA, the input current charges C_f over an integration interval T_{int}, producing an output voltage ramp with a gain of T_{int}/C_f. A smaller C_f therefore results in a higher gain, causing the output to ramp more rapidly for a given input current and reach saturation sooner, thereby limiting the maximum measurable current and reducing the dynamic range of the readout system. Conversely, increasing C_f extends the dynamic range at the cost of a higher noise floor. This fundamental trade-off between noise and dynamic range is an inherent constraint of the capacitive-feedback topology.

To prevent output saturation, either a periodic reset operation or a DC-servo feedback loop must be employed. In the reset approach, discharging the feedback capacitor through the reset switch introduces kT/C_f noise, adding an input-referred charge noise of $\overline{Q_n^2} = k_B T C_f$ at each reset event. Notably, this noise is independent of the switch resistance and cannot be eliminated by slowing down the reset. Alternatively, a DC-servo feedback loop can be used to continuously discharge C_f, avoiding the discrete reset; however, the additional feedback element introduced by the servo loop contributes further noise sources at the TIA input.

2.3.2 Resistive-Feedback TIA

In the resistive-feedback TIA, the feedback element is primarily a resistance R_f with an unavoidable stray capacitance C_f in parallel. A straightforward approach to realizing this is the use of a passive ohmic resistor. When a passive resistor R_f is employed as the feedback element, its direct noise contribution is primarily thermal, $\overline{i_f^2} \approx \overline{i_{f,th}^2} = 4k_B T/R_f$. A minimal flicker noise component may also be present depending on the resistor technology and layout, but is generally negligible for passive resistors. Substituting into (2.20), the total input-referred current noise becomes:

$$\overline{i_{n,\mathrm{TIA}}^2}(f) = \frac{4k_B T}{R_f} + \overline{e_{op}^2}\left[\frac{1}{R_f^2} + (2\pi f)^2 (C_{in} + C_f)^2\right] \tag{2.26}$$

A high-value R_f is therefore desirable to reduce the thermal noise floor and to attenuate the op-amp voltage noise contribution at low frequencies. However, increasing R_f introduces several critical challenges:

1. Larger resistors inherently exhibit greater parasitic capacitance C_f, which further restricts the TIA bandwidth and exacerbates the high-frequency capacitive noise.

2. Integrating high-value resistors in standard CMOS technology is challenging due to physical limitations on doping levels. The achievable sheet resistance typically ranges from a few $\Omega/\square$ to several $\mathrm{k}\Omega/\square$, forcing high-value resistors to occupy substantial silicon area through long and often folded geometries, leading to increased chip size and cost.

These limitations motivate the use of MOS-based PRs as an integrated alternative.

MOS-Based Pseudo-Resistors

To overcome the integrability limitation of passive resistors, MOS-based PRs have been widely adopted in integrated TIA designs. A PR is realized from one or more MOSFET devices biased in the subthreshold region, where the exponential I–V characteristic results in a very large equivalent small-signal resistance—reaching GΩ to TΩ values—within a compact CMOS layout.

The simplest PR implementation employs a PMOS transistor in a transdiode connection, formed by shorting its gate and drain terminals [30]. The gate potential is stabilized by the op-amp virtual ground, while the source voltage varies in response to the input current I_{in}, thereby determining the TIA output. The input current thus modulates the source-gate voltage V_{SG}, dynamically biasing the feedback transistor. Since the gate and drain are shorted, the condition $V_{SG} = V_{SD}$ holds throughout operation.

For low input current levels where V_{SG} remains below the absolute threshold voltage $|V_T|$, the transistor operates in the subthreshold (weak inversion) region. In this regime, the inversion layer beneath the gate is only weakly formed, and the drain current arises primarily from the diffusion of minority carriers across the channel, driven by carrier concentration gradients between source and drain. A non-negligible drift component is also present due to the longitudinal electric field along the channel. The combined diffusion-drift subthreshold current is given by [34]:

$$I_{SD} = I_{SD0}\, e^{(V_{SG}-|V_T|)/nV_{th}} \left(1 - e^{-V_{SD}/V_{th}}\right) \tag{2.27}$$

where I_{SD0} is a pre-factor dependent on process parameters and transistor geometry, and n is the subthreshold slope factor. As I_{in} decreases and V_{SG} drops further below $|V_T|$, the transistor transitions deeper into weak inversion and the current decreases exponentially. For input current levels where $V_{SG} > |V_T|$, the transistor enters saturation, as the condition $V_{SD} > V_{SG} - |V_T|$ is always satisfied in the transdiode configuration.

The small-signal equivalent resistance of the PR corresponds to the resistive component R_f of the feedback network. With $V_{SG} = V_{SD}$ and assuming $n = 1$ and $V_{SD} \gg V_{th}$ such that $(1 - e^{-V_{SD}/V_{th}}) \approx 1$, the equivalent resistance r_{PR} is obtained as [30]:

$$R_f = r_{PR} = \left(\frac{\partial I_{SD}}{\partial V_{SD}}\right)^{-1} \approx \frac{V_{th}}{I_{SD0}}\, e^{(|V_T|-V_{SD})/V_{th}} \tag{2.28}$$

At $V_{SD} \approx 0$, this simplifies to the maximum equivalent resistance:

$$r_{PR} \approx \frac{V_{th}}{I_{SD0}} \tag{2.29}$$

As V_{SD} increases within the subthreshold region ($0 < V_{SD} < |V_T|$), r_{PR} decreases exponentially. Nevertheless, throughout this operating range the equivalent resistance remains significantly large, enabling the PMOS transistor in weak inversion to effectively emulate a high-value resistor within a compact CMOS layout.

The above analysis applies symmetrically to a complementary NMOS PR. To extend bidirectional operation and improve linearity, an NMOS transistor configured identically can be placed in parallel with the PMOS, forming a complementary PR pair [31]. Each transistor handles one polarity of the input current, and the combined structure maintains a high equivalent resistance across a wider signal range.

The noise contribution of a MOS-based PR consists of two components. As established in Section 2.2.1, a MOSFET biased in the subthreshold region exhibits a channel thermal noise that evaluates to $2qI_{SD}$, per (2.13). In addition, flicker noise in the feedback transistor becomes significant, particularly at low frequencies and extremely low current levels. As discussed in Section 2.2.2, this noise is commonly modeled as a voltage noise source in series with the gate terminal. Since the gate is shorted to the drain and connected to the inverting input of the op-amp, this flicker voltage noise is directly reflected at the TIA input as an equivalent current noise. The total noise injected by the PR into the TIA input is therefore:

$$\overline{i_f^2} = \frac{K_f}{C_{ox}\, W\, L\, r_{PR}^2\, f} + 2q\, I_{SD} \tag{2.30}$$

The first term is the flicker noise contribution of the feedback transistor referred to the input, and the second term is the white thermal noise of the subthreshold channel current. Substituting into (2.20), the total input-referred current noise of the PR-feedback TIA becomes:

$$\begin{aligned}\overline{i_{n,\mathrm{TIA}}^2}(f) = {} & \frac{K_f}{C_{ox}\, W\, L\, r_{PR}^2\, f} + 2q\, I_{in,dc} \\ & + \overline{e_{op}^2}\left[\frac{1}{r_{PR}^2} + (2\pi f)^2\,(C_{in} + C_f)^2\right]\end{aligned} \tag{2.31}$$

where $I_{in,dc} = I_{SD}$ denotes the average input current flowing through the feedback network. At low input current levels, the high equivalent resistance r_{PR} strongly suppresses both the flicker noise and the low-frequency contribution of $\overline{e_{op}^2}$, since both terms scale as $1/r_{PR}^2$. The shot noise term $2qI_{in,dc}$ also remains negligibly small at pA current levels. Furthermore, since the transimpedance gain is set by r_{PR} independently of C_f, the stray capacitance C_f can be minimized to suppress the high-frequency capacitive noise without incurring the dynamic range penalty inherent to the capacitive-feedback topology.

2.4 DC-Compensated Transimpedance Amplifiers

Both the capacitive-feedback and resistive-feedback TIA topologies analyzed in the preceding sections share a common limitation: in the presence of a large DC baseline current—such as the ionic offset current inherent to nanopore sensing—the output of the TIA is driven toward saturation, severely restricting the available dynamic range for the AC signal components of interest. To address this limitation, a DC-compensation approach is commonly employed.

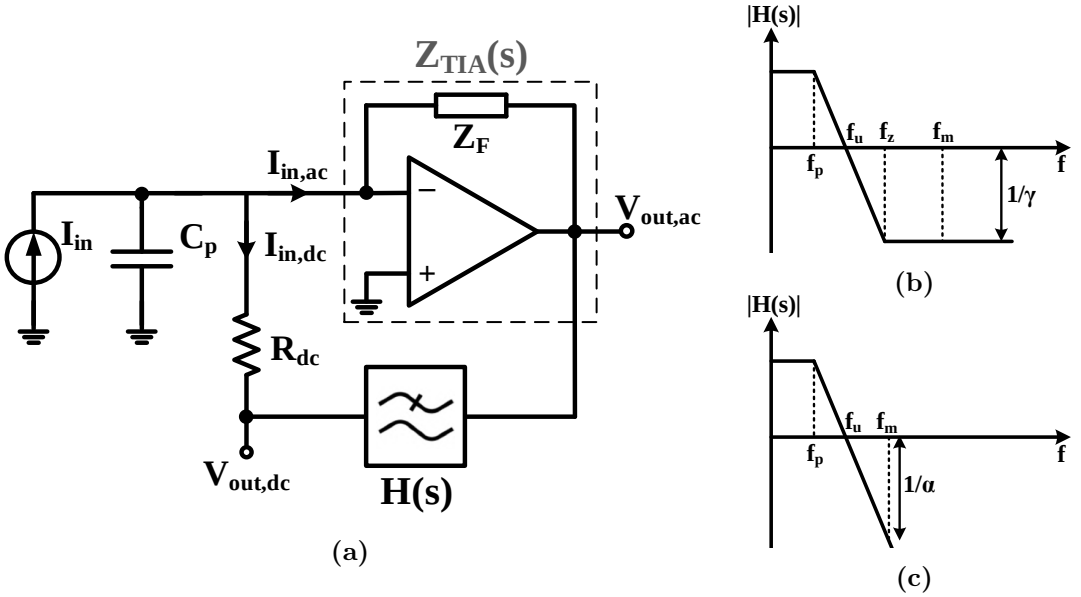


Figure 2.3: Conceptual representation of a DC-compensated TIA: (a) general architecture showing the TIA core $Z_{\mathrm{TIA}}(s)$, compensation resistor R_{dc}, and low-pass filter $H(s)$; and example realizations of $H(s)$ for (b) capacitive-feedback TIA cores and (c) resistive-feedback TIA cores.

The general architecture of a DC-compensated TIA is illustrated in Fig. 2.3(a), in which an additional low-frequency feedback loop, commonly referred to as a DC-servo loop, continuously monitors the TIA output and extracts its slowly varying DC component through a low-pass transfer function $H(s)$. The filtered signal is then converted into a compensation current through the resistor R_{dc} and injected back into the TIA input node, progressively cancelling the DC baseline component of the input current until steady-state equilibrium is reached. While the DC and low-frequency components of the input current ($I_{in,dc}$) are handled by the DC-servo loop, the loop becomes effectively inactive for frequencies above its unity-gain frequency f_m. Consequently, the AC components of the input current ($I_{in,ac}$) propagate through the TIA core and are converted to an output voltage through its feedback impedance Z_f, effectively decoupling the DC and AC signal paths. However, the introduction of the DC-servo loop inevitably gives rise to trade-offs among noise performance, dynamic range, and loop stability, which are analyzed in the following subsections.

2.4.1 Dynamic Range

Since the DC and AC components of the input current are processed through separate signal paths, the TIA exhibits distinct dynamic range limits for each. Both paths share the same output voltage swing $V_{out,max}$, determined by the supply voltage and the op-amp output stage. The maximum DC current that can be absorbed

by the DC-servo loop is set by the compensation resistor R_{dc}:

$$I_{in,dc,max} = \frac{V_{out,max}}{R_{dc}} \tag{2.32}$$

The maximum AC current that can be processed without driving the TIA core into saturation is limited by the feedback impedance Z_f:

$$I_{in,ac,max} = \frac{V_{out,max}}{|Z_f|} \tag{2.33}$$

Since the DC-servo loop maintains the TIA output close to its nominal operating point by cancelling $I_{in,dc}$, the full output swing $V_{out,max}$ remains available for AC signal excursions regardless of the DC baseline level, thereby extending the effective dynamic range of the readout system.

2.4.2 Noise

The adoption of DC compensation inevitably introduces additional noise contributions at the TIA input. The total input-referred current noise density of the system is the sum of two components:

$$\overline{i_{n,in}^2} = \overline{i_{n,\mathrm{TIA}}^2} + \overline{i_{n,\mathrm{DC}}^2} \tag{2.34}$$

where $\overline{i_{n,\mathrm{TIA}}^2}$ represents the intrinsic noise of the TIA core as analyzed in (2.20), while $\overline{i_{n,\mathrm{DC}}^2}$ accounts for the additional noise introduced by the DC-servo loop. Referring to Fig. 2.3(a), the noise injected by the servo loop arises from two sources: the thermal noise of R_{dc}, and the TIA output voltage noise $\overline{v_{n,\mathrm{out}}^2}$ filtered by $H(s)$ and converted to a current through R_{dc}. The DC-servo loop noise contribution is therefore:

$$\overline{i_{n,\mathrm{DC}}^2} = \frac{4k_BT}{R_{dc}} + \overline{v_{n,\mathrm{out}}^2}\frac{|H(s)|^2}{R_{dc}^2} \tag{2.35}$$

The first term is the thermal noise of the compensation resistor R_{dc}, and the second term represents the TIA output voltage noise referred to the input through the DC-servo loop.

2.4.3 Stability

The DC-servo loop forms a closed-loop system around the TIA core. From the architecture shown in Fig. 2.3(a), the loop gain can be derived by tracing the signal path from the TIA input, through the TIA core with transimpedance $Z_{\mathrm{TIA}}(s)$, through the filter $H(s)$, and back to the input via the compensation resistor R_{dc}. This yields:

$$G_{\mathrm{loop}}(s) = -Z_{\mathrm{TIA}}(s)\,\frac{H(s)}{R_{dc}} \tag{2.36}$$

The negative sign reflects the inverting nature of the TIA core, which together with the sign convention of the compensation current injection ensures negative feedback

under normal operating conditions. The stability of the DC-servo loop is therefore governed by the combined magnitude and phase characteristics of $Z_{\mathrm{TIA}}(s)$ and $H(s)$. For stable operation, the loop gain must satisfy the Bode stability criterion: the phase of $G_{\mathrm{loop}}(s)$ must not reach $-180°$ before the loop gain magnitude falls below unity. Consequently, the interaction between the poles and zeros of $Z_{\mathrm{TIA}}(s)$ and $H(s)$ directly determines the achievable phase margin and must be carefully accounted for in the design of $H(s)$, as discussed in Section 2.4.4.

2.4.4 Design Considerations

The analysis presented above highlights two key requirements for the design of $H(s)$:

1. $H(s)$ must provide sufficiently high gain at very low frequencies to accurately track and cancel DC variations at the TIA output. By maintaining the output voltage close to its nominal operating point, the DC-servo loop preserves the available voltage headroom for AC excursions and thereby retains the effective AC dynamic range in the presence of large baseline currents.

2. $H(s)$ must strongly attenuate higher frequencies to prevent AC components of the TIA output from being fed back to the input through the DC-servo path. This attenuation also suppresses the second term in (2.35), reducing the noise contribution of the DC-servo loop within the signal band.

In terms of stability, additional constraints on the design of $H(s)$ arise from the configuration of the TIA core. Assuming an ideal op-amp, the frequency response of the TIA core is primarily defined by its feedback impedance Z_f. Consequently, the loop gain behavior in (2.36) strongly depends on the feedback topology. How these requirements are met in practice is examined separately for C-TIA and R-TIA cores in the following.

C-TIA core. The transfer function of a C-TIA core can be approximated as $Z_{\mathrm{TIA}}(s) \approx 1/(sC_f)$, indicating integrator behavior with a pole at the origin. This introduces an inherent $-90°$ phase lag in the DC-servo loop. To maintain adequate phase margin at the unity-gain frequency f_m, the filter $H(s)$ must contribute less than $45°$ of additional phase lag up to this frequency. As shown in Fig. 2.3(b), $H(s)$ is therefore designed with a pole at f_p, a unity-gain frequency f_u, and a compensating zero at f_z placed above f_u to partially offset the integrator phase lag [28]. Since phase recovery occurs gradually over frequency, the zero f_z must be located sufficiently below f_m to ensure that adequate phase margin is restored before the crossover frequency. Furthermore, f_z must be positioned above f_u to ensure effective attenuation of AC components by a constant factor γ. Under these conditions, the unity-gain frequency of the DC-servo loop is given by:

$$f_m = \frac{1}{2\pi C_f R_{dc}\,\gamma} \tag{2.37}$$

Reducing f_m is typically desirable, as it extends the AC passband toward lower frequencies. However, achieving very small values of f_m becomes challenging due to the tight frequency-separation constraints imposed on f_p, f_u, f_z, and f_m. Consequently, the choice of C_f and R_{dc} must be carefully balanced to obtain an optimized value of f_m.

The values of C_f and R_{dc} also introduce further design trade-offs. The value of C_f directly affects both the noise performance and the dynamic range of the TIA core. A smaller C_f improves the high-frequency noise performance per (2.20), but it also increases the transimpedance gain $1/(sC_f)$ at low frequencies, thereby reducing the maximum allowable AC input current before saturation. For this reason, practical implementations often employ switchable C_f architectures [39], allowing a trade-off between noise performance and dynamic range while maintaining stable operation. On the other hand, increasing R_{dc} reduces the noise contribution of the DC-servo loop per (2.35), but may adversely affect stability by lowering f_m. A common mitigation strategy is to maintain the product $R_{dc}\,\gamma$ approximately constant, thereby stabilizing f_m and preserving consistent loop dynamics across operating conditions [39].

R-TIA core. The transfer function of an R-TIA core can be expressed as $Z_{\mathrm{TIA}}(s) \approx R_f/(1 + sR_fC_f)$. When the pole $1/(2\pi R_fC_f)$ is placed well above f_m, the transimpedance approximates to its low-frequency value R_f. Unlike C-TIA cores, the R-TIA does not introduce an inherent phase lag at low frequencies. Consequently, as shown in Fig. 2.3(c), $H(s)$ can be implemented as a simple single-pole low-pass filter. In this case, the overall phase lag at the crossover frequency is dominated by the single pole of $H(s)$, yielding a phase margin close to 90° and ensuring stable operation. The loop crossover frequency f_m is determined by:

$$|H(f_m)| = \frac{R_{dc}}{R_f} = \frac{1}{\alpha} \tag{2.38}$$

where $\alpha = R_f/R_{dc} > 1$ must be satisfied to ensure effective attenuation above f_m. The magnitude of $H(s)$ decreases progressively with frequency, ensuring effective attenuation of signal components beyond the signal band.

Comparison and Design Implications. Table 2.1 summarizes the key design trade-offs between C-TIA and R-TIA cores in the context of DC-compensated readout systems. C-TIAs are particularly attractive because the feedback capacitor contributes no thermal noise, reducing the intrinsic TIA noise to $\overline{e_{op}^2}(2\pi f)^2(C_{in} + C_f)^2$. However, implementing DC compensation in C-TIAs requires a delicate balance among f_m, C_f, and R_{dc} to simultaneously optimize noise performance, dynamic range, and loop stability. Furthermore, due to the integrative behavior of the C-TIA core, an additional differentiator stage is typically required to flatten the AC frequency response [28], increasing system complexity. In contrast, DC compensation in an R-TIA enables a simpler DC-servo loop design with relaxed stability constraints, as illustrated by the comparison between Fig. 2.3(b) and 2.3(c). These observations motivate the architecture presented in Chapter 3, which combines the

Table 2.1: Comparison of DC-compensated C-TIA and R-TIA cores.

Property	**C-TIA**	**R-TIA**
Feedback element noise	None (ideal C_f)	White + flicker
Op-amp noise contribution	$\propto f^2$	White + $\propto f^2$
Inherent phase lag	$-90°$ (integrator)	None
$H(s)$ complexity	Pole, zero, crossover	Single pole
Phase margin	Requires compensation	$\approx 90°$
C_f trade-off	Noise vs dynamic range	Stray only
Additional stage required	Differentiator	None

favorable stability characteristics of R-TIAs with a feedback element that achieves a noise floor comparable to capacitive feedback.

Chapter 3

Proposed Current Readout

As established in Chapter 2, the noise performance of a continuous-time TIA is fundamentally limited by the feedback element. In resistive-feedback implementations based on passive resistors, the thermal noise floor constrains the minimum achievable input-referred current noise. In pseudo-resistor-based designs, additional flicker noise and sensitivity to bias conditions further compromise performance. Capacitive-feedback architectures eliminate feedback element noise but introduce a fundamental trade-off between noise and dynamic range, requiring periodic reset or DC compensation. This chapter presents two original contributions that address these limitations. The first is a novel continuous-time TIA exploiting the intrinsic drain–bulk PN junction of a MOSFET as the feedback element, achieving a noise floor governed exclusively by junction transport while maintaining compatibility with standard CMOS technology and reset-free operation. The second extends this TIA core with a dedicated DC-servo loop that absorbs the large DC baseline current inherent to nanopore sensing, enabling wide dynamic range operation while preserving the low-noise properties of the core.

3.1 TIA with MOSFET PN-Junction Feedback

Fig. 3.1(a) shows the TIA configuration with the proposed diode-based feedback. C_{in} accounts for the parasitic capacitances at the input node, including the op-amp input capacitance, while C_f represents the total parasitic capacitance in the feedback path along with any additional stabilizing capacitance.

The feedback element is realized using a PMOS transistor (M_p) deliberately configured to operate as a compact PN-junction diode. The transistor source is shorted to its bulk, so the parasitic PN junction between the drain (P^+) and the bulk (N-well) is formed. The transistor gate is then statically biased at the highest supply voltage V_{DD}, ensuring a consistently negative V_{SG} and keeping the channel fully off under all operating conditions, including subthreshold leakage. Consequently, the input current I_{in} is directed exclusively through the drain–bulk PN junction, as shown in Fig. 3.1(b). For simplicity, only unidirectional conduction is considered in this

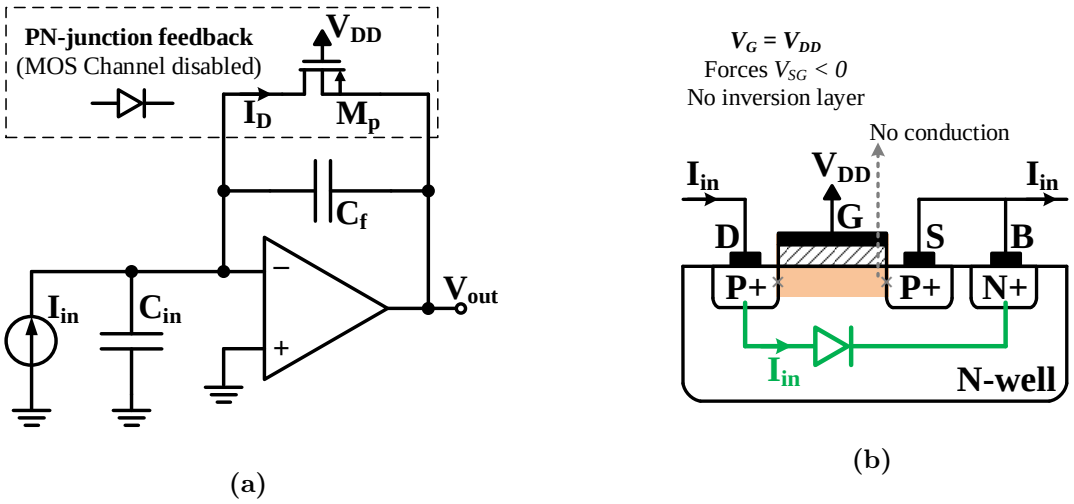


Figure 3.1: Proposed TIA with MOSFET PN-junction feedback: (a) circuit configuration; (b) cross-section illustrating drain–bulk PN-junction conduction without inversion.

section; bidirectional operation is discussed in Section 3.2.1.

The input current flowing through the proposed feedback is converted into a voltage signal according to the diode's exponential current–voltage (I–V) characteristic:

$$I_D = I_S \left(e^{V_{DS}/\alpha V_{th}} - 1 \right) \tag{3.1}$$

where I_D and I_S are the diode current and reverse saturation current of the junction, respectively, V_{DS} is the drain–source voltage (i.e., the diode voltage), and α denotes the ideality factor. I_S depends on the technological and physical parameters of the drain–well junction and can be expressed as:

$$I_S = J_S \cdot [2t_{dif}\, l_{dif} + W(2t_{dif} + l_{dif})] \tag{3.2}$$

where J_S denotes the reverse saturation current density, and the term in brackets corresponds to the effective junction area. W is the channel width, while t_{dif} and l_{dif} represent the vertical diffusion thickness and the lateral diffusion length, respectively.

3.1.1 Equivalent Resistance

Under the ideal assumption of $\alpha = 1$, the small-signal equivalent resistance of the proposed diode feedback, r_d, is given by the reciprocal of the derivative of the I–V characteristic:

$$r_d = \left(\frac{\partial I_D}{\partial V_{DS}} \right)^{-1} = \frac{V_{th}}{I_S}\, e^{-V_{DS}/V_{th}} \tag{3.3}$$

At low input current levels, where the PN junction operates in weak forward bias, r_d becomes extremely large. Fig. 3.2 depicts the simulated equivalent resistance of the proposed feedback for input currents below 1 nA. For currents below 10 pA, r_d reaches values on the order of GΩ, comparable to those achievable with passive

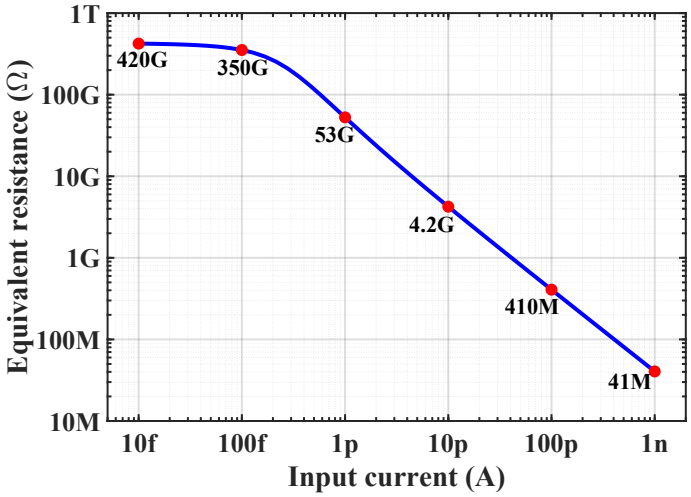


Figure 3.2: Simulated equivalent resistance of the proposed diode feedback as a function of input current. The feedback PMOS transistor size is $W/L = 5\,\mu m/2\,\mu m$.

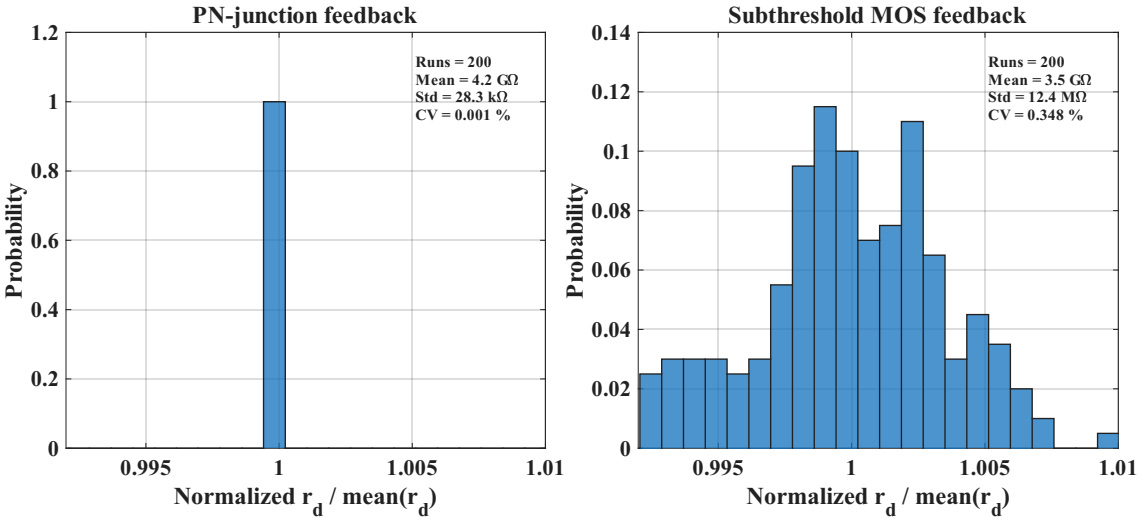


Figure 3.3: Monte Carlo analysis results (200 runs, $I_{in} = 10\,pA$, $T = 27\,°C$) showing the normalized distribution of equivalent dynamic resistance r_d for the proposed PN-junction feedback and a conventional subthreshold pseudo-resistor, including process and mismatch variations.

resistors. Crucially, however, passive resistors of such large values inherently exhibit substantial parasitic capacitance and require a stabilizing capacitor of several pF, restricting the TIA bandwidth to only a few tens of Hz. In contrast, the proposed diode-based feedback introduces minimal parasitic capacitance, typically in the range of tens of fF, preserving the TIA bandwidth.

To further assess the robustness of the proposed feedback element, a Monte Carlo analysis was performed at a representative operating point of $I_{in} = 10\,pA$ and $T = 27\,°C$, including both process and mismatch variations over 200 runs. The same transistor sizing ($W/L = 5\,\mu m/2\,\mu m$) was used for both the proposed PN-junction feedback and a conventional subthreshold pseudo-resistor for direct comparison. The resulting normalized distributions of the equivalent dynamic resistance r_d, expressed

as $r_d/\overline{r_d}$, are shown in Fig. 3.3. The proposed PN-junction feedback yields a mean equivalent resistance of 4.2 GΩ with a standard deviation of only 28.3 kΩ, corresponding to a coefficient of variation (CV) of 0.001 %. The normalized distribution is effectively a delta function on the scale of the plot, confirming that the equivalent resistance is practically insensitive to process and mismatch variations. In contrast, the conventional subthreshold pseudo-resistor achieves a comparable mean of 3.5 GΩ but exhibits a standard deviation of 12.4 MΩ and a CV of 0.348 %—more than 340 times larger than that of the proposed feedback—with the normalized distribution spreading broadly across the plotted range and displaying a mild right-skew characteristic of exponentially sensitive operating points.

This pronounced difference in variability is consistent with the fundamental distinction in the underlying conduction mechanisms. In subthreshold operation, the equivalent resistance is governed by gate-controlled channel conduction and therefore depends exponentially on the threshold voltage V_T, which is itself subject to substantial process-induced variation through both global (inter-die) and local (mismatch) components [33]. Since $r_{PR} \propto \exp(V_T/nV_{th})$ (cf. (2.28)), even modest fluctuations in V_T are amplified into large resistance variations. In the proposed PN-junction feedback, by contrast, the current is governed by junction transport rather than gate-controlled channel conduction. The reverse saturation current I_S depends primarily on junction geometry and doping profiles, both of which are tightly controlled by the fabrication process, and does not rely on maintaining a device in the subthreshold region through gate biasing. Consequently, the equivalent dynamic resistance $r_d = (V_{th}/I_S) \cdot \exp(-V_{DS}/V_{th})$ inherits the low variability of the junction parameters, resulting in the near-deterministic behavior observed in the Monte Carlo distribution. This robustness is particularly advantageous in a readout front-end, where variability in the feedback impedance directly translates into gain uncertainty, offset, and degraded noise predictability across fabricated units.

3.1.2 Noise Analysis

When the MOS channel is completely suppressed, the input current flows exclusively through the drain–bulk PN junction, bypassing the gate oxide interface entirely. Since no inversion layer is formed beneath the gate, the proposed feedback element is inherently free from the two dominant noise mechanisms of conventional subthreshold pseudo-resistors: channel thermal noise and flicker noise (Sections 2.2.1 and 2.2.2). Channel thermal noise is absent because no resistive conductive medium exists under the gate. Flicker noise is likewise suppressed, as the drain–bulk junction contains no oxide interface and the absence of an inversion layer eliminates the primary trapping mechanism responsible for $1/f$ noise in MOSFETs [40]. A minor generation–recombination component may in principle be present at junction defect states, but this is a second-order effect under forward-bias operation and is neglected here [41].

The dominant noise contribution is the shot noise arising from carrier transport

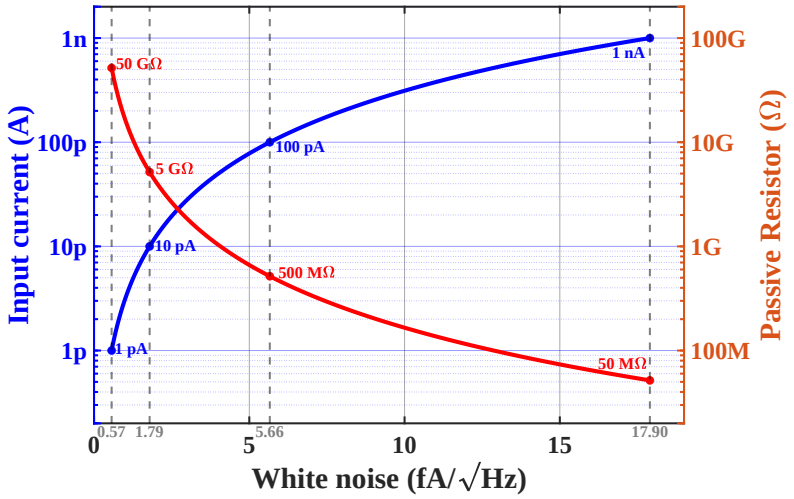


Figure 3.4: Shot noise of the proposed diode feedback (blue) versus input current, and equivalent thermal noise of passive resistors (red), based on analytical calculations.

across the drain–bulk junction potential barrier (Section 2.2.3), giving:

$$\overline{i_f^2} = \overline{i_{sh}^2} = 2q\, I_{in,dc} \tag{3.4}$$

where $I_{in,dc}$ denotes the average input current flowing through the feedback. It should be noted that the small-signal equivalent resistance r_d of (3.3) is a dynamic incremental parameter corresponding to the local slope of the exponential I–V characteristic, and does not constitute an independent physical resistor generating thermal Johnson noise. The drain–bulk junction does present a physical series resistance R_s due to the finite resistivity of the diffusion regions and the N-well, which generates thermal noise of PSD $4k_BTR_s$ [38]; however, since R_s is typically on the order of tens to hundreds of Ω, its input-referred contribution $4k_BTR_s/r_d^2$ is negligible compared to (3.4) under the operating conditions of interest. The absence of a $1/f$ term is a direct consequence of the channel-suppressed operating mode and represents a fundamental noise advantage over subthreshold PR implementations, for which $\overline{i_f^2}$ includes the additional flicker term given in (2.30).

Substituting into (2.20), the total input-referred current noise of the proposed TIA becomes:

$$\overline{i_{n,\mathrm{TIA}}^2} = 2q\, I_{in,dc} + \overline{e_{op}^2}\left[\frac{1}{r_d^2} + (2\pi f)^2(C_{in} + C_f)^2\right] \tag{3.5}$$

The first term, representing the shot noise of the feedback diode, remains low at small input current levels. Fig. 3.4 illustrates the shot noise spectral density as a function of input current over the range 1 pA to 1 nA, yielding a white noise floor of 0.57 fA/$\sqrt{\mathrm{Hz}}$ to 17.9 fA/$\sqrt{\mathrm{Hz}}$. For comparison, achieving equivalent noise performance with a passive resistor would require resistances ranging from 50 MΩ to 50 GΩ at room temperature. As a representative example, an input current of 10 pA generates 1.8 fA/$\sqrt{\mathrm{Hz}}$ of shot noise, equivalent to the thermal noise of a 5 GΩ passive resistor.

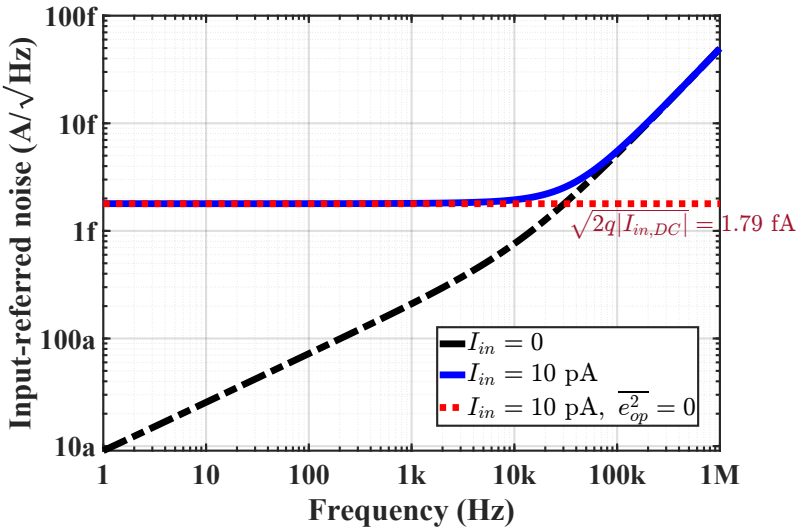


Figure 3.5: Simulated input-referred current noise of the proposed TIA: zero input current (black); 10 pA input current with op-amp noise disabled (red); and 10 pA input current with op-amp noise enabled (blue). $C_f = 50\,\text{fF}$, $C_{in} = 1\,\text{pF}$.

The second term represents the input-referred contribution of the op-amp voltage noise $\overline{e_{op}^2}$, shaped by r_d at low frequencies and by the total input capacitance $(C_{in} + C_f)$ at high frequencies, consistent with the general framework of (2.20). The compact layout of the diode-based feedback minimizes C_f, partially alleviating the high-frequency capacitive noise rise relative to conventional resistive implementations.

Fig. 3.5 shows the simulated input-referred current noise of the TIA with the proposed feedback, evaluated with $C_f = 50\,\text{fF}$ and $C_{in} = 1\,\text{pF}$. The black curve corresponds to zero input current, where the shot noise vanishes and r_d approaches extremely large values; under this condition, (3.5) reduces to $\overline{e_{op}^2}(2\pi f)^2 C_{in}^2$ since $C_f \ll C_{in}$. The red curve shows the spectrum with a 10 pA DC input current and op-amp noise disabled ($\overline{e_{op}^2} = 0$), confirming that the proposed diode feedback introduces predominantly shot noise at the input. The blue curve shows the complete noise spectrum with op-amp noise included, where the noise floor remains dominated by shot noise at low and mid frequencies.

3.2 TIA Core Architecture

While the proposed PN-junction feedback enables ultra-low noise performance, the basic configuration of Fig. 3.1(a) introduces several critical challenges that must be addressed for precision sensing applications:

1. The input current is sensed only if it drives the drain–bulk (P^+/N-well) junction of the feedback PMOS transistor into forward bias, i.e., when $V_D > V_S$. This limits the TIA's ability to handle bipolar input currents.

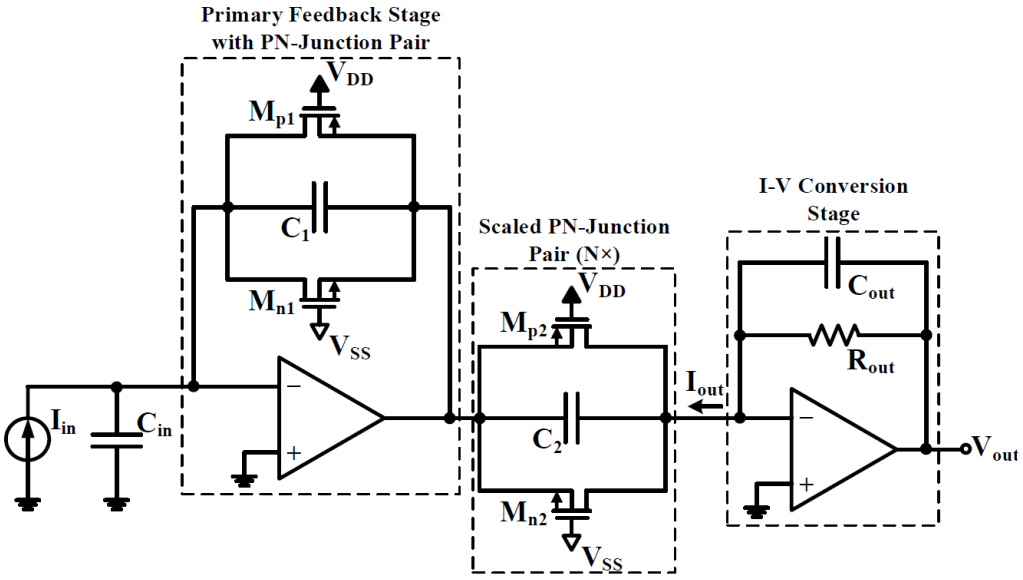


Figure 3.6: Implemented TIA core, showing the primary PN-junction feedback stage, scaled auxiliary stage, and I–V conversion stage.

2. The exponential I–V characteristic of the PN junction introduces inherent nonlinearity in the current-to-voltage conversion.

3. The high equivalent resistance r_d in the weak forward-bias regime forms a large time constant with the feedback capacitance C_f, restricting the amplifier bandwidth.

These drawbacks degrade signal fidelity and constrain the TIA's applicability in precision sensing applications. To overcome these limitations while preserving the low-noise benefits of the original configuration, the basic structure is augmented with complementary techniques. The resulting implemented architecture, hereafter referred to as the TIA core, is shown in Fig. 3.6. It is powered by the highest and lowest supply voltages V_{DD} and V_{SS}, respectively, with the common-mode voltage set to $(V_{DD} + V_{SS})/2 = 0$, such that the non-inverting inputs of both op-amps are connected to ground. The architecture consists of three cascaded stages: a primary PN-junction feedback stage, a scaled auxiliary PN-junction stage, and a linear I–V conversion stage. The following subsections address each of the limitations identified above in turn: Section 3.2.1 introduces the complementary anti-parallel junction pair for bipolar operation; Section 3.2.2 describes the ratiometric technique used to linearize the current gain; Sections 3.2.3 and 3.2.4 analyze the frequency response and loop stability of the cascaded architecture; and Section 3.2.5 derives the noise performance of the complete system.

3.2.1 Signal Symmetry

To enable symmetric signal response for bipolar input currents, an NMOS transistor M_{n1} is placed in parallel with the PMOS transistor M_{p1}, forming a complementary

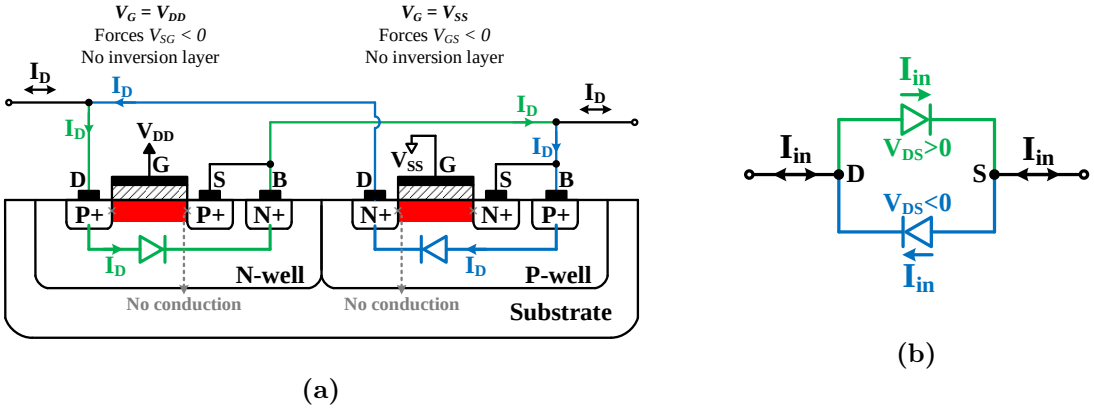


Figure 3.7: Anti-parallel PN-junction diodes: (a) cross-section of the PMOS and NMOS transistors with the channels fully turned off; (b) schematic circuit view.

anti-parallel pair. As illustrated in the cross-section of Fig. 3.7(a), both transistors are configured to operate exclusively as PN-junction diodes with their channels fully suppressed. The PMOS gate is biased at V_{DD}, enforcing $V_{SG} < 0$ and eliminating inversion in the N-well, while the NMOS gate is biased at V_{SS}, enforcing $V_{GS} < 0$ and eliminating inversion in the P-well. Under these conditions, the PMOS drain–bulk (P^+/N-well) junction conducts for positive input currents, while the NMOS drain–bulk (N^+/P-well) junction conducts for negative input currents, as shown in the schematic circuit view of Fig. 3.7(b). The resulting anti-parallel configuration provides bidirectional current conduction with symmetric signal sensing, while preserving the channel-suppressed operating mode that fundamentally eliminates MOS channel noise in both devices.

3.2.2 Gain and Linearity

The exponential I–V characteristic of the PN junction introduces inherent nonlinearity into the current-to-voltage conversion of the basic topology. To mitigate this, a ratiometric linearization technique [31] is employed, in which the nonlinearity of the feedback element is cancelled by operating two matched junctions at identical bias points and exploiting the proportionality of their saturation currents to transistor geometry.

The primary feedback stage (M_{p1}–M_{n1}) is cascaded with an auxiliary anti-parallel diode pair (M_{p2}–M_{n2}), constructed as N replicas of the primary feedback transistors. As shown in Fig. 3.6, the virtual ground enforced by the first op-amp ensures that each matched pair (M_{p1}–M_{p2} or M_{n1}–M_{n2}) experiences the same V_{DS}, ensuring identical voltage drops across their respective drain–bulk junctions. Consequently, from (3.1), the ratio of their drain currents equals the ratio of their reverse saturation currents: $I_{D1}/I_{D2} = I_{S1}/I_{S2}$. Since the term proportional to W typically dominates in (3.2), I_S scales approximately linearly with transistor width, giving a

current gain of:

$$\frac{I_{out}}{I_{in}} = \frac{I_{D2}}{I_{D1}} = \frac{W_2}{W_1} = N \tag{3.6}$$

The cascaded structure therefore functions as a linear current amplifier with a constant gain factor N, effectively decoupling the overall transimpedance gain from the nonlinear exponential I–V characteristic of the junction. The nonlinearity is mitigated because both junctions in each matched pair track identically across all operating points: any deviation from linearity in the primary stage is replicated proportionally in the auxiliary stage, so their current ratio remains constant and equal to N regardless of the instantaneous junction voltage.

The amplified current I_{out} is subsequently converted into an output voltage by a conventional resistive-feedback TIA forming the I–V conversion stage. The low-frequency transimpedance gain of the complete architecture is therefore:

$$R_{TIA} = \frac{V_{out}}{I_{in}} = \frac{I_{out}}{I_{in}} \cdot \frac{V_{out}}{I_{out}} = N \cdot R_{out} \tag{3.7}$$

where R_{out} is the linear feedback resistor of the output stage. The designation R_{TIA} reflects the resistive, frequency-independent nature of the gain at low frequencies, where the feedback capacitances C_1, C_2, and C_{out} present negligible admittance.

It is important to distinguish the proposed architecture from prior implementations that employ a similar ratiometric technique [31, 42, 43]. In those designs, the gates of all transistors in the current amplifier are connected to the same voltage as the non-inverting input of the op-amp—either a reference potential such as ground [31, 42] or a fixed bias voltage [43]. Because the virtual ground at the op-amp inverting input forces the drain to the same potential as the gate, the transistors operate in a transdiode connection, placing them in subthreshold conduction for low input currents. In the proposed architecture, by contrast, the PMOS gates are permanently connected to V_{DD} and the NMOS gates to V_{SS}. This ensures that the transistors function exclusively as PN-junction diodes under all operating conditions, including large-signal excursions, with the MOS channel fully suppressed at all times. The noise advantage demonstrated in Section 3.1.2 is therefore preserved throughout the complete signal chain, from the primary feedback stage through to the auxiliary current amplifier.

3.2.3 Bandwidth

Fig. 3.8 shows the small-signal equivalent circuit of the TIA core, where r_{d1} and r_{d2} denote the equivalent dynamic resistances of the feedback and auxiliary PN junction pairs, respectively, and C_1 and C_2 are the stabilizing capacitances placed in parallel with each pair. Assuming the first op-amp can be modeled as a single-pole system with gain-bandwidth product GBW_1, the transfer function from I_{in} to the first-stage output V_x is:

$$\frac{V_x(s)}{I_{in}(s)} = -\frac{r_{d1}}{\left(1 + \dfrac{C_{in} + C_1}{GBW_1 \cdot C_1}\, s\right)(1 + r_{d1} C_1\, s)} \tag{3.8}$$

By adding the auxiliary stage, a zero is formed by r_{d2} and C_2 at:

$$Z_1 = -\frac{1}{r_{d2}C_2} \tag{3.9}$$

Since the equivalent dynamic resistance of a PN junction is inversely proportional to its reverse saturation current (3.3), and I_S scales proportionally with junction area (3.2), the resistance of the primary pair is N times that of the auxiliary pair:

$$r_{d1} = N\, r_{d2} \tag{3.10}$$

Accordingly, scaling C_2 to N times C_1 satisfies the pole-zero cancellation condition:

$$r_{d1}C_1 = r_{d2}C_2 \quad \Rightarrow \quad C_2 = N \cdot C_1 \tag{3.11}$$

Under this condition, pole–zero compensation between the primary feedback and scaled replica branches in the current amplifier is achieved. Assuming the second op-amp can be modeled as a single-pole system with gain-bandwidth product GBW_2, the overall transimpedance transfer function of the TIA core can be approximated as:

$$Z_{TIA}(s) \approx \frac{NR_{out}}{\left(1 + \dfrac{C_{in} + C_1}{GBW_1 C_1} s\right)\left(1 + \dfrac{s}{GBW_2}\right)(1 + R_{out}C_{out}\, s)} \tag{3.12}$$

which exhibits three poles:

$$P_1 \approx -GBW_1 \cdot \frac{C_1}{C_{in} + C_1} \tag{3.13}$$

$$P_2 \approx -GBW_2 \tag{3.14}$$

$$P_3 = -\frac{1}{R_{out}C_{out}} \tag{3.15}$$

The first pole P_1 is set by GBW_1 scaled by the capacitive ratio $C_1/(C_{in} + C_1)$. The second pole P_2 corresponds directly to GBW_2 of the second op-amp. The third pole P_3 is determined solely by the output RC time constant $R_{out}C_{out}$, which is a well-controlled design parameter independent of sensor conditions.

In a practical implementation, P_1 and P_2 are placed at sufficiently high frequencies by selecting op-amps with adequate gain-bandwidth products. However, since P_1 is reduced by the capacitive division factor $C_1/(C_{in} + C_1)$ relative to GBW_1, the first op-amp must typically exhibit a higher gain-bandwidth product than the second to ensure $|P_1| > |P_2|$. Through appropriate selection of R_{out} and C_{out}, P_3 is positioned as the dominant pole of the TIA, such that the -3 dB bandwidth is determined by the output stage alone:

$$f_{-3\text{dB}} \approx \frac{1}{2\pi R_{out}C_{out}} \tag{3.16}$$

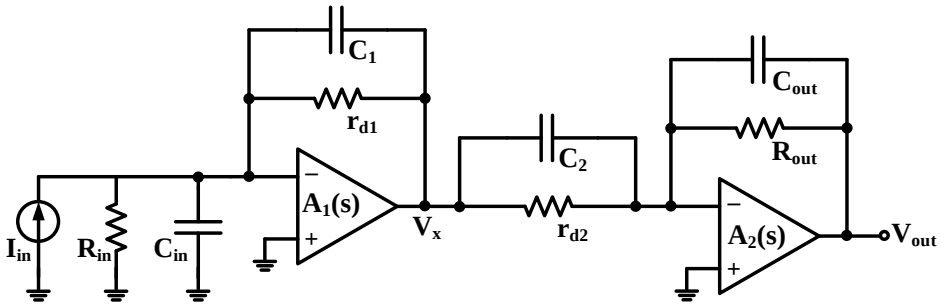


Figure 3.8: Small-signal equivalent circuit of the TIA core, showing the dynamic resistances r_{d1} and r_{d2} of the feedback and auxiliary PN junction pairs, stabilizing capacitances C_1 and C_2, and the output stage components R_{out} and C_{out}.

3.2.4 Stability

The first feedback stage, being closest to the input, primarily governs the TIA's dynamic response and therefore plays the dominant role in overall system stability. The stability analysis is accordingly focused on the first stage; the output I–V conversion stage operates under more controlled conditions and has a comparatively minor influence. Based on the small-signal model of Fig. 3.8, and assuming the first op-amp exhibits a DC gain A_0 and a dominant pole at P_0, the open-loop transfer function of the first stage is:

$$G(s) = -\frac{A_0 P_0 \, R_{in}(1 + r_{d1} C_1 \, s)}{(R_{in} + r_{d1} + R_{in} r_{d1}(C_{in} + C_1) \, s) \, (P_0 + s)} \tag{3.17}$$

where R_{in} represents the output resistance of the sensor. This transfer function features a zero at:

$$Z_1 = -\frac{1}{r_{d1} C_1} \tag{3.18}$$

and two poles at:

$$P_1 = -\frac{1}{(R_{in} \| r_{d1})(C_{in} + C_1)} \tag{3.19}$$

$$P_2 = -P_0 \tag{3.20}$$

At low input current levels, r_{d1} becomes very large, shifting the zero Z_1 toward very low frequencies. Concurrently, since R_{in} is also large in nanopore sensing applications, the first pole P_1 moves to similarly low frequencies. When both Z_1 and P_1 lie well below P_2, they primarily attenuate the loop gain at low frequencies without introducing significant phase shift near the unity-gain crossover frequency. This behavior inherently improves the phase margin and enhances the stability of the first-stage feedback loop, without requiring additional compensation networks.

3.2.5 Noise

Fig. 3.9 illustrates the noise sources in the TIA core. $\overline{i^2_{sh1,2}}$ represent the shot noise from the feedback and auxiliary PN junctions, $\overline{i^2_{op1,2}}$ denote the equivalent input

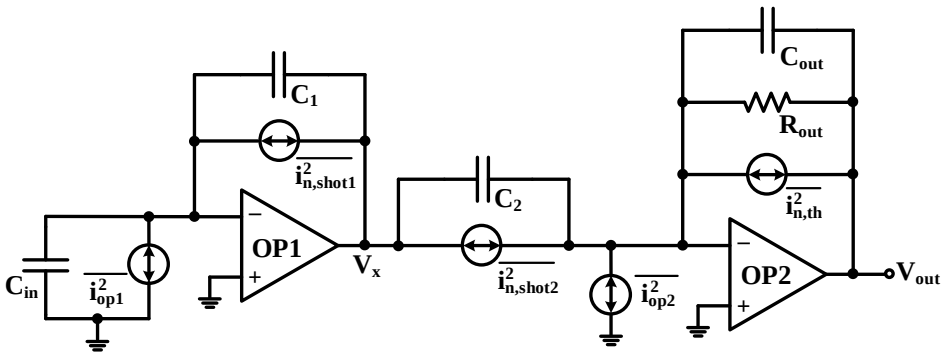


Figure 3.9: Noise model of the TIA core, showing shot noise sources from the feedback and auxiliary PN junctions, op-amp input noise sources, and the thermal noise of the output resistor R_{out}.

current noise of the op-amps arising from their intrinsic voltage noise $\overline{e_{op}^2}$, and $\overline{i_{th}^2}$ is the thermal noise of the output resistor R_{out}. The noise sources $\overline{i_{sh2}^2}$, $\overline{i_{op2}^2}$, and $\overline{i_{th}^2}$ appear at the output of the current amplifier stage and, when referred to the TIA input, are attenuated by the current gain N. The total input-referred current noise is therefore:

$$\overline{i_{n,\mathrm{TIA}}^2} \approx \overline{i_{sh1}^2} + \overline{i_{op1}^2} + \frac{1}{N^2}\left[\overline{i_{sh2}^2} + \overline{i_{th}^2} + \overline{i_{op2}^2}\right] \tag{3.21}$$

Assuming both op-amps have identical intrinsic voltage noise $\overline{e_{op}^2}$, (3.21) expands to:

$$\begin{aligned}\overline{i_{n,\mathrm{TIA}}^2} \approx{}& 2q\,I_{in,dc} + \frac{2q\,I_{out,dc}}{N^2} + \frac{4k_BT}{N^2R_{out}} \\ &+ \overline{e_{op}^2}\left[\frac{1}{r_{d1}^2} + \frac{1}{(NR_{out})^2} + (2\pi f)^2\left((C_{in}+C_1)^2 + \left(\frac{C_{out}+C_2}{N}\right)^2\right)\right]\end{aligned} \tag{3.22}$$

where $I_{out,dc} = N \cdot I_{in,dc}$ is the DC output current of the current amplifier. The noise contributions from the output stage are governed by R_{out} and C_{out}, which also determine the TIA bandwidth; their values must therefore be carefully chosen to achieve an optimal trade-off between noise and bandwidth. By applying the design condition $C_2 = NC_1$ of (3.11), noting that $C_{out} \ll C_2$, and selecting $N \gg 1$ such that the contributions of subsequent stages become negligible, (3.22) reduces to:

$$\overline{i_{n,\mathrm{TIA}}^2} \approx 2q\,I_{in,dc} + \overline{e_{op}^2}\left[\frac{1}{r_{d1}^2} + (2\pi f)^2\left((C_{in}+C_1)^2 + C_1^2\right)\right] \tag{3.23}$$

This expression provides nearly the same noise performance as the single-stage configuration of (3.5), confirming that the TIA core architecture preserves the fundamental noise advantage of the proposed TIA with PN-junction feedback.

3.3 DC-Compensated TIA

While the implemented TIA core of Section 3.2 achieves ultra-low input-referred noise through the PN-junction feedback mechanism, it shares a limitation common

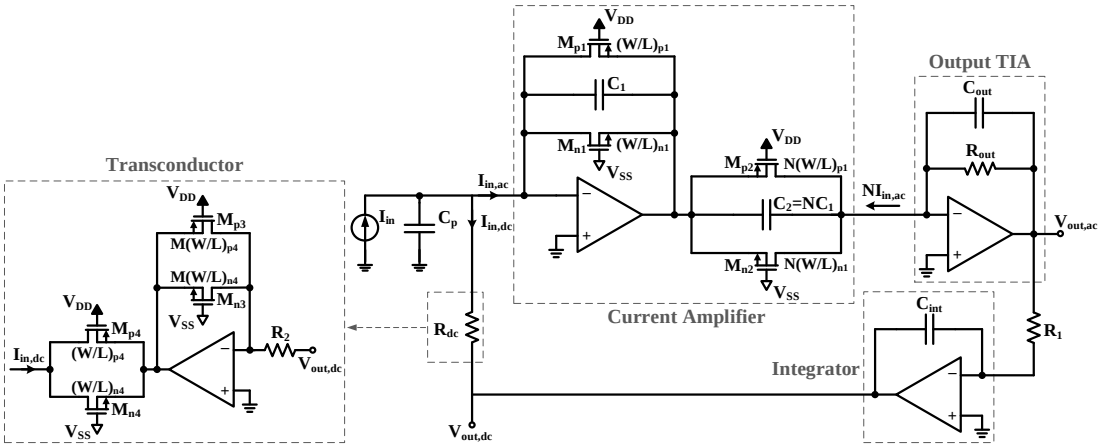


Figure 3.10: Proposed DC-compensated TIA architecture. The current amplifier and output TIA together form the TIA core, while R_1, the integrator, and R_{dc} constitute the DC-servo loop.

to all resistive-feedback topologies: the presence of a large DC baseline current $I_{in,dc}$—such as the open-pore ionic current inherent to nanopore sensing—drives the TIA output toward saturation, severely restricting the available dynamic range for the AC signal components of interest. As analyzed in Section 2.4, this limitation can be addressed by introducing a DC-servo loop that continuously monitors and cancels the DC component of the input current, relieving the TIA core from processing large baseline currents while preserving its low-noise continuous-time operation. The proposed DC-compensated architecture is shown in Fig. 3.10. The architecture consists of two functional blocks: the TIA core, comprising the current amplifier and the output TIA; and the DC-servo loop, comprising the sampling resistor R_1, the active integrator, and the compensation resistance R_{dc} realized by the transconductor stage. The DC baseline current $I_{in,dc}$ is diverted through the DC-servo path to produce $V_{out,dc}$, while the AC signal component $I_{in,ac}$ propagates through the TIA core to produce $V_{out,ac}$. The following subsections analyze the DC-servo loop implementation, the resulting dynamic range extension, and the noise performance of the complete system.

3.3.1 DC-Servo Loop

The DC-servo loop consists of the sampling resistor R_1, an active integrator realizing $H(s)$, and a transconductor stage generating the compensation current through the effective resistance R_{dc}, as shown in Fig. 3.10. As established in Section 2.4.4, the resistive nature of the R-TIA core does not introduce an inherent phase lag at low frequencies, permitting $H(s)$ to be realized as a simple active integrator without a compensating zero. The resistor R_1 samples the output voltage of the TIA and feeds it to the integrator input. Assuming a finite op-amp open-loop gain A_0, the

transfer function of $H(s)$ is:

$$H(s) = -\frac{A_0}{1 + sR_1C_{int}(A_0 + 1)} \tag{3.24}$$

which introduces a pole at:

$$f_p = \frac{1}{2\pi R_1 C_{int}(A_0 + 1)} \tag{3.25}$$

Due to $A_0 \gg 1$, this pole is shifted to very low frequencies. At low frequencies, $H(s)$ provides a high DC gain of A_0, which decreases to unity at:

$$f_u \approx \frac{1}{2\pi R_1 C_{int}} \tag{3.26}$$

By selecting sufficiently large values of R_1 and C_{int}, both f_u and f_p are shifted toward lower frequencies, enhancing the DC filtering capability of $H(s)$ and ensuring effective attenuation of AC signal components in the DC-servo path.

As indicated by (2.35), the DC-servo loop requires a large equivalent resistance R_{dc} to minimize its noise contribution. However, implementing such large resistances using passive components is impractical in integrated circuits due to the excessive silicon area required. From the feedback perspective, the DC-servo loop generates a compensation current proportional to the filtered output voltage of the TIA, which can be interpreted as a voltage-to-current conversion with an equivalent transconductance $G_{dc} = 1/R_{dc}$. Realizing a very large R_{dc} is therefore equivalent to implementing an extremely small transconductance. To this end, the proposed architecture employs an active transconductance circuit based on a current-divider topology, as shown in the Transconductor block of Fig. 3.10. The transistors M_{p3} and M_{n3} form the primary diode pair, while M_{p4} and M_{n4}, sized at M times the width of M_{p3} and M_{n3} respectively, form the scaled replica pair. All four transistors operate as pure PN-junction diodes with their channels fully suppressed, consistent with the operating principle described in Section 3.2.1. The voltage filtered by $H(s)$ induces a reference current through the ohmic resistor R_2 via the primary pair M_{p3}–M_{n3}. This current is then scaled by a factor M through the matched replica pair M_{p4}–M_{n4}, which share identical terminal voltages with the primary pair, and the scaled current is injected into the TIA input node as the compensation current. The equivalent transconductance of this stage is therefore $G_{dc} = 1/(MR_2)$, and the effective compensation resistance is:

$$R_{dc} = M \cdot R_2 \tag{3.27}$$

producing the DC output voltage $V_{out,dc}$ at the transconductor output. The DC input current $I_{in,dc}$ is thereby diverted through this effective resistance, relieving the TIA core from processing the large baseline. From (3.6) and (3.24), the crossover frequency of the DC-servo loop can be approximated as:

$$f_m \approx \frac{R_{TIA}}{2\pi R_1 R_{dc} C_{int}} = \frac{NR_{out}}{MR_2} f_u \tag{3.28}$$

The condition $NR_{out} > MR_2$ ensures that AC signal components experience sufficient attenuation through the DC-servo path, thereby preventing their coupling to the TIA input.

3.3.2 Dynamic Range

By separating the DC and AC signal paths, the proposed architecture exhibits distinct dynamic range limits for each component. Both paths share the same output voltage swing $V_{out,max}$, determined by the supply voltage and the op-amp output stage. The maximum DC baseline current that can be absorbed by the DC-servo loop is set by the effective compensation resistance R_{dc} (3.27):

$$I_{in,dc,max} = \frac{V_{out,max}}{R_{dc}} = \frac{V_{out,max}}{M \cdot R_2} \tag{3.29}$$

The maximum AC signal current that can be processed by the TIA core without saturation is limited by the low-frequency transimpedance gain R_{TIA} (3.7):

$$I_{in,ac,max} = \frac{V_{out,max}}{R_{TIA}} = \frac{V_{out,max}}{N \cdot R_{out}} \tag{3.30}$$

Since the DC-servo loop maintains the TIA output close to its nominal operating point by continuously cancelling $I_{in,dc}$, the full output swing $V_{out,max}$ remains available for AC signal excursions regardless of the DC baseline level. The effective dynamic range of the readout system is therefore extended significantly compared to the TIA core alone, which would otherwise be driven toward saturation by the DC baseline. The scaling factors M and N provide independent control over the DC and AC dynamic range limits respectively, allowing the two to be optimized separately for a given sensing application.

3.3.3 Noise Analysis

Owing to the absence of an inversion layer in all MOSFETs configured as PN-junction diodes, the conventional channel-induced noise sources—flicker noise and channel thermal noise—are effectively suppressed throughout both the TIA core and the transconductor stage, as established in Section 3.1.2. The noise behavior of the proposed DC-compensated TIA is therefore analyzed using the equivalent noise model of Fig. 3.11, in which $\overline{i_{sh}^2}$, $\overline{i_{th}^2}$, $\overline{i_{op}^2}$, and $\overline{v_{n,\text{out}}^2}$ denote the shot noise of each PN junction, the thermal current noise of each resistor, the equivalent input current noise of each op-amp, and the voltage noise at the TIA output, respectively. To evaluate the overall noise performance of the DC-compensated TIA, the input-referred noise contributions of the TIA core and the DC-servo loop are analyzed separately below.

TIA core. By diverting the baseline current through the DC-servo loop, the DC current flowing through the TIA core is driven to zero in steady state, suppressing the shot-noise contributions $\overline{i_{sh1}^2}$ and $\overline{i_{sh2}^2}$ in the TIA core. Furthermore, as the DC diode current approaches zero, the dynamic resistance r_{d1} reaches values in the TΩ range (Section 3.1.1), strongly attenuating the op-amp voltage noise contribution through the $1/r_{d1}^2$ term. Consequently, the TIA core noise of (3.23) reduces to:

$$\overline{i_{n,\text{TIA}}^2} \approx \overline{e_{op1}^2}(2\pi f)^2 \left[(C_{in} + C_1)^2 + C_1^2\right] \tag{3.31}$$

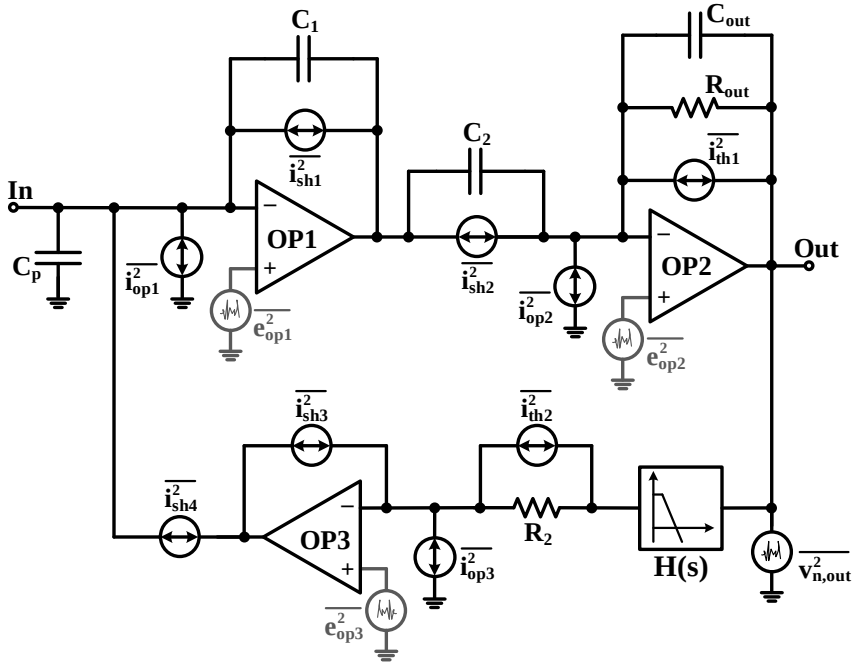


Figure 3.11: Equivalent noise model of the DC-compensated TIA, showing shot noise sources from the PN-junction diodes in the TIA core and transconductor, thermal noise of the resistors, op-amp input noise sources, and the output voltage noise $\overline{v_{n,\text{out}}^2}$.

This expression indicates that, following removal of the DC baseline current, the residual input-referred noise of the TIA core is governed solely by the op-amp intrinsic voltage noise coupled through the total input capacitance—a behavior analogous to that of capacitive-feedback TIAs (Section 2.3.1).

DC-servo loop. As established in (2.35), the noise introduced by the DC-servo loop consists of the thermal noise of R_{dc} and the TIA output noise $\overline{v_{n,\text{out}}^2}$ filtered by $H(s)$ and referred to the input through R_{dc}. The coupling of $\overline{v_{n,\text{out}}^2}$ through the DC-servo path is effectively suppressed by the high attenuation of $H(s)$ within the signal band. Since R_{dc} is realized by the proposed PN-junction transconductor rather than a passive resistor, its noise contribution is governed by the transconductor noise sources. The input-referred noise of the DC-servo loop is therefore:

$$\overline{i_{n,\text{DC}}^2} \approx \overline{i_{sh4}^2} + \frac{1}{M^2}\left[\overline{i_{sh3}^2} + \overline{i_{op3}^2} + \overline{i_{th2}^2}\right] \tag{3.32}$$

The second term represents the noise sources at the transconductor input, reduced by M^2 when referred to the TIA input. For sufficiently large M, this term becomes negligible, and (3.32) reduces to:

$$\overline{i_{n,\text{DC}}^2} \approx 2q\, I_{in,dc} \tag{3.33}$$

where $I_{in,dc}$ is the residual DC baseline current at the TIA input in steady state.

Total input-referred noise. Combining (3.31) and (3.33) with (2.34), the overall input-referred current noise of the proposed DC-compensated TIA is:

$$\overline{i_{n,in}^2} \approx 2q\, I_{in,dc} + \overline{e_{op1}^2}(2\pi f)^2 \left[(C_{in} + C_1)^2 + C_1^2\right] \tag{3.34}$$

At low frequencies, the spectrum is dominated by the shot noise contribution $2q\, I_{in,dc}$, which scales with the residual DC baseline current. At higher frequencies, the capacitive coupling of the first op-amp voltage noise becomes dominant, causing the input-referred noise to rise with frequency. To reduce the high-frequency noise floor, C_1 can be minimized without incurring a noise–dynamic range trade-off, unlike in capacitive-feedback TIAs (Section 2.3.1). In the limit $C_1 \to 0$, (3.34) further simplifies to:

$$\overline{i_{n,in}^2} \approx 2q\, I_{in,dc} + \overline{e_{op1}^2}(2\pi f)^2 C_{in}^2 \tag{3.35}$$

Further noise reduction can be achieved by minimizing the parasitic input capacitance C_{in} and the intrinsic op-amp noise $\overline{e_{op1}^2}$, the latter requiring an ultra-low-noise design for OP1. The expression in (3.35) is derived under the assumption of sufficiently large scaling factors N and M, which effectively suppress the noise contributions of subsequent stages when referred to the TIA input. Nevertheless, for input currents close to zero, where the shot-noise term becomes negligible, the residual noise contributions of subsequent stages may become dominant, giving rise to flicker and white noise components.

3.4 Summary

This chapter has presented the theoretical design of the proposed continuous-time current readout system for nanopore sensing applications.

The first original contribution is a novel TIA topology exploiting the intrinsic drain–bulk PN junction of a MOSFET as the feedback element. By biasing the transistor gate to fully suppress channel conduction, the feedback element operates exclusively through junction transport, eliminating both flicker noise and channel thermal noise. The dominant noise contribution is shot noise, which at pA-level input currents is equivalent to the thermal noise of a passive resistor in the GΩ–TΩ range. Monte Carlo analysis confirms that the junction-based feedback exhibits a coefficient of variation more than 340 times smaller than that of a comparable subthreshold pseudo-resistor, demonstrating superior robustness to process and mismatch variations.

The implemented TIA core extends the basic topology with complementary anti-parallel junction pairs for bipolar operation, a ratiometric current amplifier for linearisation, and pole-zero compensation for bandwidth control. The low-frequency transimpedance gain is $R_{TIA} = N \cdot R_{out}$, and the $-3\,\mathrm{dB}$ bandwidth is determined by the well-controlled output RC time constant $R_{out}C_{out}$, independent of sensor capacitance variations. Stability analysis confirms that at low input current levels, the inherently large junction resistance and sensor output resistance improve phase margin without additional compensation networks.

The second original contribution extends the TIA core with a DC-servo loop for wide dynamic range operation. The servo loop employs an active integrator and a PN-junction-based transconductor to continuously divert the DC baseline current away from the TIA core, preserving the full output swing for AC signal excursions. In steady state, the DC current through the TIA core approaches zero, driving r_{d1} into the TΩ range and reducing the residual input-referred noise to a behaviour analogous to capacitive-feedback TIAs, but without the associated noise–dynamic range trade-off. The combined architecture achieves pA-level noise resolution while accommodating nA-level DC baselines, meeting the simultaneous requirements of nanopore current readout established in Chapter 1.

Chapter 4

Ultra-Low-Noise Current Readout ASIC

The proposed current readout system presented in Chapter 3 is realised as a monolithic application-specific integrated circuit (ASIC), designated QC01a, designed in the 0.35 µm CMOS technology node. The chip integrates two identical current readout cores, each of which can operate independently or in parallel, providing flexibility for differential, redundant, or multi-channel measurements. The top-level block diagram of one readout core is shown in Fig. 4.1. The remainder of this chapter describes the implementation of the AFE, each supporting block, and the physical layout of the chip.

4.1 Analog Front-End

To demonstrate the practical feasibility of the proposed low-noise current recording, a prototype AFE is implemented based on the proposed DC-compensated TIA architecture of Fig. 3.10. The implemented AFE is illustrated in Fig. 4.2, designed to accommodate an output swing of $\pm 1.5\,\mathrm{V}$, where each block retains the internal transistor-level structure of Fig. 3.10 and is shown in simplified form for clarity. While the practical implementation introduces several modifications with respect to the theoretical architecture, the analyses of noise, bandwidth, stability, and dynamic range presented in Section 3.3 remain fully applicable, as the implemented circuit preserves the fundamental operating principle of the proposed architecture. The specific modifications introduced at the implementation level, together with their motivations, are detailed in the following subsections.

4.1.1 AC Current Processing

Achieving a large current gain N through a single stage is impractical due to device matching constraints and the associated increase in parasitic capacitances. The current preamplifier is therefore implemented as two cascaded PN-junction stages

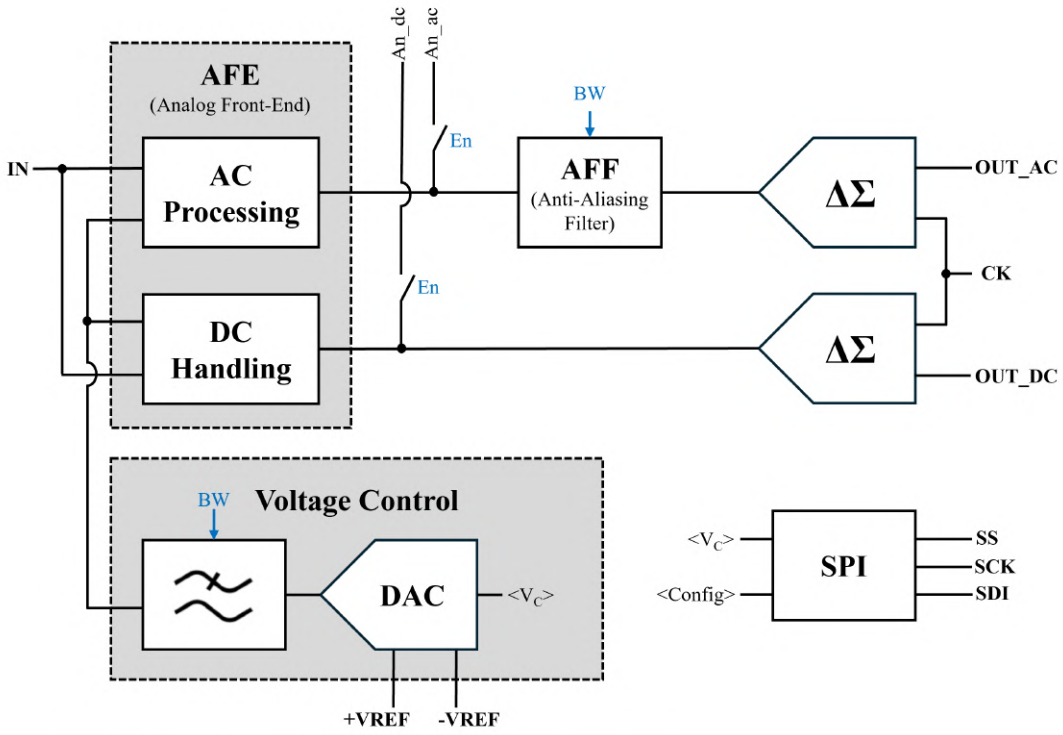


Figure 4.1: Top-level block diagram of one readout core of the QC01a ASIC, showing the analog front-end (AFE) with AC and DC processing paths, the anti-aliasing filter (AAF), the two $\Delta\Sigma$ modulators, the voltage control block, and the SPI configuration interface. Analog outputs An_ac and An_dc provide direct access to the AFE outputs for off-chip digitisation.

with individual gains $N_1 = 100$ and $N_2 = 10$, yielding a total current gain of $N = 1000$. This large gain is required to suppress the input-referred noise contributions of subsequent stages, as predicted by (3.23). The additional cascaded stage primarily serves to realise the required overall gain without significantly degrading the input-referred noise, since the DC-servo loop absorbs the DC baseline current and thereby suppresses the shot-noise contributions of all PN-junction diodes within the TIA core under steady-state conditions. The PMOS and NMOS transistors in the current preamplifier are configured with aspect ratios of $(W/L)_p = 20\,\mu\text{m}/2\,\mu\text{m}$ and $(W/L)_n = 7\,\mu\text{m}/2\,\mu\text{m}$ respectively.

To ensure closed-loop stability within the TIA core, the feedback capacitor C_1 is set to 200 fF in the first stage and 2 pF in the second stage. According to the pole–zero compensation condition of (3.11), the corresponding compensation capacitances $C_2 = N_i \cdot C_1$ are set to 20 pF for both stages, satisfying the pole-zero cancellation condition independently at each level of the cascade.

The amplified current from the preamplifier is converted to a voltage by a conventional resistive-feedback TIA, forming the output I–V conversion stage. The $-3\,\text{dB}$ bandwidth of the TIA core is by default set to approximately 1 MHz by selecting $R_{out} = 100\,\text{k}\Omega$ and $C_{out} = 1.5\,\text{pF}$, consistent with (3.16). This relatively high bandwidth ensures sufficient phase margin for the DC-servo loop, facilitating

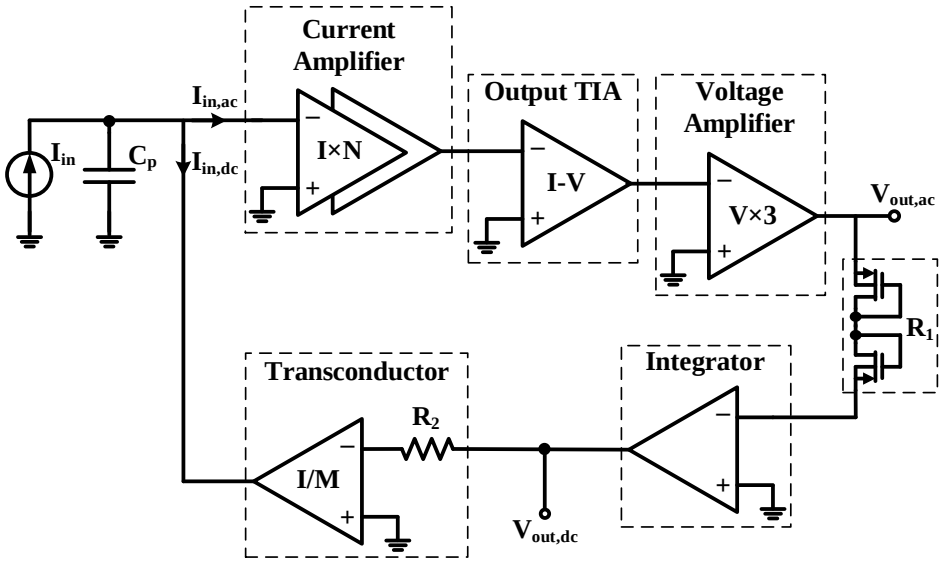


Figure 4.2: System-level schematic of the implemented AFE, based on the proposed DC-compensated TIA architecture of Fig. 3.10. With respect to the theoretical architecture, the current amplifier is realised as two cascaded stages, a voltage amplifier is added at the output of the TIA core, and the integrator resistor R_1 is implemented as a conventional PR.

its implementation as discussed in Section 2.4.4. Note that this feedback network is reconfigurable, allowing the transimpedance gain, bandwidth, and corresponding AC current range to be adjusted according to the measurement requirements.

To further increase the overall AC signal gain without degrading the bandwidth, an additional voltage amplifier stage with a gain of 3 is incorporated at the output of the TIA core. The resulting effective low-frequency transimpedance gain of the complete TIA core is:

$$R_{TIA} = N \cdot R_{out} \cdot 3 = 1000 \times 100\,\mathrm{k\Omega} \times 3 = 300\,\mathrm{M\Omega} \tag{4.1}$$

Consequently, the maximum linear AC input current swing is limited to approximately $\pm 5\,\mathrm{nA}$. The separation between current pre-amplification, transimpedance generation, and voltage amplification enables independent optimisation of input-referred noise, bandwidth, and dynamic range.

4.1.2 DC Current Handling

The DC-servo loop is implemented according to the architecture of Fig. 3.10, comprising the integrator realising $H(s)$ and the transconductor stage generating the compensation current. As established in Section 2.4.4, the resistive nature of the R-TIA core permits $H(s)$ to be realised as a simple active integrator without a compensating zero.

To set the unity-gain frequency f_u of $H(s)$ at very low frequencies, a large input

resistance of $R_1 = 80\,\mathrm{G\Omega}$ is required at the integrator input. This resistance is implemented using a conventional MOS pseudo-resistor (PR) biased in the sub-threshold regime, as shown in Fig. 4.2. In contrast to the PN-junction feedback used in the TIA core, the PR here is employed in a non-critical position within the servo loop, where its flicker noise and bias sensitivity do not directly compromise the input-referred noise performance of the readout system. By selecting an integration capacitance of $C_{int} = 20\,\mathrm{pF}$, a unity-gain frequency of:

$$f_u \approx \frac{1}{2\pi R_1 C_{int}} \approx 0.1\,\mathrm{Hz} \tag{4.2}$$

is obtained, consistent with (3.26). The pole f_p is further pushed toward near-zero frequencies by the open-loop gain of the integrator op-amp, resulting in an ultra-low bandwidth for the DC-servo path.

The transconductor stage realises the effective compensation resistance R_{dc} through the PN-junction current-divider topology described in Section 3.3.1. To accommodate a maximum DC input current of $\pm 50\,\mathrm{nA}$ within the available output voltage swing, the effective resistance is set to $R_{dc} = 30\,\mathrm{M\Omega}$. This is achieved by selecting $R_2 = 200\,\mathrm{k\Omega}$ and a scaling factor of $M = 150$, giving:

$$R_{dc} = M \cdot R_2 = 150 \times 200\,\mathrm{k\Omega} = 30\,\mathrm{M\Omega} \tag{4.3}$$

The large scaling factor $M = 150$ satisfies the condition $M \gg 1$, validating the noise approximation of (3.33) and ensuring that the noise contribution of the transconductor input stage is suppressed by a factor of $M^2 = 22500$ when referred to the TIA input. The PMOS and NMOS transistors in the transconductor stage are configured with aspect ratios of $(W/L)_p = 1\,\mu\mathrm{m}/14\,\mu\mathrm{m}$ and $(W/L)_n = 1\,\mu\mathrm{m}/5\,\mu\mathrm{m}$ respectively.

The crossover frequency of the DC-servo loop, accounting for the voltage gain of 3 within the loop, is:

$$f_m \approx 10\, f_u \approx 1\,\mathrm{Hz} \tag{4.4}$$

consistent with (3.28).

The resulting frequency response of the implemented DC-servo filter $H(s)$ is shown in Fig. 4.3. The response exhibits the expected single-pole behaviour, with a high low-frequency gain and a pole located at approximately $6.5\,\mu\mathrm{Hz}$. At the DC-servo crossover frequency $f_m \approx 1\,\mathrm{Hz}$, the magnitude of $H(s)$ is approximately -20 dB, corresponding to the designed attenuation factor $\alpha = 10$. The attenuation increases further with frequency, reaching approximately -54 dB at $50\,\mathrm{Hz}$, thereby strongly suppressing AC signal components from propagating through the DC-compensation path.

The ultra-low crossover frequency ensures that the DC-servo loop effectively tracks and compensates slow DC baseline variations while having negligible influence on the AC signal band.

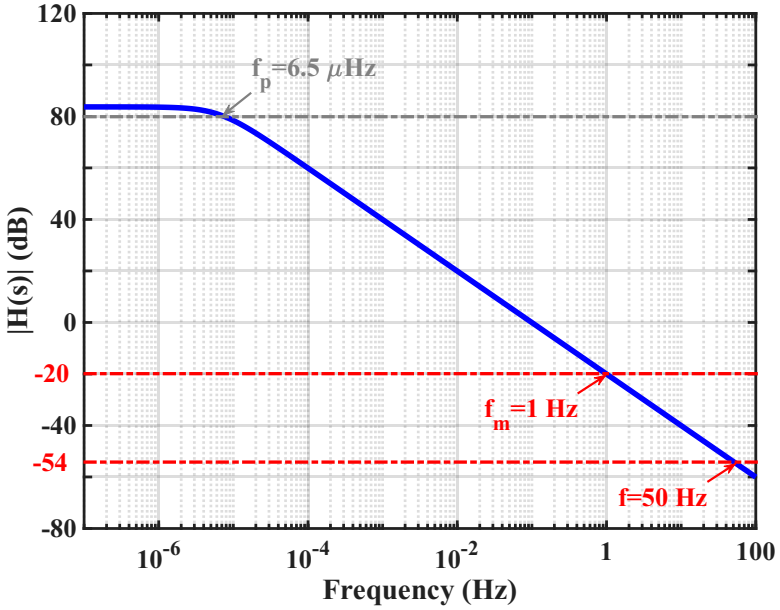


Figure 4.3: Simulated frequency response of the implemented DC-servo filter $H(s)$, showing the low-frequency pole f_p, the crossover frequency f_m, and the attenuation within the signal band.

4.2 Anti-Aliasing Filter

To prevent high-frequency signal components from aliasing into the signal band prior to digital conversion, an anti-aliasing filter (AAF) is implemented between the AC output of the AFE and the corresponding digitisation block. As established in Section 4.1.1, the TIA core bandwidth is by default set to 1 MHz, primarily to ensure sufficient phase margin in the DC-servo loop design. In nanopore sensing, the required signal bandwidth depends on the timescale of the translocation events, which can extend to the order of tens of microseconds. Accordingly, two cutoff frequencies, 20 kHz and 100 kHz, are provided to accommodate different acquisition requirements. The AAF limits the AC signal bandwidth to one of these two values prior to digitisation. In addition, a direct analog output provides access to the full-bandwidth TIA core output for off-chip digitisation when required. Since the output of the DC-handling path contains only the low-frequency component of the input current (below 100 Hz), no AAF is required on the DC path, and the filter is therefore applied exclusively to the AC signal path.

The AAF is implemented as a second-order unity-gain Sallen–Key (SK) low-pass filter, as shown in Fig. 4.4. The topology employs a general-purpose low-noise op-amp as the unity-gain buffer, with two series resistors R_1 and R_2 in the input path, a feedback capacitor C_1 from the output to the intermediate node, and a capacitor C_2 to ground at the non-inverting input. The transfer function is:

$$H(s) = \frac{1}{1 + s(R_1 + R_2)C_2 + s^2 R_1 R_2 C_1 C_2} \tag{4.5}$$

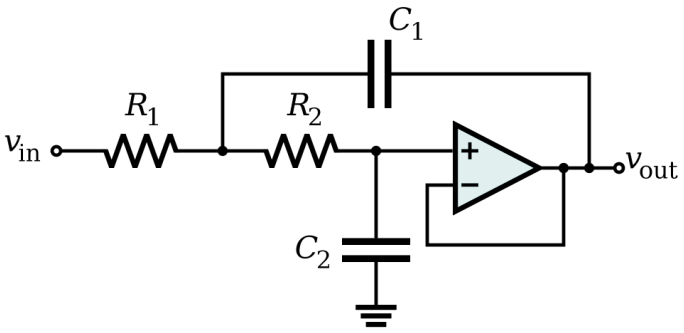


Figure 4.4: Schematic of the second-order unity-gain Sallen–Key anti-aliasing filter. The capacitor values are fixed at $C_1 = 70\,\text{pF}$ and $C_2 = 35\,\text{pF}$. The resistor value is $R = 33\,\text{k}\Omega$ for the 100 kHz mode and $R = 160\,\text{k}\Omega$ for the 20 kHz mode.

with a cutoff frequency and quality factor of:

$$f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}, \qquad Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{(R_1 + R_2)C_2} \tag{4.6}$$

Setting $R_1 = R_2 = R$, (4.6) simplifies to:

$$f_0 = \frac{1}{2\pi R\sqrt{C_1 C_2}}, \qquad Q = \frac{1}{2}\sqrt{\frac{C_1}{C_2}} \tag{4.7}$$

With $C_1/C_2 = 2$, this yields $Q = 1/\sqrt{2} \approx 0.707$, independent of R, which corresponds exactly to the Butterworth condition and provides a maximally flat magnitude response in the passband. The capacitor values are fixed at $C_1 = 70\,\text{pF}$ and $C_2 = 35\,\text{pF}$. The resistor value is set to $R = 33\,\text{k}\Omega$ for the 100 kHz mode and $R = 160\,\text{k}\Omega$ for the 20 kHz mode, yielding cutoff frequencies of 97.4 kHz and 20.1 kHz respectively. This ensures minimal passband distortion of the current-induced signal components while providing 40 dB per decade attenuation above the cutoff frequency to suppress out-of-band noise and prevent aliasing artefacts in the digitised output.

4.3 Delta-Sigma Modulator

The analog outputs of the AFE are continuous-time voltage signals proportional to the input current, which must be digitised for further signal processing, storage, and transmission. This is accomplished by an analog-to-digital converter (ADC), for which the $\Delta\Sigma$ architecture is particularly well-suited to the high-accuracy, low-bandwidth requirements of nanopore current readout for the following reasons. First, it achieves high resolution through oversampling and noise shaping rather than tight component matching, making it robust to process variations and well-suited for integration alongside sensitive analog circuitry [44]. Second, the possibility to trade bandwidth for resolution simply by adjusting the oversampling ratio offers significant design flexibility without hardware changes. Third, the inherent linearity arising from the use of a 1-bit quantiser—whose differential nonlinearity is zero

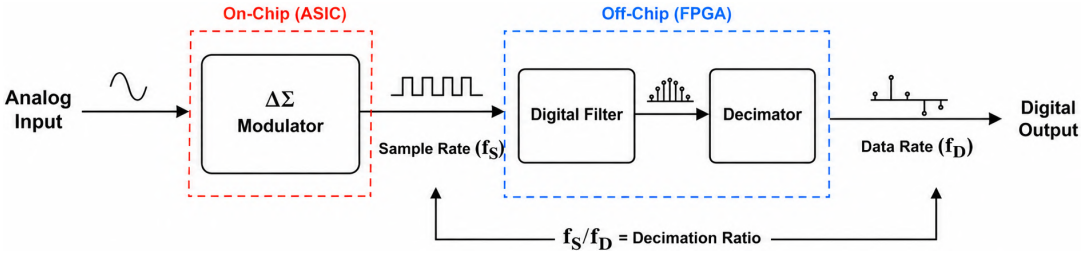


Figure 4.5: Block diagram of the ΔΣ ADC, showing the on-chip modulator (ASIC) operating at sampling rate f_s and producing a 1-bit output bitstream, and the off-chip digital/decimation filter implemented in the FPGA. The decimation ratio f_s/f_D determines the output data rate f_D and the achievable resolution.

by definition—ensures that the dynamic range of the analog front-end is faithfully preserved in the digital domain [44, 45].

The complete ΔΣ ADC consists of two functional parts, as illustrated in Fig. 4.5. The first is the on-chip ΔΣ modulator, implemented as part of the QC01a ASIC and described in this chapter. It operates at a high sampling rate f_s and converts the analog input into a 1-bit oversampled bitstream. The second is the off-chip digital/decimation filter, implemented in an FPGA, which removes the shaped out-of-band quantisation noise and downsamples the bitstream to produce a high-resolution multi-bit output word at the final data rate f_D. The ratio f_s/f_D is the decimation ratio, which determines the OSR and hence the achievable resolution. The FPGA implementation is described in Chapter 5.

4.3.1 Operating Principle and Noise Shaping

A ΔΣ modulator is an oversampling ADC that exploits both oversampling and noise shaping to achieve high resolution from a low-resolution (typically 1-bit) quantiser [44, 45]. Rather than sampling at the Nyquist rate, the modulator samples at a frequency f_s much higher than twice the signal bandwidth f_{BW}, defined by the oversampling ratio (OSR):

$$f_s = \mathrm{OSR} \cdot 2f_{BW} \tag{4.8}$$

Oversampling alone spreads the total quantisation noise power $\Delta^2/12$ (where Δ is the quantisation step) uniformly over the Nyquist band $[0, f_s/2]$, reducing the in-band noise power spectral density by a factor of OSR. For an N-bit quantiser with oversampling only, the signal-to-quantisation-noise ratio is [46]:

$$\mathrm{SQNR} = 6.02N + 1.76 + 10\log_{10}(\mathrm{OSR}) \quad [\mathrm{dB}] \tag{4.9}$$

and the corresponding ENOB improves as:

$$\mathrm{ENOB} = N + 0.5\log_2(\mathrm{OSR}) \tag{4.10}$$

showing that a fourfold increase in OSR yields only 0.5 extra bits of resolution — a modest improvement requiring impractically large OSR values for high-resolution

applications. Regardless of the modulator order, the ENOB is obtained from the SQNR through the standard conversion:

$$\text{ENOB} = \frac{\text{SQNR} - 1.76}{6.02} \tag{4.11}$$

This relation is used throughout to evaluate the effective resolution for different modulator orders and OSR configurations.

The key advantage of $\Delta\Sigma$ modulation over simple oversampling is *noise shaping*. Rather than distributing the quantisation noise uniformly across the Nyquist band, a negative feedback loop around the quantiser acts as a high-pass filter on the quantisation noise, suppressing it within the signal band and pushing it toward higher frequencies outside f_{BW}, where it is subsequently removed by the digital decimation filter. In the z-domain, this high-pass filtering is characterised by the *noise transfer function* (NTF):

$$NTF(z) = (1 - z^{-1})^L \tag{4.12}$$

where L is the modulator order. The NTF acts as an L-th order differentiator on the quantisation noise, providing increasingly aggressive suppression at low frequencies as L increases.

First-order modulator. The first-order modulator, shown in Fig. 4.6, comprises a difference amplifier, an integrator, a 1-bit comparator (ADC), and a 1-bit DAC in the negative feedback path. In the time domain, the output is:

$$y_i = x_{i-1} + (e_i - e_{i-1}) \tag{4.13}$$

where x_i is the input sample, y_i is the 1-bit output, and e_i is the quantisation error at sample i. The signal component x_{i-1} passes undistorted (delayed by one sample), while the quantisation noise term $(e_i - e_{i-1})$ corresponds to $NTF(z) = 1 - z^{-1}$ — a first-order high-pass filter that suppresses quantisation noise at low frequencies and shapes it toward high frequencies [45]. Integrating the shaped noise power from DC to f_{BW}, assuming a full-scale sinusoidal input, the SQNR for a first-order 1-bit modulator becomes:

$$\text{SQNR} = 6.02 + 1.76 - 5.17 + 30\log_{10}(\text{OSR}) \quad [\text{dB}] \tag{4.14}$$

Doubling the OSR now improves the SQNR by 9 dB (1.5 bits) — a substantial improvement over simple oversampling.

A practical limitation of the first-order modulator is the presence of *idle tones* (also known as limit cycles). For a near-zero DC input, the modulator output becomes a periodic sequence of ones and zeros, generating spurious tones at sub-harmonics of f_s that fall within the signal band and degrade the effective resolution.

Second-order modulator. To mitigate idle tones and further improve noise shaping, a second-order modulator is employed, using two cascaded integrators in the feedback loop, as shown in Fig. 4.7. The output of the second-order modulator is:

$$y_i = x_{i-1} + (e_i - 2e_{i-1} + e_{i-2}) \tag{4.15}$$

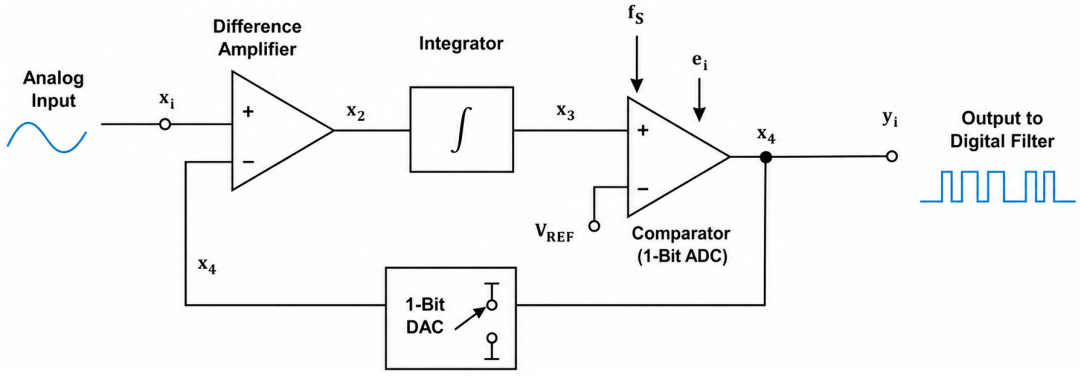


Figure 4.6: First-order $\Delta\Sigma$ modulator, comprising a difference amplifier, an integrator, a 1-bit comparator (ADC), and a 1-bit DAC in the negative feedback path. The feedback loop acts as a first-order high-pass filter ($NTF = 1 - z^{-1}$) on the quantisation noise.

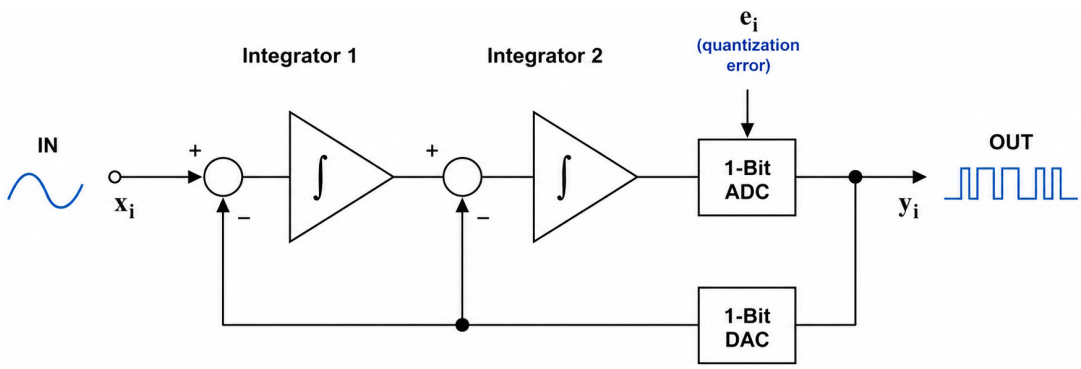


Figure 4.7: Second-order $\Delta\Sigma$ modulator with two cascaded integrators, a 1-bit ADC, and a 1-bit DAC feeding back to both summing nodes. The NTF $= (1 - z^{-1})^2$ provides second-order high-pass filtering of the quantisation noise.

The quantisation noise term $(e_i - 2e_{i-1} + e_{i-2})$ corresponds to $NTF(z) = (1 - z^{-1})^2$ — a second-order high-pass filter providing more aggressive suppression at low frequencies compared to the first-order case [45, 46]. For a full-scale sinusoidal input, integrating the second-order shaped noise over $[0, f_{BW}]$ yields [44]:

$$\text{SQNR} = 6.02 + 1.78 - 12.9 + 50\log_{10}(\text{OSR}) \quad [\text{dB}] \tag{4.16}$$

where each doubling of OSR improves the SQNR by 15 dB (2.5 bits) — substantially faster than the first-order case, making the second-order modulator the standard choice for high-resolution sensor interface applications.

4.3.2 On-Chip Implementation

The on-chip $\Delta\Sigma$ modulator is implemented as a fully-differential switched-capacitor (SC) circuit, as shown in Fig. 4.8. The fully-differential topology provides inherent rejection of common-mode noise and supply perturbations, which is critical for maintaining the low-noise performance of the readout system. The circuit operates on two non-overlapping clock phases, labelled P1 and P2 in the figure, generated by an on-chip phase generator from the input clock.

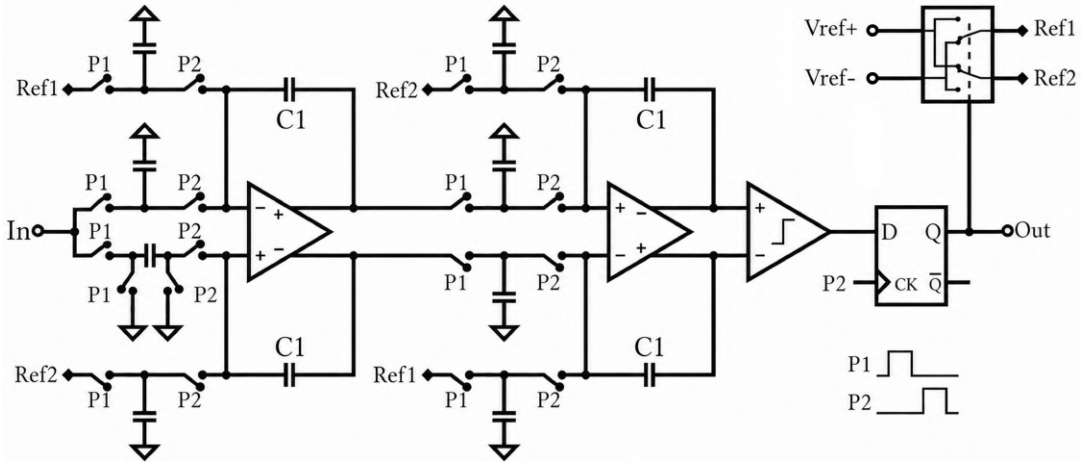


Figure 4.8: Schematic of the on-chip second-order fully-differential switched-capacitor $\Delta\Sigma$ modulator. The circuit comprises two cascaded SC integrator stages followed by a 1-bit quantiser and a reference multiplexer that closes the feedback loop. Clock phases (P1 and P2) are non-overlapping.

First integrator stage. The input signal is sampled onto the input capacitor during P1 and transferred to the differential feedback capacitor C_1 during P2, performing the integration operation. To improve loop stability and prevent integrator overload, the gain of the first integrator is halved relative to the second by reducing the ratio of the input sampling capacitor to C_1. The feedback reference charges — Ref1 during P1 and Ref2 during P2 — are injected directly into the summing node of this stage, implementing the 1-bit DAC feedback required by the $\Delta\Sigma$ loop.

Second integrator stage. The output of the first integrator is sampled and integrated by an identical SC stage with feedback capacitor C_1. The reference injection polarity is swapped relative to the first stage — Ref2 during P1 and Ref1 during P2 — as required by the second-order loop topology to maintain correct noise shaping.

1-bit quantiser. The output of the second integrator drives a single-threshold comparator, which determines the sign of the accumulated signal. The comparator output is registered by a D flip-flop clocked on P2, which serves two purposes: it synchronises the 1-bit output bitstream to the clock edge, and it breaks the direct combinational path around the feedback loop, ensuring the feedback reference is updated only once per clock cycle. The registered output Q constitutes the output bitstream, while the complementary output $\bar{Q}$ controls the reference multiplexer.

Reference multiplexer. The reference multiplexer selects between the positive reference V_{ref+} and negative reference V_{ref-} based on $Q/\bar{Q}$, generating the Ref1 and Ref2 voltages fed back to both integrator stages. The differential reference voltage is $V_{ref} = 1.2\,\mathrm{V}$, giving a total DAC step of $\Delta = 2V_{ref} = 2.4\,\mathrm{V}$ and a differential input range of $\pm 1.2\,\mathrm{V}$.

Clock and system integration. The ASIC receives an external master clock of 82 MHz, which is divided internally by a factor of 8, yielding a modulator sampling frequency of $f_s = 10.25\,\mathrm{MHz}$. Two identical and independent modulators are integrated per readout core: the first digitises the AC output of the TIA core, pre-

ceded by the on-chip anti-aliasing filter; the second digitises the DC output of the DC-handling feedback path directly, without an AAF, since this signal is inherently low-frequency. Both modulators can be independently disabled when an external ADC is preferred. The 1-bit bitstream produced by each modulator is routed to the FPGA digital back-end, where a sinc^3 decimation filter extracts the high-resolution output data at a rate determined by the configured OSR, as described in Chapter 5.

4.4 Programmable Bias Voltage Generator

The programmable bias voltage generator integrated into the ASIC serves two distinct functional roles within the readout system. The first is offset cancellation: unavoidable DC offsets arising from device mismatch, process variations, and electrode electrochemical potentials can shift the operating point of the analog front-end away from its nominal value, degrading the available dynamic range and potentially driving internal nodes toward saturation. By programming V_C to inject a compensating voltage at the appropriate node, these offsets can be nulled in situ without requiring external trimming components. The second role is sensor biasing: in electrochemical and nanopore sensing applications, a well-defined DC voltage must be applied across the sensor to establish the operating conditions for the measurement. In nanopore sensing specifically, this bias drives the ionic current through the pore and directly determines the open-pore current baseline I_0; any noise or instability on the applied voltage appears directly as a current noise contribution at the readout input [20], imposing stringent requirements on the voltage source quality. In both roles, the generator must simultaneously satisfy two conflicting requirements: a sufficiently wide output swing to cover the full range of offset and bias voltages encountered in practice, and a fine voltage resolution to enable precise adjustment with minimal quantisation noise. A single DAC of moderate word length cannot satisfy both requirements simultaneously without an impractical increase in bit count. The implemented architecture therefore combines a coarse and a fine voltage generation path, as illustrated in Fig. 4.9, achieving both wide output range and high-resolution adjustment within a compact on-chip implementation.

The generator comprises two independent 10-bit DACs, each operating with differential reference voltages of $\pm 512\,\mathrm{mV}$. The first DAC provides the main coarse voltage $V_{C,\mathrm{Main}}$, which sets the primary output level, while the second DAC provides a fine offset voltage $V_{C,\mathrm{Fine}}$ for high-resolution trimming. Both DAC outputs are individually buffered by unity-gain voltage followers before being combined through a weighted non-inverting summing amplifier, with input resistors $R_{1,\mathrm{Main}} = 10\,\mathrm{k\Omega}$ and $R_{1,\mathrm{Fine}} = 80\,\mathrm{k\Omega}$ for the coarse and fine paths respectively, and a common feedback resistor $R_2 = 10\,\mathrm{k\Omega}$. The resulting output voltage is:

$$V_C = V_{C,\mathrm{Main}} + \frac{1}{8} V_{C,\mathrm{Fine}} \tag{4.17}$$

The coarse path operates with unity gain, preserving the full output swing of the main DAC, while the fine path introduces an attenuation factor of 1/8, reducing the contribution of $V_{C,\mathrm{Fine}}$ to one-eighth of its nominal value. The maximum total

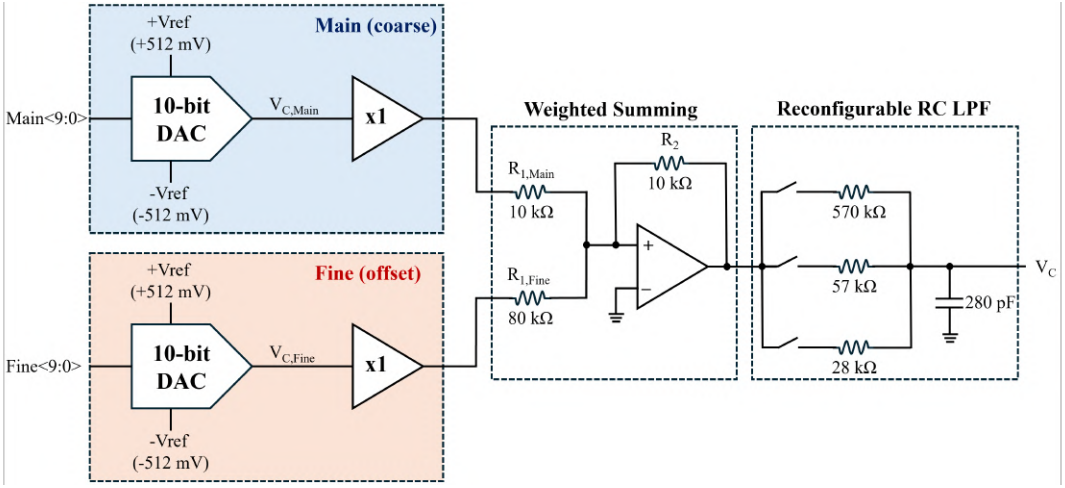


Figure 4.9: Block diagram of the programmable bias voltage generator, comprising two independent 10-bit DACs for coarse and fine voltage generation, unity-gain output buffers, a weighted non-inverting summing amplifier, and a reconfigurable first-order RC low-pass filter.

output range of V_C is consequently $\pm 576\,\mathrm{mV}$, comprising the $\pm 512\,\mathrm{mV}$ coarse range extended by the maximum $\pm 64\,\mathrm{mV}$ fine adjustment range.

For each 10-bit DAC operating over a full-scale span of $1024\,\mathrm{mV}$, the nominal voltage resolution of the coarse path is $\mathrm{LSB}_{\mathrm{Main}} = 1024\,\mathrm{mV}/2^{10} = 1\,\mathrm{mV}$. After the 1/8 attenuation introduced by the weighted summing network, the effective resolution of the fine adjustment path at the output becomes:

$$\mathrm{LSB}_{\mathrm{Fine}} = \frac{1\,\mathrm{mV}}{8} = 125\,\mu\mathrm{V} \tag{4.18}$$

This sub-millivolt resolution enables precise bias point adjustment and fine offset trimming in nanopore sensing experiments, where small variations in the applied membrane voltage directly affect both the open-pore current baseline and the translocation event amplitude.

The output of the summing amplifier is passed through a programmable first-order RC low-pass filter prior to being presented at the V_C output. The filter attenuates quantisation noise arising from the DAC conversion process and suppresses high-frequency switching artefacts, both of which would otherwise contribute voltage noise to the applied membrane bias or degrade the offset cancellation accuracy. The filter employs a fixed output capacitance of $C = 280\,\mathrm{pF}$ and three selectable series resistor branches of $R = 570\,\mathrm{k\Omega}$, $57\,\mathrm{k\Omega}$, and $28\,\mathrm{k\Omega}$, engaged individually through digitally controlled switches, yielding $-3\,\mathrm{dB}$ cutoff frequencies of approximately 1 kHz, 10 kHz, and 20 kHz respectively according to $f_c = 1/(2\pi RC)$. The narrowest bandwidth setting provides the lowest output noise floor and is the preferred configuration for DC-biased nanopore measurements, while the wider settings accommodate applications requiring faster voltage settling or dynamic bias adjustment. When a noise floor below 1 kHz is required, an external capacitor can be connected to the V_C output pin, augmenting the on-chip capacitance and further reducing the cutoff frequency without any additional on-chip resources.

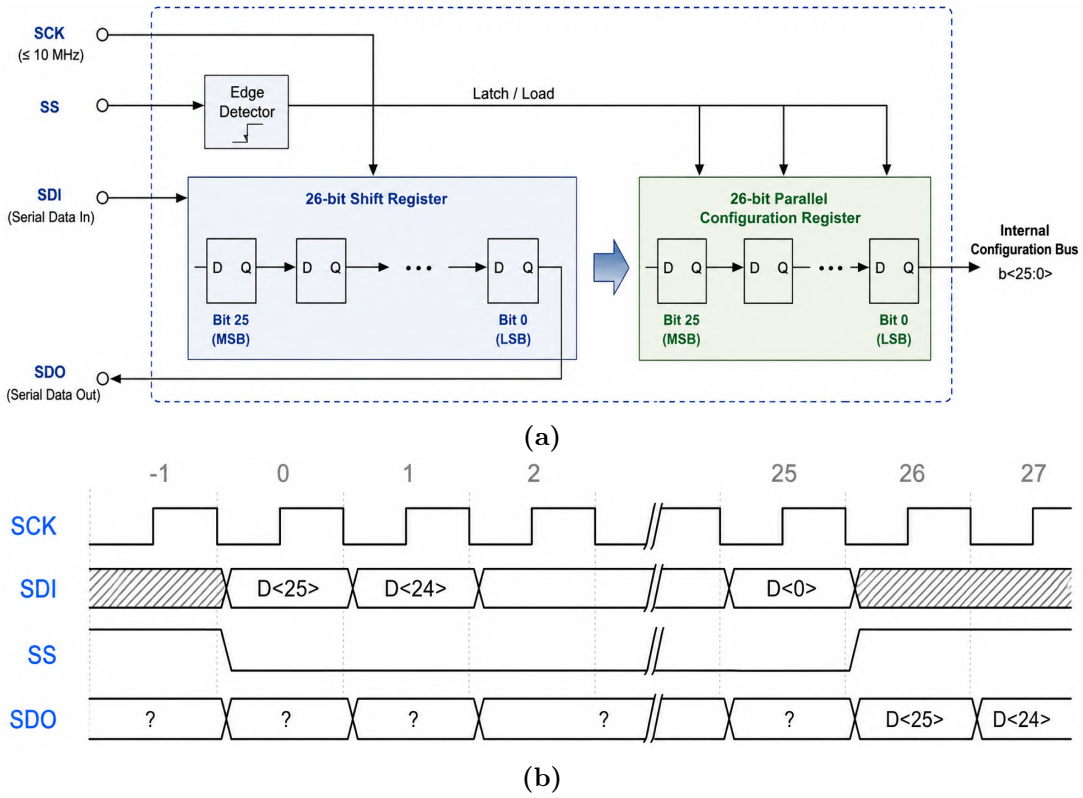


Figure 4.10: 26-bit SPI configuration interface: (a) block structure, showing the 26-bit shift register, parallel configuration register, edge detector, and internal configuration bus b⟨25:0⟩; (b) timing diagram of a complete 26-bit transaction, showing the SCK clock, SDI data sequence, SS enable signal, and SDO readback output. Data is sampled on the rising edge of SCK and latched into the configuration register on the rising edge of SS.

The generator also supports two alternative operating modes to accommodate different experimental configurations. In the first, when the membrane bias is applied externally from the opposite terminal of the sensor, the V_C output is programmed to the system common-mode voltage, ensuring that the on-chip signal path remains correctly referenced without interfering with the externally applied bias. In the second, the generator can be disabled entirely by opening all switches in the RC filter network, in which case the V_C output is internally connected to the fixed common-mode voltage, providing a stable reference at the sensor interface regardless of the DAC state. The complete generator is programmed via the on-chip SPI interface, which sets the DAC codes for both paths, the filter bandwidth selection, and the operating mode, enabling fully integrated generation of calibrated low-noise bias voltages suitable for both offset cancellation and direct sensor biasing without external instrumentation.

4.5 SPI Configuration Interface

All configurable parameters of the ASIC are programmed through an on-chip serial peripheral interface (SPI), which provides a compact and robust digital control path without requiring additional parallel bus routing across the die. Each readout core is equipped with an independent 26-bit SPI interface, allowing the two cores to be configured simultaneously or independently as required by the measurement scenario.

The interface follows a standard synchronous serial protocol, as illustrated in Fig. 4.10. Three dedicated pins are used per core: the serial data input (SDI), the slave select (SS), and the serial clock (SCK). The SCK pin is shared between both cores and supports a maximum operating frequency of 10 MHz. Data on the SDI line is sampled on the rising edge of SCK, with transmission proceeding from the most significant bit (bit 25) down to the least significant bit (bit 0). As shown in Fig. 4.10(a), the 26-bit shift register is implemented as a chain of D flip-flops clocked by SCK. When SS returns high at the end of a complete 26-bit transaction, the rising edge is detected and the full 26-bit word is latched in parallel into the configuration register, simultaneously updating all configuration bits on the internal bus $b\langle 25{:}0\rangle$. If SS goes high before all 26 bits have been shifted in, the received data is discarded and the configuration register retains its previous state. A serial data output (SDO) pin provides readback capability by reflecting the shift register contents, as shown in Fig. 4.10(b), enabling verification of the programmed configuration and supporting daisy-chain operation. The SDO pin remains in a high-impedance (Hi-Z) state when SS is deasserted, releasing the bus between transactions.

The SPI interface enables complete in-system reconfigurability of the readout chain, allowing the ASIC to be optimised for the target application by adjusting the signal bandwidth, noise performance, and dynamic range of the analog front-end, as well as controlling the bias voltage for sensor biasing or offset cancellation, without requiring any physical hardware changes.

4.6 Physical Layout

The physical layout of an integrated circuit is a critical step in the design process that bridges the gap between the circuit schematic and the fabricated silicon. Non-ideal layout effects—including parasitic capacitances, substrate noise coupling, device mismatch arising from process gradients, and leakage currents through unintended conduction paths—can significantly degrade the performance of the fabricated circuit relative to simulation predictions, particularly in ultra-low-noise analog front-ends where the signals of interest are at the pA level. Careful layout design is therefore essential to preserve the noise, bandwidth, and dynamic range performance established at the circuit level.

The QC01a ASIC layout was designed using Tanner EDA tools and verified against the design rule check (DRC) and layout-versus-schematic (LVS) requirements of the

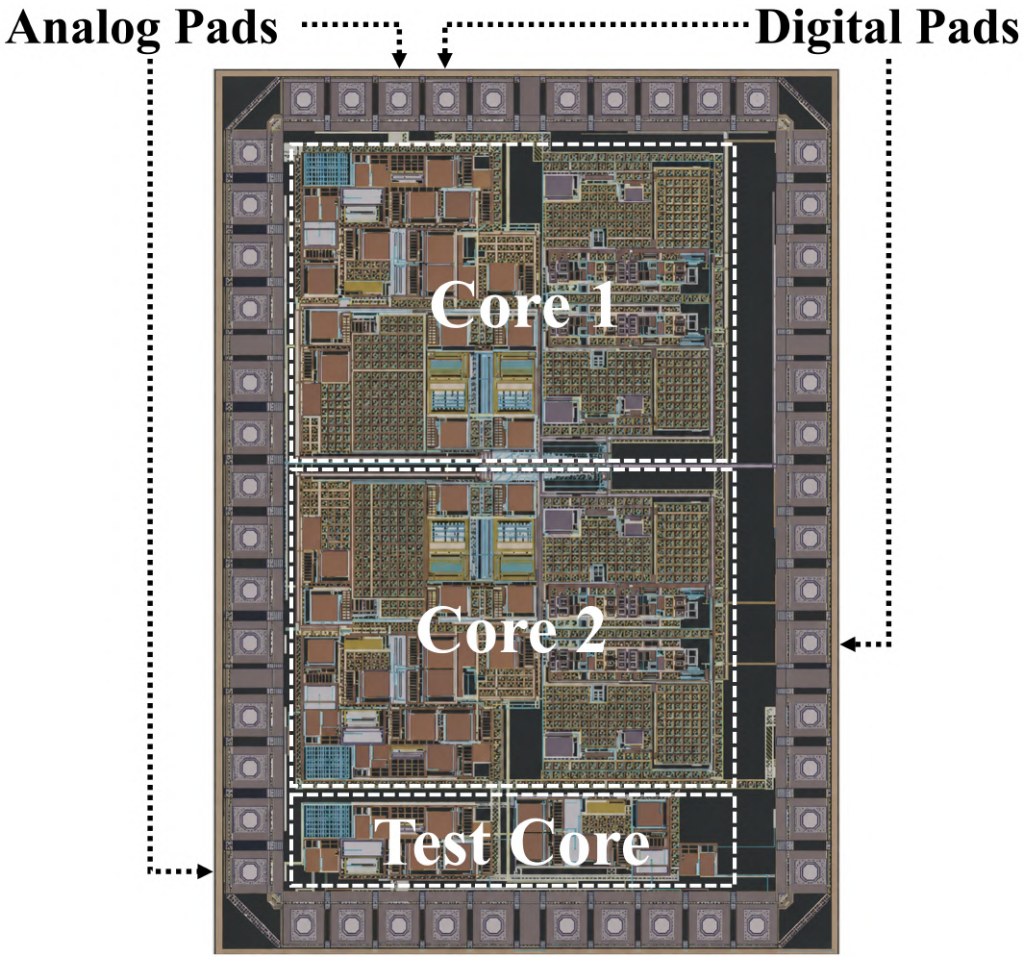


Figure 4.11: Physical layout of the QC01a ASIC (2.6 mm × 3.75 mm), designed in the X-Fab 0.35 µm CMOS technology.

X-Fab 0.35 µm CMOS process using Calibre. The physical layout of the ASIC is shown in Fig. 4.11. The die occupies an area of 2.6 mm × 3.75 mm (9.75 mm^2) and employs the following process modules: MOS, ISOMOS, CAPPOLY, HRPOLY, XRPOLY, DMIM, and METAL4. The die is organised into three vertically stacked regions: two identical readout cores (Core 1 and Core 2) occupying the upper and middle portions of the die respectively, and a dedicated test core in the lower portion. Core 1 and Core 2 are placed symmetrically about the horizontal axis of the die and implement the complete readout chain described in this chapter; they can be operated independently or in parallel. The test core provides independent access to the AC processing unit and the DC handling unit as separate stand-alone blocks, facilitating targeted electrical characterisation of individual circuit stages during experimental validation. The pad ring is organised to achieve a clear physical separation between analog and digital signals. Analog pads are grouped along the left side of the die, placing the sensitive analog input and output nodes as far as possible from the digital switching activity. Digital pads, carrying the SPI interface signals, clock, and digital outputs, are grouped along the right side of the die. The analog and digital supply voltages are routed through independent pad cells and separate on-chip metal tracks, preventing switching noise on the digital supply from coupling

into the sensitive analog signal path through the power distribution network. The bottom pad row serves the test core and provides dedicated access to its individual circuit blocks. The analog input pads are implemented without ESD protection structures, in contrast to standard pad cell practice. This deliberate choice eliminates the leakage current and parasitic capacitance introduced by ESD diodes at the TIA input node, both of which would directly degrade the noise performance and measurement resolution of the readout system at pA-level input currents. As a consequence, appropriate electrostatic discharge handling precautions must be observed during PCB assembly and measurement to protect the unguarded input nodes.

Several layout techniques were applied systematically throughout the design to mitigate non-ideal effects arising from process gradients, device mismatch, and parasitic coupling, as described in the following.

Analog-digital separation and shielding. The analog and digital circuit blocks are physically separated on the die, with the sensitive AFE placed away from the digital logic and the $\Delta\Sigma$ modulator. Rather than shielding the analog input routing directly, digital signal tracks are routed physically away from the analog input nodes and are individually enclosed by grounded metal shields, containing the switching noise at the source and preventing it from coupling into the sensitive analog signal paths. Routing of digital or other signal lines over the analog layout area is avoided throughout.

Deep-well isolation. To enhance substrate isolation and minimise leakage currents, all transistors in the current preamplifier and transconductor stages are implemented using deep-well isolation structures (ISOMOS module), as illustrated in Fig. 4.12. Each transistor is enclosed within a deep P-well ring that electrically isolates it from the global substrate, allowing independent body biasing and effectively suppressing both substrate noise injection and leakage through parasitic conduction paths at the sensitive TIA input node.

Common-centroid and interdigitated placement. The PN-junction feedback and replica transistor pairs in the current amplifier, whose matching directly determines the accuracy of the current gain N, are laid out in a common-centroid arrangement with interdigitated fingers. This configuration ensures that both devices of each matched pair share the same centroid and are therefore equally affected by any linear process gradients in threshold voltage, oxide thickness, or carrier mobility across the die, minimising systematic mismatch [33, 46]. The DMIM feedback capacitors C_1 and compensation capacitors C_2 are similarly arranged in common-centroid arrays to suppress gradient-induced capacitance mismatch, which would otherwise translate directly into gain and bandwidth errors in the TIA core.

Dummy devices. Dummy transistors are placed at the periphery of each matched transistor array, and dummy capacitor cells are placed at the boundaries of each DMIM capacitor array. This ensures that all active fingers and capacitor cells experience identical boundary conditions, eliminating the asymmetric edge effects that would otherwise affect the outermost elements and introduce systematic mismatch between nominally identical devices [46].

Multi-finger layouts. Wide transistors throughout the design are implemented us-

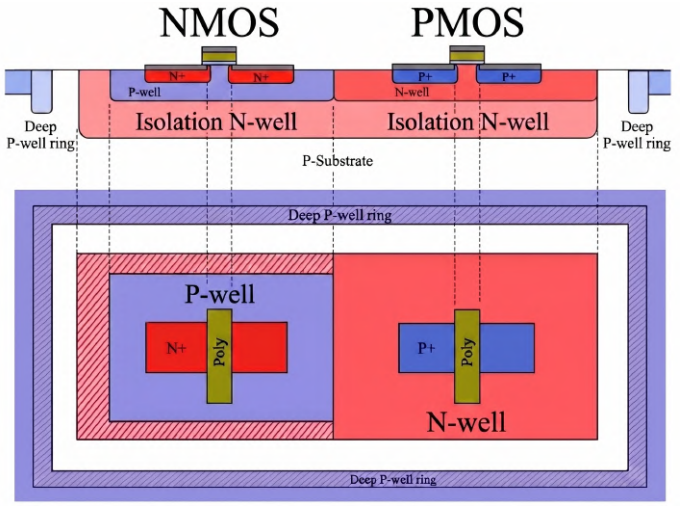


Figure 4.12: Cross-section (top) and layout (bottom) of isolated NMOS and PMOS devices implemented within a deep N-well surrounded by a deep P-well ring (ISOMOS module), providing electrical isolation from the global substrate for all transistors connected to the sensitive TIA input node.

ing multi-finger layouts, splitting the total width into multiple parallel fingers. This reduces the drain and source diffusion capacitances—which scale with the number of diffusion-to-substrate junctions—and lowers the distributed gate resistance, both of which contribute to the parasitic input capacitance C_{in} and the high-frequency noise performance of the readout front-end.

Matched interconnections. Within the current amplifier, the metal routing connecting matched transistor pairs is designed to be symmetric, ensuring that the parasitic resistance and capacitance of the interconnect are identical for each device in a matched pair. Asymmetric interconnect impedances would otherwise introduce a systematic current offset between the primary and replica branches, degrading the linearity of the current gain. Guard rings surround all sensitive analog blocks, providing an additional barrier against substrate noise injection from adjacent circuit regions.

4.7 Summary

This chapter has described the implementation of the proposed current readout system as a monolithic ASIC, designated QC01a, designed in the X-Fab 0.35 µm CMOS process. The chip integrates two identical readout cores, each implementing the DC-compensated TIA architecture proposed in Chapter 3. The analog front-end realises the separate signal paths for AC and DC current processing. Supporting blocks include a second-order Sallen–Key anti-aliasing filter with selectable cutoff frequencies, two second-order fully-differential $\Delta\Sigma$ modulators independently digitising the AC and DC signal paths, a programmable bias voltage generator serving both offset cancellation and sensor biasing, and a 26-bit SPI configuration interface for complete in-system reconfigurability. The physical layout was designed in Tan-

ner EDA and verified using Calibre DRC and LVS. Experimental characterisation of the fabricated system is presented in Chapter 5.

Chapter 5

System Integration and Characterisation

The preceding chapter described the circuit-level design and physical layout of the QC01a ASIC. Translating this design into a fully operational readout system requires its integration into a complete measurement platform, encompassing the packaged chip, a dedicated printed circuit board (PCB), and the associated digital signal processing infrastructure. This chapter presents the system-level integration of the QC01a ASIC and its experimental characterisation. The chapter opens with the chip micrograph and packaging, confirming the physical realisation of the fabricated device. The PCB platform developed to interface the ASIC with external instrumentation is then described, including the hardware architecture and the FPGA-based decimation filter implementing the digital back-end of the $\Delta\Sigma$ ADC. The chapter concludes with the experimental characterisation of the complete integrated system, covering the noise, bandwidth, dynamic range, and DC compensation performance of the fabricated readout platform.

5.1 Fabricated ASIC

The QC01a ASIC was fabricated through the X-Fab 0.35 µm CMOS. The chip micrograph of the fabricated die is shown in Fig. 5.1(a), together with a zoom inset identifying the chip designation and author inscription. The two readout cores and the test core are clearly visible, confirming the symmetric floorplan described in Section 4.6. The annotated micrograph of a single readout core is shown in Fig. 5.1(b), with the functional blocks identified. Each core occupies an area of 1.82 mm × 1.35 mm (2.457 mm^2).

The area breakdown of a single readout core is illustrated in Fig. 5.1(c). The $\Delta\Sigma$ modulators collectively occupy the largest fraction of the core area at 32.8 %, owing to the large switched-capacitor arrays required for high-resolution analog-to-digital conversion. The programmable bias voltage generator is the second largest block at 25.6 %; its area is dominated by the 280 pF on-chip capacitor of the reconfigurable

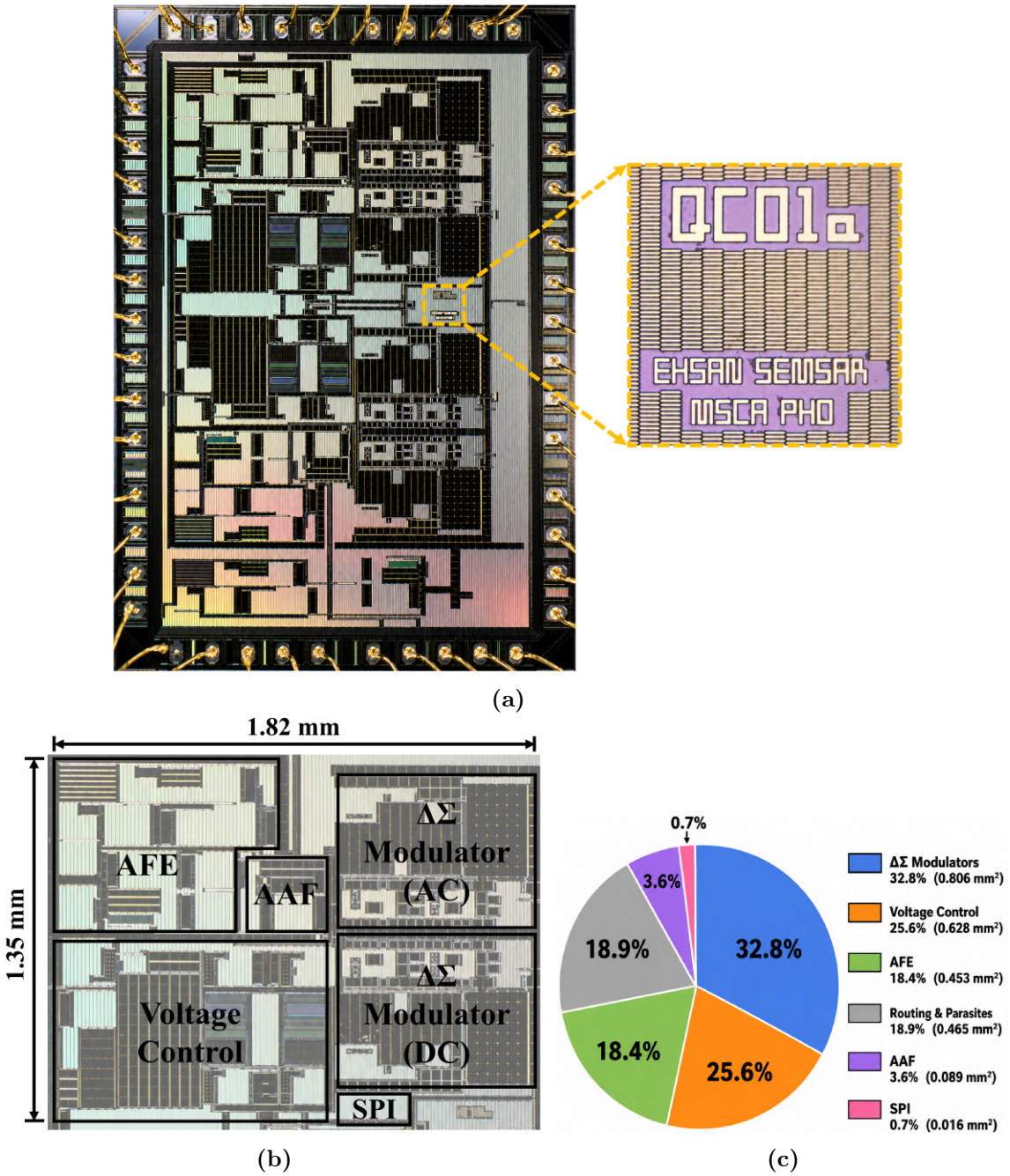


Figure 5.1: QC01a ASIC: (a) full die micrograph with wire bonds and zoom inset showing the chip identification label; (b) annotated micrograph of a single readout core (1.82 mm × 1.35 mm), with functional blocks identified; (c) area breakdown of a single readout core.

RC low-pass filter at the output stage, which requires a large CAPPOLY structure to achieve the required capacitance density. The AFE occupies 18.4 % of the core area, reflecting the area consumed by the deep-well isolated transistor arrays, the DMIM feedback and compensation capacitors, and the pseudo-resistor integrator of the DC-servo loop. The remaining area (18.9 %) is attributed to routing, guard rings, decoupling capacitors, and inter-block spacing. The AAF and SPI interface

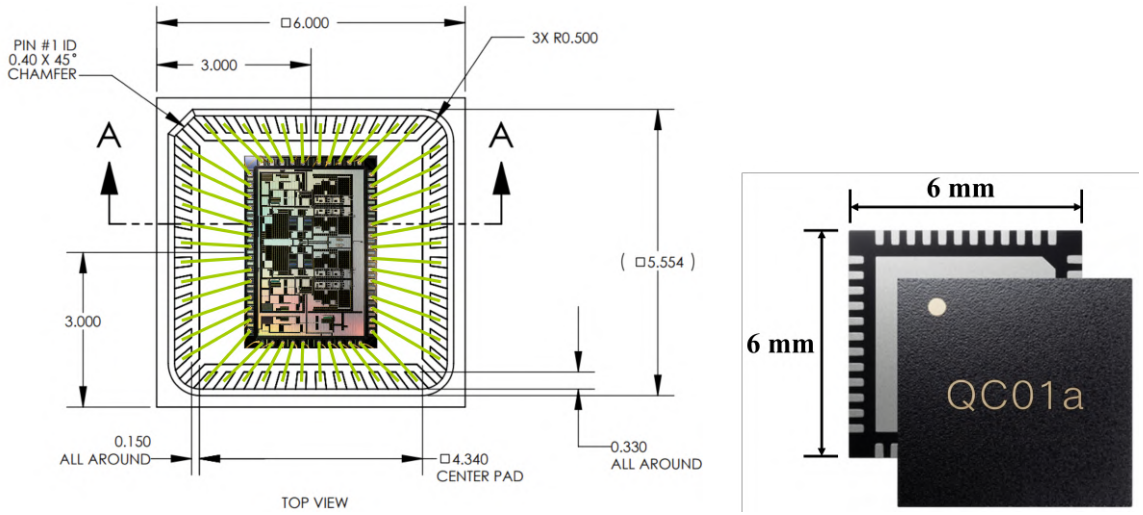


Figure 5.2: QC01a ASIC packaging: (a) bonding diagram showing the die mounted on the 4.34 mm center pad of the QFN48 package, with wire-bond connections to the 48 leads at 0.4 mm pitch; (b) photograph of the packaged QC01a ASIC in the QFN48 6 mm × 6 mm package.

together account for less than 5 % of the core area, consistent with their relatively simple circuit topologies.

5.2 Packaging

The QC01a ASIC is housed in a QFN48 package with a 6 mm × 6 mm footprint and a 0.4 mm lead pitch, conforming to the JEDEC MO-220 standard. The QFN package was selected for its compact footprint, low parasitic inductance and capacitance of the lead frame, and the exposed center pad which provides a low-impedance thermal and electrical connection to the PCB ground plane. These properties make it well-suited for a low-noise analog readout application, where minimising parasitic impedances at the package interface is critical to preserving the noise performance of the on-chip circuitry. The lead frame is fabricated from copper with electroless nickel and gold plate finish, ensuring reliable wire-bond adhesion and solderability.

The die is mounted on a 4.34 mm × 4.34 mm center pad and connected to the 48 package leads via gold wire bonds, as illustrated in the bonding diagram of Fig. 5.2(a). The wire bonds are distributed across all four sides of the die, with the analog input bonds kept as short as possible to minimise the parasitic inductance and capacitance introduced at the most noise-sensitive nodes of the readout chain. Pin 1 is identified by a 0.40 mm × 45° chamfer on the package corner, as visible in Fig. 5.2(b). The complete pin assignment and detailed package mechanical drawings, including the bottom land pattern and package cross-section, are provided in the Appendix.

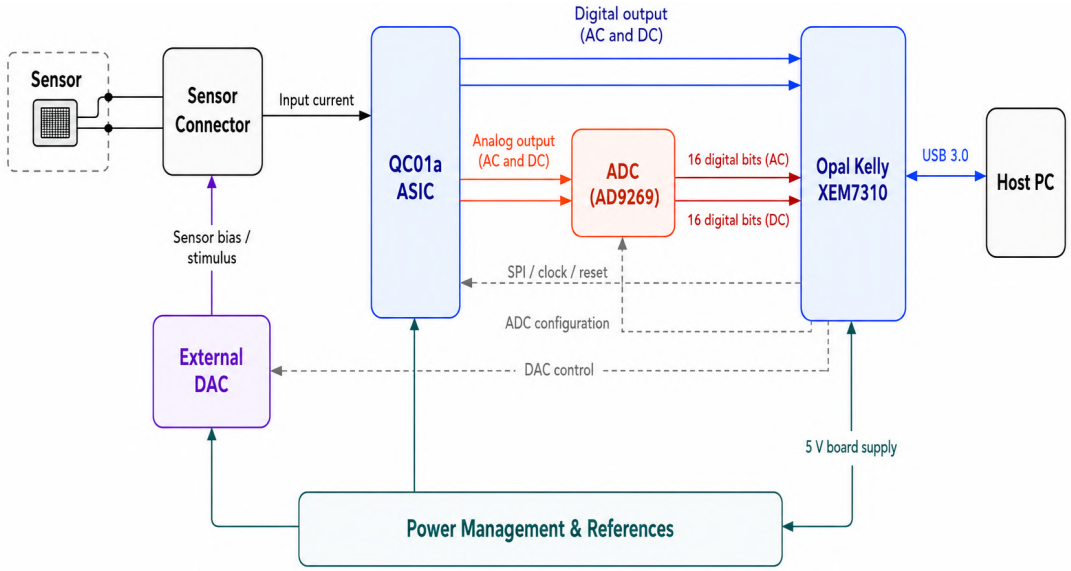


Figure 5.3: Top-level block diagram of the QC01a readout platform, showing the sensor interface, QC01a ASIC, external DAC, external ADC, Opal Kelly XEM7310 digital back-end, and power-management and reference circuitry.

5.3 PCB Readout Platform

To provide a complete system-level validation environment for the QC01a ASIC, a dedicated printed circuit board (PCB) platform was developed. The board integrates all hardware required for ASIC configuration, sensor interfacing, signal conditioning, digitisation, and data transfer to a host computer. The top-level block diagram of the platform is shown in Fig. 5.3, and a photograph of the assembled board is shown in Fig. 5.4.

The sensor interface is realised through a shielded connector, which routes the sensor current signals to the ASIC inputs. Its shielded construction helps minimise external interference at the highly sensitive input nodes of the readout system.

The QC01a ASIC is the central component of the platform, performing current-to-voltage conversion, anti-aliasing filtering, and analog-to-digital conversion through its on-chip $\Delta\Sigma$ modulators, as described in Chapter 4. The digital AC and DC output bitstreams are routed directly to the FPGA digital back-end for decimation filtering and data transfer.

The bandwidth of the on-chip $\Delta\Sigma$ conversion path is limited to approximately 100 kHz, since its high-resolution operation relies on oversampling and therefore requires a sufficiently large oversampling ratio. To enable acquisition over the wider bandwidth available from the analog signal path, the readout board incorporates a commercial dual-channel AD9269 ADC from Analog Devices. The AD9269 is a 16-bit converter based on a multistage differential pipeline architecture with output error correction, providing substantially higher conversion rates than the on-chip $\Delta\Sigma$ modulators. The AD9269 accepts a differential analog input with a full-scale range of approximately 2 V_{pp}. Since the QC01a analog output is single-ended and

spans approximately from −1.65 V to 1.65 V, a differential driver is placed between the ASIC and the ADC. This stage converts the single-ended signal into a differential signal, establishes the common-mode level required by the ADC, and scales the signal amplitude to fit within the ADC full-scale input range. Prior to digitisation, an external anti-aliasing filter is also included in the analog acquisition path. The filter is reconfigurable, allowing the analog acquisition bandwidth to be selected according to the measurement requirements. In the implemented platform, the ADC is operated at a sampling rate of 3.3 MS/s, enabling digitisation of the wide-bandwidth analog outputs of the ASIC. The differential driver and external anti-aliasing filter are omitted from the simplified top-level block diagram in Fig. 5.3 for clarity. The two 16-bit digital output buses corresponding to the AC and DC acquisition paths are subsequently routed to the FPGA for data processing and transfer to the host computer.

An external 16-bit DAC provides a programmable bias voltage as an alternative to the on-chip stimulus generator. The DAC output is buffered and filtered by a second-order Sallen–Key low-pass filter with a cutoff frequency of 20 kHz, followed by an additional RC low-pass stage. This final RC stage can be bypassed to retain the 20 kHz cutoff frequency set by the Sallen–Key filter, or reconfigured to provide additional low-pass filtering down to approximately 16 Hz. This allows the bandwidth of the applied sensor bias to be adjusted according to the measurement requirements. For measurements requiring a quasi-DC bias, the external DAC can be set to the system common-mode voltage $V_{cm} = 1.65\,\mathrm{V}$, while the final RC stage is configured to provide the lowest cutoff frequency of approximately 16 Hz, thereby strongly suppressing high-frequency noise on the applied bias.

The digital back-end is implemented using an Opal Kelly XEM7310 module hosting a Xilinx Artix-7 FPGA. The FPGA acquires the digital outputs from both the on-chip $\Delta\Sigma$ modulators and the external ADC, and performs the required digital processing before transferring the acquired data to the host computer through the USB 3.0 interface provided by the XEM7310 module. In addition to data acquisition, the FPGA provides the digital configuration and control signals required by the readout platform. These include the SPI, clock, and reset signals for the QC01a ASIC, configuration signals for the external ADC, and digital control of the external DAC used for sensor bias generation.

The readout platform is powered by an external 5 V adapter connected to the Opal Kelly XEM7310 module. The 5 V supply is then distributed to the readout board and filtered into separate analog and digital power domains. Dedicated regulation and filtering subsequently generate the supply and reference voltages required by the different subsystems. A low-noise regulator generates the common-mode voltage $V_{cm} = 1.65\,\mathrm{V}$ used throughout the analog signal chain. For the QC01a ASIC, separate regulators generate the 3.3 V analog and digital supply rails, helping to isolate the sensitive analog circuitry from digital switching noise. Precision reference voltages $V_{\mathrm{refH}} = 2.162\,\mathrm{V}$ and $V_{\mathrm{refL}} = 1.138\,\mathrm{V}$ required by the ASIC are generated by dedicated reference circuitry based on a 1.024 V precision voltage reference. The external ADC section similarly employs dedicated local regulators to generate its 1.8 V and 3.3 V supply rails from the filtered 5 V board supply.

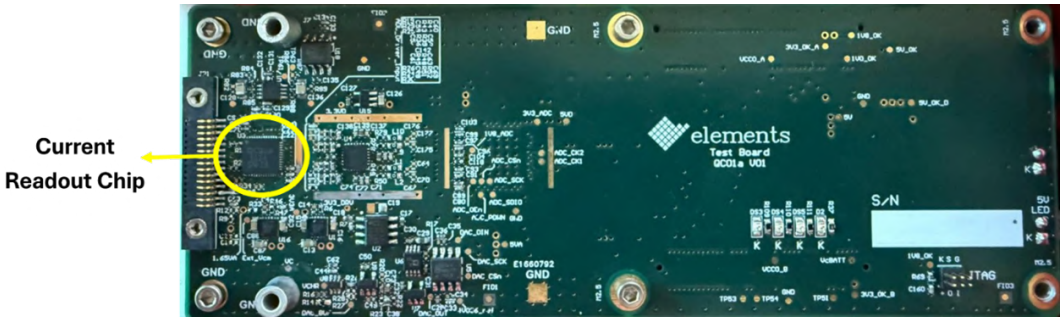


Figure 5.4: Photograph of the assembled QC01a readout board, with the QC01a ASIC highlighted.

5.4 FPGA Digital Back-End

The FPGA digital back-end supports both acquisition paths of the readout platform. When the on-chip $\Delta\Sigma$ modulators are used, the FPGA receives continuous 1-bit oversampled bitstreams and applies sinc^3 digital filtering and decimation to obtain high-resolution output samples. The selected oversampling ratio (OSR) determines the output data rate and the corresponding digital bandwidth–resolution trade-off. In contrast, when the external ADC is used, the FPGA directly acquires the parallel 16-bit output data without requiring $\Delta\Sigma$ decimation. The remainder of this section describes the clock and synchronisation scheme, the sinc^3 decimation filter, the achievable bandwidth–resolution trade-offs, and the transfer of the acquired data to the host computer.

5.4.1 Clock and Synchronisation

The QC01a ASIC is clocked by a master clock of 82 MHz generated by the FPGA. This clock is divided internally by a factor of 8, yielding a $\Delta\Sigma$ modulator sampling frequency of $f_s = 10.25\,\text{MHz}$. The clock is shared across the on-chip modulators and other digital blocks of the ASIC. The four on-chip $\Delta\Sigma$ modulators produce continuous 1-bit digital output streams corresponding to the AC and DC signal paths of the two readout cores. Two synchronisation signals are provided by the ASIC: one associated with the AC digital outputs and one associated with the DC digital outputs. The FPGA uses these synchronisation signals to capture the corresponding 1-bit streams prior to digital filtering and decimation. The FPGA also provides a reset signal to initialise the $\Delta\Sigma$ modulators before each measurement.

The external ADC operates in a separate clock domain and is driven by a dedicated 80 MHz differential clock source implemented on the readout board. The ADC provides corresponding data-clock signals together with its two 16-bit digital output buses, allowing the FPGA to synchronously capture the converted AC and DC data.

5.4.2 Sinc^3 Decimation Filter

The one-bit output bitstream of the $\Delta\Sigma$ modulator contains the input signal together with shaped quantisation noise, which is shifted towards higher frequencies by the second-order noise-shaping loop, as described in Section 4.3.1. The digital back-end performs two operations to recover a high-resolution output signal [45]. First, a low-pass digital filter attenuates the high-frequency shaped quantisation noise while preserving the signal band. The filtered signal is then decimated to reduce the output data rate to a useful value.

The high-rate filter output is downsampled by retaining one sample every OSR input samples. The ratio between the modulator sampling frequency f_s and the resulting output sampling rate f_{SR} defines the oversampling ratio:

$$\mathrm{OSR} = \frac{f_s}{f_{SR}} \tag{5.1}$$

For a fixed f_s, increasing the OSR reduces the output sampling rate and the corresponding signal bandwidth, while reducing the integrated in-band quantisation noise and thereby improving the theoretical resolution [45].

The digital filter is implemented as a sinc^3 filter, which is well suited to second-order $\Delta\Sigma$ modulators [44]. Sinc filters belong to a class of averaging filters with a frequency response of the form $\mathrm{sinc}^k(f)$ [45]. The sinc^3 filter can be interpreted as the cascade of three first-order sinc filters. Its frequency response exhibits deep nulls at integer multiples of the output sampling rate f_{SR}, providing strong attenuation of the out-of-band quantisation noise. The $-3\,\mathrm{dB}$ bandwidth of the sinc^3 filter is related to the output sampling rate f_{SR} by:

$$f_{-3\mathrm{dB}} = 0.262 \times f_{SR} \tag{5.2}$$

The OSR is configurable in the FPGA, allowing the output sampling rate and digital signal bandwidth to be adjusted over a wide range without modification of the analog hardware.

5.4.3 Operating Modes and Resolution

The achievable signal bandwidth and resolution are jointly determined by the OSR configured in the FPGA decimation filter. With the modulator sampling frequency of $f_s = 10.25\,\mathrm{MHz}$, increasing the OSR reduces the output sampling rate f_{SR} and the signal bandwidth, while improving the theoretical resolution by reducing the integrated in-band quantisation noise. The ENOB values are derived from (4.16) and (4.11). The achievable bandwidth and resolution across the full range of supported OSR configurations are summarised in Table 5.1. The full range of configurable output sampling rates spans from $1.25\,\mathrm{kHz}$ ($\mathrm{OSR} = 8192$) to $205\,\mathrm{kHz}$ ($\mathrm{OSR} = 50$), providing a range of bandwidth–resolution trade-offs suited to different sensing applications. For nanopore sensing applications requiring high temporal resolution, $\mathrm{OSR} = 50$ ($f_{SR} \approx 205\,\mathrm{kHz}$, $\mathrm{BW} \approx 53.7\,\mathrm{kHz}$, $13\,\mathrm{bits}$, $\mathrm{LSB} \approx 0.5\,\mathrm{pA}$) provides a suitable balance between bandwidth and resolution. The LSB column quantifies the

Table 5.1: Achievable output sampling rate, −3 dB signal bandwidth, theoretical ENOB, and current LSB of the sinc^3 decimation chain as a function of OSR. The modulator sampling frequency is $f_s = 10.25\,\text{MHz}$ (main clock 82 MHz, divided internally by 8). ENOB values are derived from (4.16) and (4.11). The LSB is defined as $V_{FS}/(2^{ENOB} \times NR_{out}A_v)$, with $V_{FS} = 1.2\,\text{V}$, $NR_{out} = 100\,\text{M}\Omega$, and $A_v = 3$ (post-amplifier voltage gain), giving a total transimpedance of 300 MΩ. At high OSR, the analog noise floor limits the achievable resolution in practice.

OSR	f_{SR}	**−3 dB BW**	**ENOB (bit)**	**LSB**
8192	1.25 kHz	0.33 kHz	31.4	<0.01 fA
4096	2.5 kHz	0.66 kHz	28.9	0.01 fA
2048	5 kHz	1.31 kHz	26.4	0.05 fA
1024	10 kHz	2.62 kHz	23.9	0.26 fA
512	20 kHz	5.25 kHz	21.4	1.48 fA
200	51.25 kHz	13.4 kHz	18.0	15.6 fA
100	102.5 kHz	26.9 kHz	15.5	88.0 fA
50	205 kHz	53.7 kHz	13.0	0.50 pA

minimum resolvable current step of the digitisation chain for each configuration, defined as $V_{FS}/(2^{ENOB} \times NR_{out}A_v)$, where $A_v = 3$ is the post-amplifier voltage gain and $NR_{out} = 100\,\text{M}\Omega$, giving a total transimpedance of 300 MΩ. At high OSR, the LSB falls well below the analog noise floor of the readout system, confirming that quantisation noise does not limit the measurement sensitivity in those configurations.

5.4.4 Data Transfer

Depending on the selected acquisition path, the FPGA receives either the decimated output samples derived from the four on-chip ΔΣ bitstreams or the 16-bit digital samples provided by the external ADC. The acquired data are buffered in the FPGA and transferred to the host computer through the USB 3.0 interface of the Opal Kelly XEM7310 module using the FrontPanel SDK. In addition to data acquisition and transfer, the FPGA provides the digital configuration and control signals required by the readout platform, including configuration of the QC01a ASIC and external ADC, as well as control of the external DAC used for sensor-bias generation. This provides a unified digital interface between the readout platform and the host computer.

5.5 Experimental Characterisation

The fabricated and assembled Nanopore Reader was subjected to a systematic experimental characterisation to verify the noise performance, signal bandwidth, dynamic range, and DC-compensation capability of the complete integrated system. All measurements were performed with the QC01a ASIC mounted in its QFN48 package on the Nanopore Reader PCB and operating at the nominal supply volt-

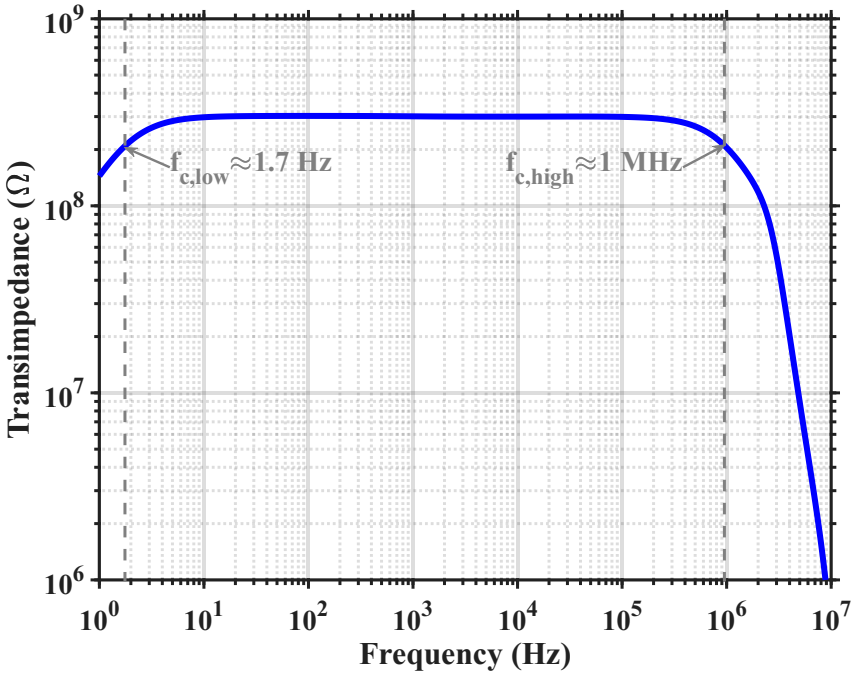


Figure 5.5: Measured frequency response of the QC01a readout AFE.

ages of $V_{DD} = 1.65\,\text{V}$ and $V_{SS} = -1.65\,\text{V}$. Unless otherwise stated, the ASIC input was terminated with a calibrated capacitive load representative of a packaged solid-state nanopore chip, and the on-chip stimulus generator was used to apply the bias conditions described for each test.

5.5.1 Bandwidth

The frequency response of the complete readout front-end was characterised experimentally by applying a small-signal sinusoidal test current to the ASIC input node through a series resistor connected to an external signal generator, such that the generator behaves as a voltage-controlled current source over the entire swept bandwidth. The frequency was swept from 1 mHz to beyond 1 MHz. The output signal was passed through the off-chip AAF and digitised by the off-chip ADC at a sampling rate of 3.3 MSPS. The acquired data were processed to extract the transimpedance magnitude $|Z_{TIA}(f)| = |V_{out}(f)|/I_{in}$ at each frequency step.

The measured frequency response is shown in Fig. 5.5. The front-end exhibits a well-defined bandpass characteristic spanning nearly six decades of signal bandwidth, with a mid-band transimpedance of approximately 300 MΩ maintained from f_m to $f_{-3\text{dB}}$. At low frequencies, the response rolls off with a cutoff around $f_m \approx 1.7\,\text{Hz}$, corresponding to the crossover frequency of the DC-servo loop, as established in Chapter 3. Below this frequency, the DC-servo loop is active and diverts the DC baseline current through feedback, such that very slow AC signals become indistinguishable from DC drift and are attenuated accordingly. This lower cutoff defines the minimum detectable signal frequency of the readout system. At high frequencies, the response rolls off above $f_{-3\text{dB}} \approx 1\,\text{MHz}$, set by the combined response of the TIA

output pole and the off-chip AAF. The measured upper $-3\,\mathrm{dB}$ frequency confirms that the TIA core dominant pole is located well above the DC-servo crossover frequency f_m, validating stable closed-loop operation. Since the DC-servo loop transfer function is designed as an integrator, it contributes a phase lag of $-90°$ at all frequencies. The TIA core, having its dominant pole at approximately 1 MHz, contributes negligible additional phase lag at $f_m \approx 1.7\,\mathrm{Hz}$ — six decades below the TIA pole — resulting in a total loop phase of approximately $-90°$ and therefore a phase margin of $\approx 90°$ at the crossover frequency. The response remains flat over the signal band with no noticeable peaking, confirming stable operation consistent with this analysis.

5.5.2 Linearity

The linearity of the current-processing path was evaluated over different input-current ranges. Figure 5.6(a) shows the measured transfer characteristic for input currents spanning approximately $\pm 1\,\mathrm{nA}$. The measured response exhibits good symmetry between positive and negative input currents and closely follows the expected linear characteristic. To evaluate the linearity at lower current levels, the integral nonlinearity (INL) was extracted over the range of $\pm 100\,\mathrm{pA}$, as shown in Fig. 5.6(b). The maximum deviation remains below approximately 0.45 pA, demonstrating good linearity within the low-current operating range. The AC linearity was further evaluated using a 10 kHz sinusoidal input with an amplitude of 2 nA_{pp}. The corresponding output spectrum is shown in Fig. 5.6(c). The fundamental component is clearly dominant, while higher-order harmonics are strongly suppressed, resulting in a total harmonic distortion (THD) of approximately 0.37%.

5.5.3 Noise

The noise performance of the QC01a readout system was characterised experimentally through systematic measurement of the input-referred current noise. The AC output signal was acquired and divided by the measured transimpedance gain to obtain the equivalent input-referred current noise. The noise power spectral density (PSD) was computed in MATLAB using Welch's method with spectral averaging.

Open-Input Noise Floor

When the input is left open ($I_{in,DC} \approx 0$), no current is injected into the readout system. As discussed in Section 3.3.3, for input currents close to zero the shot-noise term becomes negligible, and the residual noise contributions of subsequent stages become dominant, giving rise to flicker and white noise components. Considering that the equivalent resistance of the PN-junction elements is extremely high for $I_{in,DC} = 0$, and for the implemented design parameters of the ASIC, the low-frequency input-referred noise predicted by the model of Fig. 3.11 can be expressed

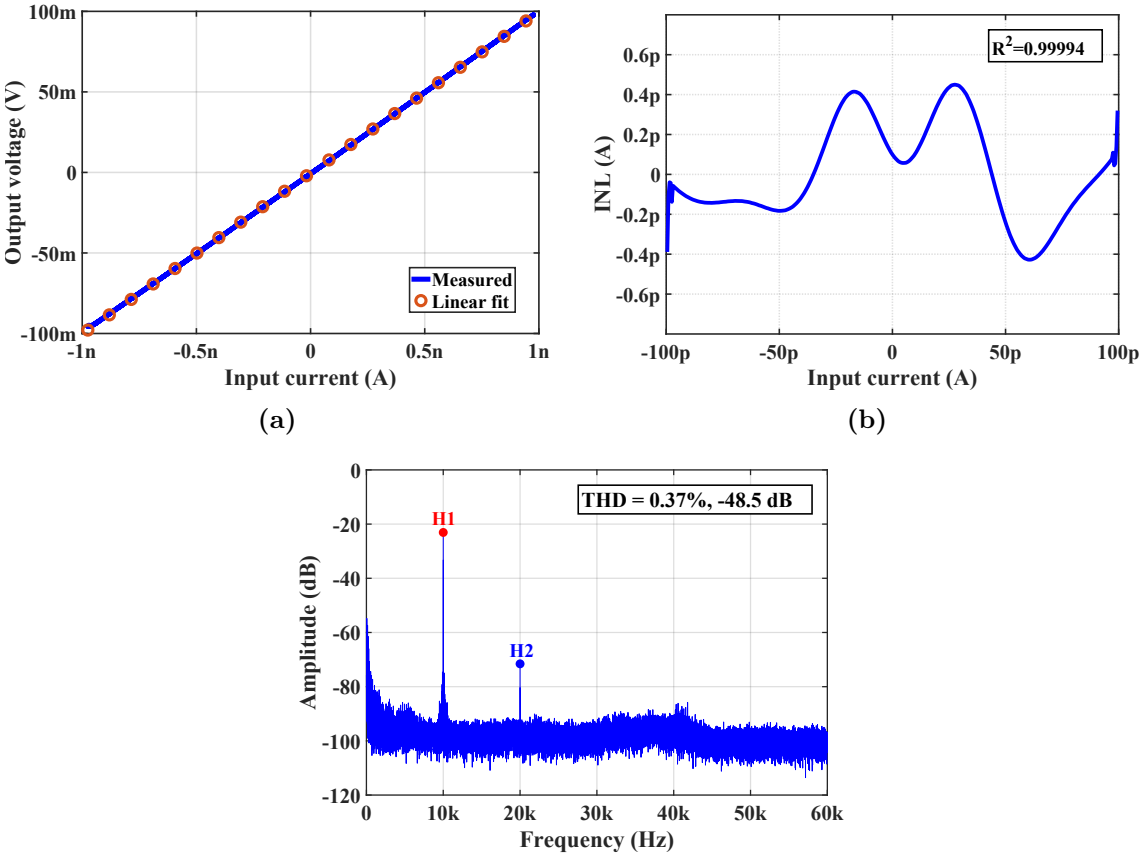


Figure 5.6: Measured linearity of the current-processing path: (a) transfer characteristic over an input-current range of approximately ±1 nA; (b) integral nonlinearity over ±100 pA; and (c) output spectrum for a 10 kHz, 2 nA_{pp} sinusoidal input, showing a THD of approximately 0.37%.

as:

$$\overline{i_{n,in}^2}\big|_{I_{in,dc}\approx 0} \approx \frac{\overline{e_{op2,fl}^2}}{(NR_{out})^2 f} + \left[\frac{\overline{e_{op2,th}^2}}{(NR_{out})^2} + \frac{4kT}{N^2 R_{out}} + \frac{4kT}{M^2 R_2} + \overline{i_q^2}\right] \tag{5.3}$$

where $\overline{i_q^2}$ denotes the input-referred quantisation noise of the AC ΔΣ modulator, given by:

$$\overline{i_q^2} = \frac{V_{FS}^2}{2\, f_{BW}\, (NR_{out}A_v)^2\, 10^{SQNR/10}} \tag{5.4}$$

This expression assumes the residual in-band quantisation noise is approximately white over the signal bandwidth $f_{BW} = 100$ kHz, which is a valid approximation for the sinc^3-filtered output of the second-order ΔΣ modulator at OSR = 50 [44].

In (5.3), the first term is the flicker noise component, which originates from the flicker noise of the output TIA op-amp (OP2), referred to the input. Although the PN-junction configuration at the input node suppresses MOS channel conduction and eliminates flicker noise generation throughout the input circuitry, the input-referred flicker noise of OP2, despite effective attenuation by the transimpedance gain NR_{out}, remains dominant in the low-frequency region as long as the shot-noise contribution

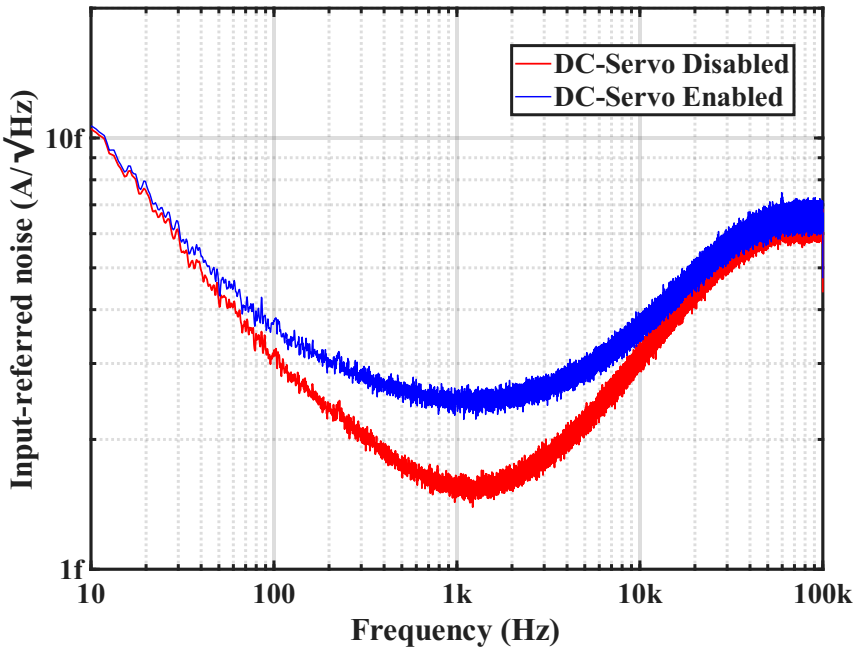


Figure 5.7: Measured input-referred current noise PSD at open input ($I_{in,DC} \approx 0$). Blue curve: DC-servo enabled (R_2 connected); red curve: DC-servo disabled (R_2 disconnected). Both acquired via the on-chip $\Delta\Sigma$ ADC at OSR = 50.

is negligible. The second term represents the total white noise floor, comprising the thermal noise of OP2 and R_{out}, the thermal noise of R_2, and the input-referred quantisation noise of the AC $\Delta\Sigma$ modulator. With $V_{FS} = 1.2\,\mathrm{V}$, $f_{BW} = 100\,\mathrm{kHz}$, $SQNR \approx 79.85\,\mathrm{dB}$, and $NR_{out}A_v = 300\,\mathrm{M\Omega}$, (5.4) evaluates to $\sqrt{\overline{i_q^2}} \approx 0.91\,\mathrm{fA}/\sqrt{\mathrm{Hz}}$. The quantisation noise of the DC $\Delta\Sigma$ modulator is negligible by comparison, since its effective signal bandwidth is limited to the DC-servo crossover frequency $f_m \approx 1.7\,\mathrm{Hz}$, resulting in an extremely high effective OSR and a quantisation floor many orders of magnitude below the analog noise floor.

Fig. 5.7 shows the measured input-referred noise spectra at open input for DC-servo disabled (red) and DC-servo enabled (blue). Both spectra are free of spurious tones, confirming robust circuit implementation and effective shielding against external and supply-induced interference. Both curves exhibit $1/f$ behaviour at low frequencies, consistent with (5.3), and a noise minimum is reached around 1 kHz for both curves. At higher frequencies, the noise density increases due to the conversion of op-amp input voltage noise through the total input capacitance. The blue curve exhibits a steeper high-frequency rise, consistent with the additional input capacitance loading introduced by the DC-servo connection.

For the red curve (DC-servo disabled), R_2 is disconnected from the input node. The white noise floor is therefore determined by the remaining terms in (5.3) — the thermal noise of R_{out} and OP2, together with the AC $\Delta\Sigma$ quantisation noise — yielding a measured minimum noise density of approximately $1.5\,\mathrm{fA}/\sqrt{\mathrm{Hz}}$. For the blue curve (DC-servo enabled), R_2 is connected to the input node, adding its thermal noise contribution of approximately $1.9\,\mathrm{fA}/\sqrt{\mathrm{Hz}}$ in quadrature with the

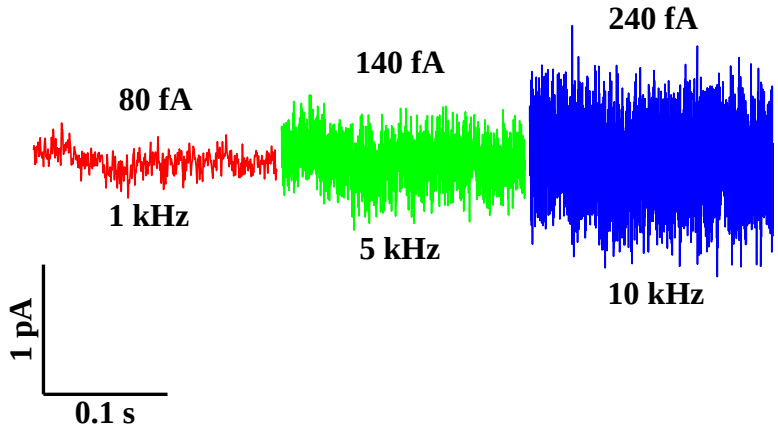


Figure 5.8: Concatenated input-referred current time trace over 200 ms, filtered at 1 kHz (red, 80 fA RMS), 5 kHz (green, 140 fA RMS), and 10 kHz (blue, 240 fA RMS) using a 4th-order Butterworth low-pass filter. Open input, DC-servo disabled, OSR = 50. The scale bar indicates 1 pA vertically and 0.1 s horizontally.

existing floor:

$$\sqrt{\overline{i_{n,white}^2}} = \sqrt{1.5^2 + 1.9^2} \approx 2.4\,\text{fA}/\sqrt{\text{Hz}} \tag{5.5}$$

which is consistent with the measured minimum noise density for the blue curve.

The lower open-input noise floor measured with DC-servo disabled is corroborated by time-domain measurements. The input-referred current trace was recorded over a 200 ms window with DC-servo disabled and filtered using a 4th-order Butterworth low-pass filter at three cutoff frequencies: 1 kHz, 5 kHz, and 10 kHz. The three filtered segments are concatenated and shown in Fig. 5.8. The corresponding integrated RMS noise levels are 80 fA, 140 fA, and 240 fA respectively, confirming sub-pA noise resolution up to 10 kHz and consistency with the integrated noise derived from the PSD.

Effect of DC Baseline Current

To evaluate the noise performance under practical sensing conditions, the input-referred current noise was measured at several representative DC baseline currents, with the DC-handling feedback loop enabled and using the on-chip $\Delta\Sigma$ ADC at OSR = 50.

The measured noise spectra are shown in Fig. 5.9. As the applied DC baseline current increases from 100 pA to 10 nA, the overall noise floor rises progressively above the open-input reference. The minimum noise density in each case is consistent with the expected shot-noise level $\sqrt{2qI_{in,DC}}$, confirming that shot noise dominates the white noise floor at these current levels. Consequently, the low-frequency $1/f$ behaviour becomes less visible with increasing current, indicating a transition toward shot-noise-dominated operation. At higher frequencies, the noise density also increases with the applied DC current, due to the elevated bias in the PN-junction elements, which increases the capacitive noise conversion through the input capaci-

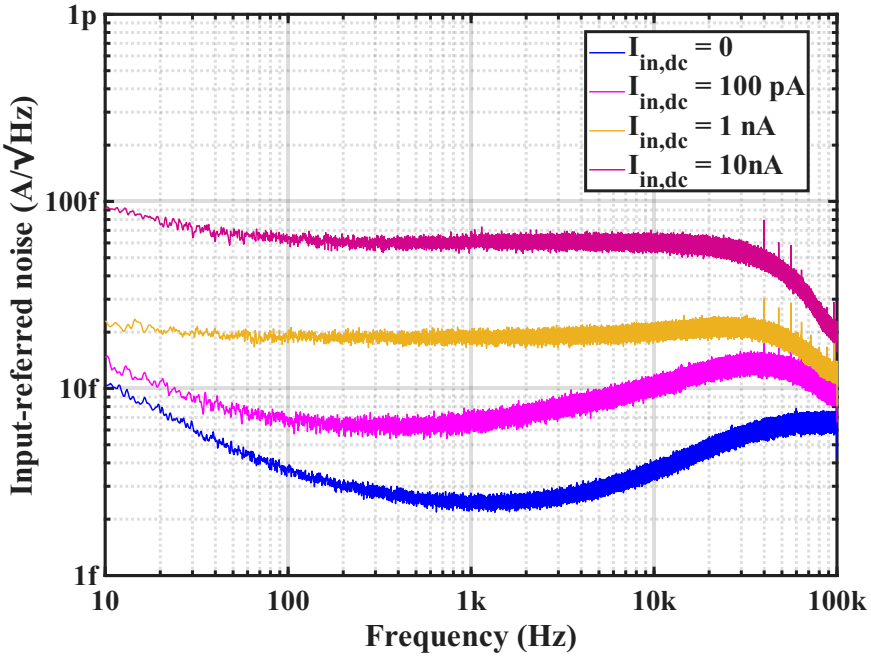


Figure 5.9: Measured input-referred current noise PSD for open input (dashed) and applied DC baseline currents of 100 pA, 1 nA, and 10 nA (solid curves). DC-handling feedback loop enabled in all cases. Acquired via the on-chip ΔΣ ADC at OSR = 50 (f_{SR} = 205 kHz).

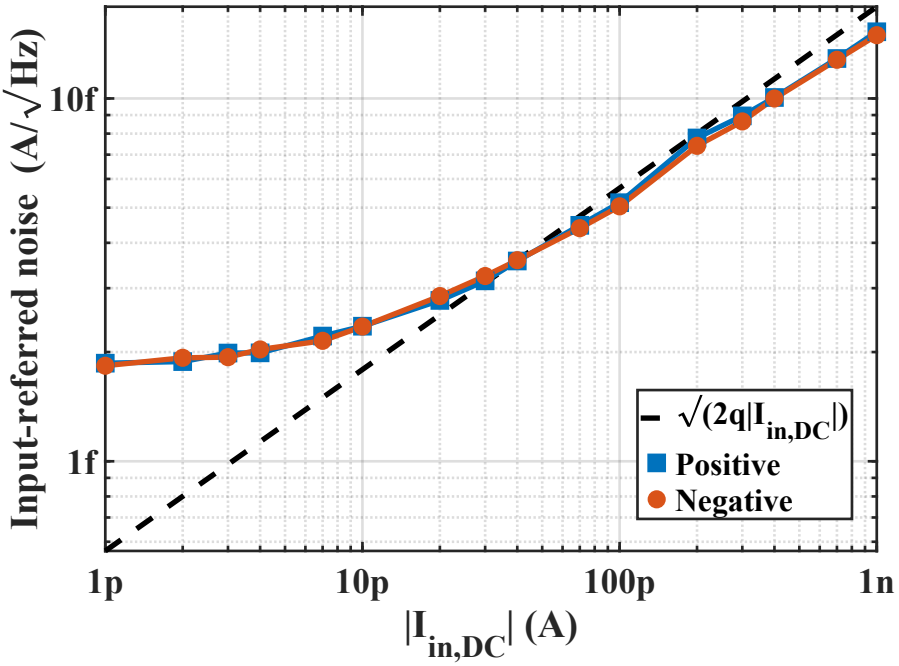


Figure 5.10: Measured input-referred spot noise at 1 kHz as a function of applied DC baseline current magnitude $|I_{in,DC}|$, for positive (blue) and negative (orange) polarities, over a range of ±1 nA. The dashed line shows the theoretical shot noise $\sqrt{2q|I_{in,DC}|}$.

tance.

To further evaluate the noise performance under different input conditions, a con-

Table 5.2: Performance comparison with representative state-of-the-art continuous-time current-readout architectures.

Reference	[29] 2022	[32] 2018	[42] 2017	[43] 2019	[47] 2026	This Work
Technology	0.18-µm SOI CMOS	0.18-µm SOI CMOS	0.35-µm CMOS	0.18-µm CMOS	28-nm CMOS	0.35-µm CMOS
Supply Voltage	1.8 V	1.8 V	3 V	3.3 V	0.9 V	3.3 V
AC Gain[a]	1 GΩ	1 GΩ	220 MΩ	225 MΩ	–	300 MΩ
Bandwidth[a]	80 kHz	8 kHz	10 kHz	–	1 MHz	1 MHz
Noise Floor	1.6 fA/$\sqrt{\text{Hz}}$	5.5 fA/$\sqrt{\text{Hz}}$	1.85 fA/$\sqrt{\text{Hz}}$	3.2 fA/$\sqrt{\text{Hz}}$	29.7 fA/$\sqrt{\text{Hz}}$ @ 0 nA_{DC}	1.5 fA/$\sqrt{\text{Hz}}$[d]
RMS Noise in 5 kHz	–	–	–	0.23 pA_{RMS}	–	0.14 pA_{RMS}
RMS Noise in 10 kHz	–	–	0.3 pA_{RMS}	0.38 pA_{RMS}	–	0.24 pA_{RMS}
THD	–	< 0.1%	–	–	0.22% @ 100 kHz	0.37% @ 10 kHz
Power Consumption	26.6 mW	9.5 mW	7 mW	7 mW	8.4 mW[c]	30 mW
Area	0.42 mm^2	0.07 mm^2	0.6 mm^2	8.82 mm^2[b]	0.13 mm^2[c]	0.45 mm^2

[a] The TIAs presented in [29, 32, 43] are reconfigurable; the listed gain and bandwidth correspond to the configurations yielding the minimum reported input-referred noise.
[b] [43] presents a multi-clamp system incorporating both voltage- and current-clamp functionalities together with compensation circuitry.
[c] The implementation in [47] additionally employs an off-chip digital differentiator, reported to consume 0.12 mW and occupy 0.003 mm^2.
[d] The minimum noise density of 1.5 fA/$\sqrt{\text{Hz}}$ is measured with the DC-servo path disconnected. With the DC-servo enabled, the measured minimum noise density is approximately 2.4 fA/$\sqrt{\text{Hz}}$.

trolled DC current in the range of ±1 nA was injected at the input. For each operating point, the input-referred spot noise at 1 kHz was measured and plotted in Fig. 5.10 as a function of the injected DC current magnitude. The close agreement between positive and negative polarities further validates the symmetry of the complementary anti-parallel PN-junction configuration described in Chapter 3. For currents below 10 pA, the noise floor is approximately constant at 1.9 fA/$\sqrt{\text{Hz}}$, consistent with the R_2-dominated open-input floor established in Section 5.5.3. As the current increases beyond this threshold, the measured noise follows the expected shot-noise dependence $\sqrt{2q|I_{in,DC}|}$, remaining in close agreement with the theoretical limit and confirming shot-noise-dominated operation.

5.5.4 Performance Comparison

Table 5.2 compares the measured performance of the proposed readout with representative continuous-time low-current sensing interfaces reported in the literature. The comparison highlights the combination of fA/$\sqrt{\text{Hz}}$-level input-referred noise and approximately 1 MHz signal bandwidth achieved by the proposed architecture. The recent wideband design of [47] similarly reaches a 1 MHz bandwidth, but with a substantially higher minimum spot-noise density. The present architecture therefore maintains very low input-referred noise while extending the usable bandwidth into the MHz range.

5.6 Summary

This chapter has described the system-level integration of the QC01a ASIC and presented its complete experimental characterisation.

The fabricated ASIC was packaged in a QFN48 surface-mount package and mounted on a dedicated PCB readout platform integrating all hardware required for full system operation: regulated power supply rails, bias voltage generation, off-chip anti-aliasing filtering, and an FPGA digital back-end implementing the sinc^3 decimation filter, operating mode control, and USB data transfer to the host computer.

Experimental characterisation of the complete system confirmed agreement with the theoretical predictions of Chapter 3 across all key performance metrics. The measured frequency response exhibits a well-defined bandpass characteristic spanning nearly six decades of signal bandwidth, with a mid-band transimpedance of approximately 300 MΩ between the DC-servo crossover frequency $f_m \approx 1.7$ Hz and the upper -3 dB cutoff $f_{-3\text{dB}} \approx 1$ MHz. The phase margin at the DC-servo crossover is approximately 90°, confirming stable closed-loop operation.

Noise characterisation at open input yields a minimum input-referred noise density of $1.5\,\text{fA}/\sqrt{\text{Hz}}$ with DC-servo disabled, rising to $2.4\,\text{fA}/\sqrt{\text{Hz}}$ with DC-servo enabled due to the added thermal noise of R_2. Integrated RMS noise levels of 80 fA, 140 fA, and 240 fA at 1 kHz, 5 kHz, and 10 kHz bandwidths confirm sub-pA resolution across the biologically relevant measurement bandwidth. Under applied DC baseline currents, the noise floor rises in close agreement with the theoretical shot-noise limit $\sqrt{2q|I_{in,DC}|}$, validating the DC-compensation architecture and confirming shot-noise-dominated operation for both positive and negative input polarities. The experimental results validate the complete sensing platform and provide the characterised system that underpins the nanopore sensing experiments presented in Chapter 6.

Chapter 6

Experimental Validation with Nanopore Recordings

This chapter presents the experimental validation of the complete QC01a-based readout platform through ionic current recordings with solid-state nanopores. The objective is to demonstrate that the ultra-low-noise current readout system developed in the preceding chapters is capable of operating under practical nanopore sensing conditions—interfacing directly with a nanopore device, handling an nA-level DC baseline through the integrated DC-compensation loop, and resolving nA-scale transient blockade events corresponding to the translocation of individual DNA molecules. The chapter describes the experimental configuration, the nanopore sensing platform, the measurement protocol, and the recorded translocation data.

6.1 Nanopore Sensing Platform

Fig. 6.1 presents a simplified block diagram of the nanopore readout system used for the experimental validation. A DNA molecule translocating through the solid-state nanopore produces a transient modulation of the ionic current I_{in}, carried by electrophoretically driven charge carriers through the pore aperture. This current is presented directly to the front-end of the QC01a ASIC, where the DC baseline component is handled by the integrated DC-servo loop while the transient AC component is processed by the wideband signal path.

For the nanopore recordings presented in this chapter, the analog AC output of the ASIC is digitised through the external ADC path of the Nanopore Reader, allowing wideband acquisition of the translocation signals. The digitised data are transferred to the FPGA digital back-end and subsequently to the host computer through the USB interface for acquisition and analysis. The nanopore bias voltage is applied through the programmable bias-generation circuitry of the readout platform. The diagram is intentionally simplified, and intermediate signal-conditioning and control circuitry is omitted for clarity.

The nanopore sensing platform assembled for the validation experiments in this

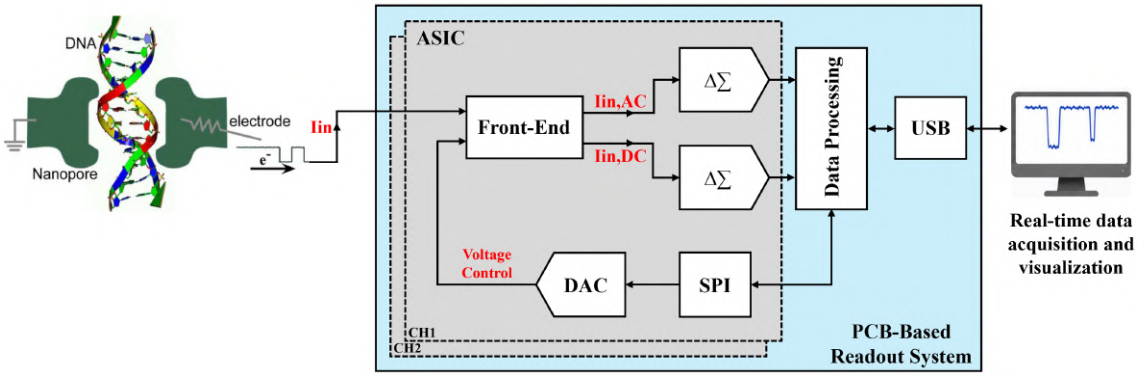


Figure 6.1: Simplified block diagram of the QC01a-based nanopore readout system used for the experimental validation. The ionic current I_{in} produced by DNA translocation events through the solid-state nanopore is processed by the QC01a front-end, where the DC baseline is compensated by the integrated DC-servo loop and the transient AC component is available at the wideband analog output. For the measurements reported in this chapter, the analog signal is digitised through the external ADC path and transferred to the host computer through the FPGA and USB interface. Intermediate conditioning and control circuitry is omitted for clarity.

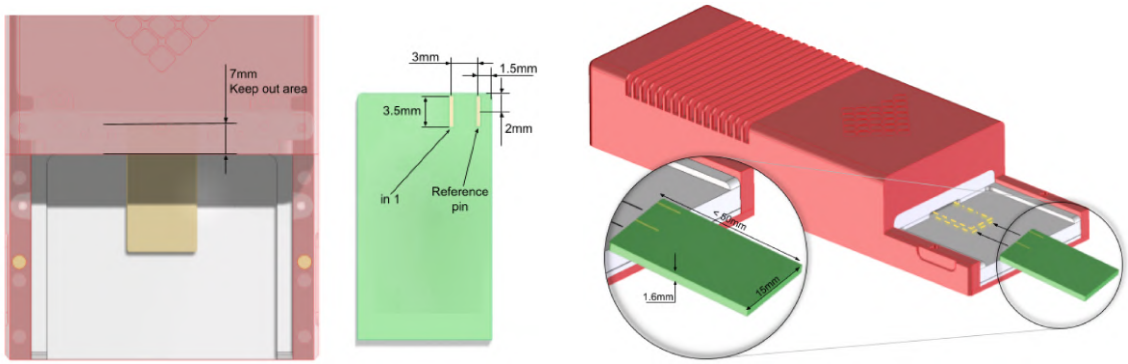
chapter consists of three components: an interface printed circuit board (PCB) that forms the electrical and mechanical base; a microfluidic flow cell that houses the nanopore chip and provides a controlled electrolyte environment; and a solid-state nanopore chip that constitutes the sensing element. Together, these components form a self-contained cartridge that inserts directly into the QC01a Nanopore Reader. The following subsections describe each component in turn, followed by a description of the complete integrated platform.

6.1.1 Interface PCB

The interface PCB serves as the electrical and mechanical base of the sensing platform. Its primary function is to route the signals from the Ag/AgCl electrodes of the fluidic cell to the input contact pads of the QC01a Nanopore Reader with minimum parasitic loading. The PCB adopts a compact card-edge form factor of 15 mm × 1.6 mm, designed for direct insertion into the reader's front-panel slot via spring-contact pads.

As illustrated in Fig. 6.2(a), two gold contact pads are placed at the card edge: the signal input pad (`In 1`, 3 mm × 3.5 mm) and the reference electrode contact (1.5 mm × 2 mm). A 7 mm keep-out zone is maintained above the contact region to accommodate the fluidic cell body without mechanical interference. Fig. 6.2(b) shows the PCB being inserted into the reader enclosure, where mechanical guides enforce repeatable alignment and stable electrical contact, with a total routing length of less than 50 mm from the electrode contact points to the reader input.

Minimising the routing length at the high-impedance input node is an important design requirement. As established in Chapter 2, parasitic capacitance added at the



(a) (b)

Figure 6.2: Interface PCB design. (a) Top-view schematic of the card-edge contact pad layout, showing the signal input pad (`In 1`, 3 mm × 3.5 mm), the reference electrode contact (1.5 mm × 2 mm), and the 7 mm keep-out zone reserved for the fluidic cell body. (b) CAD render of the interface PCB (15 mm × 1.6 mm) sliding into the Nanopore Reader slot, illustrating the mechanical guide alignment and the sub-50 mm routing length from electrode contacts to reader input.

TIA input increases the high-frequency input-referred current noise of the front-end. The short, direct routing topology of the interface PCB therefore helps minimise the additional parasitic capacitance introduced between the nanopore device and the ASIC input. Since the measurements in this chapter employ a single nanopore device, only Core 1 (`In 1`) is used for current recording.

6.1.2 Nanopore Flow Cell

The microfluidic flow cell used in this work was developed by Elements Srl (Cesena, Italy) and serves as the interface between the solid-state nanopore chip and the current readout system. The flow cell defines the two electrolyte reservoirs on either side of the nanopore membrane, establishes the electrochemical interface through which the ionic current flows, and provides the mechanical housing for the nanopore chip.

The architecture of the flow cell is shown in the exploded view of Fig. 6.3(a). The nanopore chip occupies the central position in the assembly stack, sandwiched between two PMMA fluidic bodies that define the *cis* and *trans* electrolyte chambers. Silicone gaskets on both faces of the chip provide a hermetic seal around the membrane perimeter, preventing electrolyte exchange between the two chambers except through the nanopore itself. Fluidic access ports machined into the PMMA bodies allow electrolyte filling, rinsing, and analyte introduction into each chamber independently.

Electrical contact with the electrolyte in each chamber is established via Ag/AgCl electrodes, fabricated from silver wires electrochemically chloridised to form a stable AgCl surface layer. Ag/AgCl electrodes are the standard choice for nanopore measurements owing to their stable and well-defined electrode potential, which min-

imises DC offset voltages and suppresses low-frequency electrochemical noise in the ionic current signal [18]. The electrodes are inserted through the PMMA chambers and secured by a stainless-steel ring clamped onto the top of the assembly, ensuring a reproducible immersion geometry across experiments. The base of the assembly mounts directly onto the interface PCB, with the electrode contacts aligning to the PCB signal and reference pads.

Figs. 6.3(b)–(d) show the fabricated hardware at successive stages of assembly. Fig. 6.3(b) shows the bare interface PCB with the two Ag electrode receptacles and the four mounting holes visible. Fig. 6.3(c) shows the PCB with the PMMA flow cell body and nanopore chip mounted and the Ag electrodes inserted into the fluidic chambers, with the fluidic channel network visible through the transparent PMMA. Finally, Fig. 6.3(d) shows the fully assembled flow cell with the clamping ring secured on top, constituting the complete sensing cartridge ready for insertion into the Nanopore Reader.

6.1.3 Solid-State Nanopore Chip

Solid-state nanopores were employed as the sensing element in the validation experiments. A solid-state nanopore is a nanometre-scale aperture through a thin inorganic membrane—typically silicon nitride (SiN_x) or silicon dioxide (SiO_2)—fabricated by focused-ion beam (FIB) milling, transmission electron microscopy (TEM)-controlled drilling, or controlled dielectric breakdown [10]. Relative to protein nanopores reconstituted in lipid bilayers, solid-state devices offer greater mechanical and chemical robustness, compatibility with a wide range of analytes and ionic conditions, and straightforward co-integration with semiconductor readout electronics.

The nanopore chips used in this work were commercially sourced from Norcada Inc. (Edmonton, Canada). Each chip consists of a free-standing SiN_x membrane of 25 nm nominal thickness, supported on a silicon frame. Nanopores with a nominal diameter of 10 nm were used for all translocation experiments reported in this chapter. Prior to assembly, chips were cleaned using standard solvent and piranha protocols and conditioned under the measurement electrolyte to ensure stable and reproducible open-pore conductance before analyte introduction.

6.1.4 Integration with the QC01a Readout Platform

The complete sensing cartridge—comprising the interface PCB, flow cell, and nanopore chip—is integrated with the QC01a Nanopore Reader by inserting it through the front-panel slot of the reader enclosure, as shown in Fig. 6.4. The card-edge contact pads of the PCB engage with the spring-loaded contacts inside the reader slot, establishing simultaneous mechanical registration and electrical connection in a single insertion step. This modular architecture supports rapid cartridge exchange and provides a reproducible, low-parasitic electrical interface between the nanopore sensor and the readout ASIC.

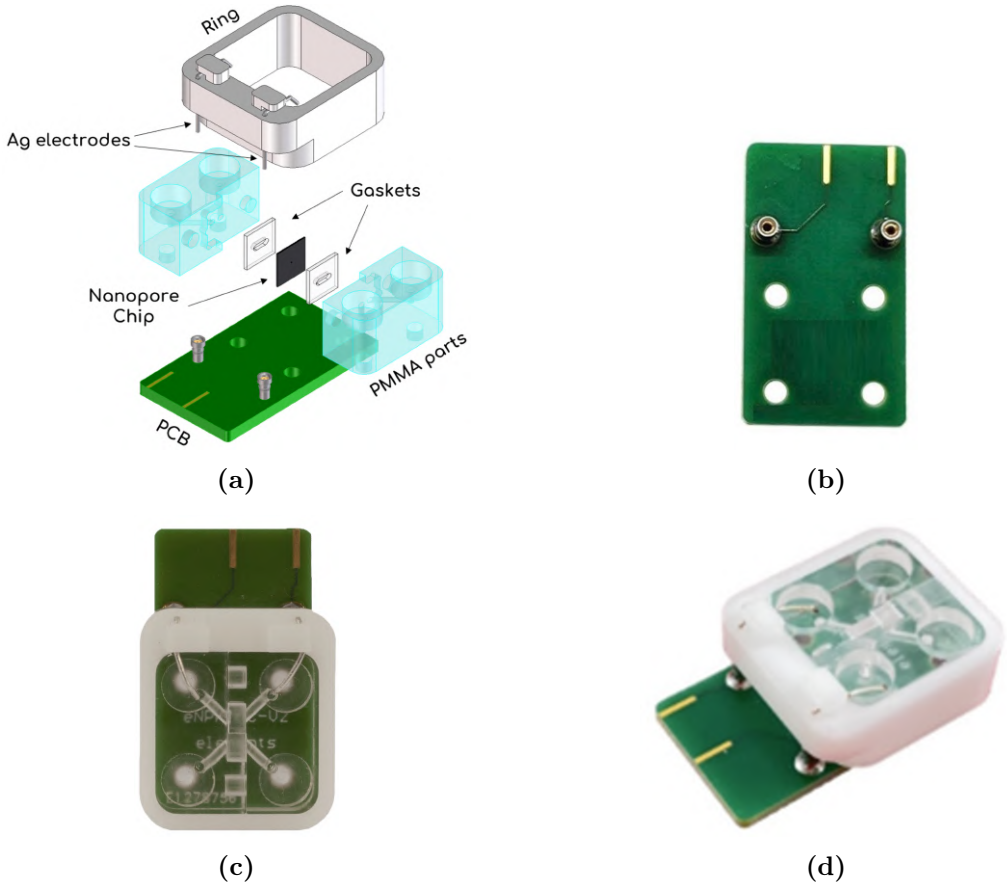


Figure 6.3: Nanopore flow cell assembly (Elements Srl, Cesena, Italy). (a) Exploded view of the complete stack from bottom to top: interface PCB, lower PMMA fluidic body (*trans* chamber), silicone gasket, nanopore chip, silicone gasket, upper PMMA fluidic body (*cis* chamber), Ag/AgCl electrodes, and stainless-steel clamping ring. (b) Bare interface PCB showing the Ag electrode receptacles and card-edge contact pads. (c) Intermediate assembly with the PMMA flow cell and nanopore chip mounted on the PCB and Ag electrodes inserted; the fluidic channel network is visible through the transparent PMMA. (d) Fully assembled sensing cartridge with the clamping ring secured, ready for insertion into the Nanopore Reader.

6.2 Measurement Protocol

Prior to the translocation experiments, the flow cell was filled with a 1 M KCl aqueous electrolyte solution. This concentration is commonly employed in solid-state nanopore measurements because it provides high ionic conductance and a well-characterised electrochemical environment [10, 18]. The 10 nm diameter, 25 nm thick SiN_x nanopore described in Section 6.1.3 was biased at 300 mV throughout the experiments.

Lambda (λ)-DNA was selected as the analyte for the translocation validation. Lambda DNA is a linear, double-stranded DNA molecule of 48,502 base pairs, with a contour length of approximately 16.5 µm. It is widely employed as a standard analyte in solid-state nanopore experiments due to its well-defined length, charge density,

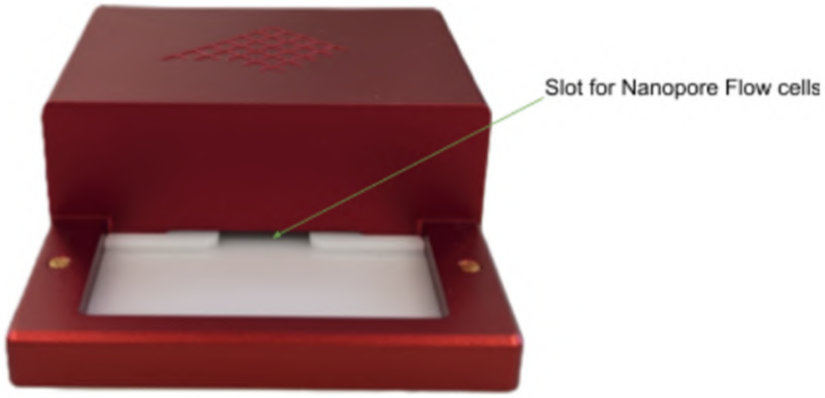


Figure 6.4: Photograph of the QC01a Nanopore Reader with the lid open, showing the front-panel slot into which the assembled sensing cartridge is inserted. The spring-loaded card-edge contacts inside the slot establish simultaneous mechanical and electrical connection upon insertion.

and translocation characteristics [10, 48]. Lambda DNA was introduced into the *cis* chamber (the chamber connected to the negatively biased electrode) at a concentration of approximately 1 nM. Under the applied bias, the negatively charged DNA molecules are electrophoretically driven through the nanopore toward the *trans* chamber, producing transient blockades in the open-pore ionic current.

The DC baseline current arising from the unobstructed ionic flow through the nanopore under the applied bias was accommodated by the DC-handling feedback loop of the QC01a AFE. The DC-servo loop continuously diverts the baseline component away from the TIA core signal path, maintaining the AC output within its linear operating range and preserving the available output swing for the detection of transient blockade signals. This continuous DC-compensation mechanism operates without periodic reset or interruption of the measurement.

Signals were acquired at a sampling rate of 1.6 MS/s using the wideband analog output and the external ADC path of the Nanopore Reader. The TIA core was configured for an approximately 1 MHz analog bandwidth. The recorded data were subsequently post-processed using a fourth-order Butterworth low-pass filter with a cutoff frequency of 50 kHz, suppressing out-of-band noise while retaining the temporal information of the observed translocation events.

6.3 Experimental Results

6.3.1 Ionic Current Recording and Baseline Stability

The nanopore measurements reported in this section were conducted at the Keyser Lab, Cavendish Laboratory, University of Cambridge, UK. Prior to the translocation experiments, the open-pore ionic current was measured to characterise the nanopore conductance and verify the experimental conditions. The conductance of

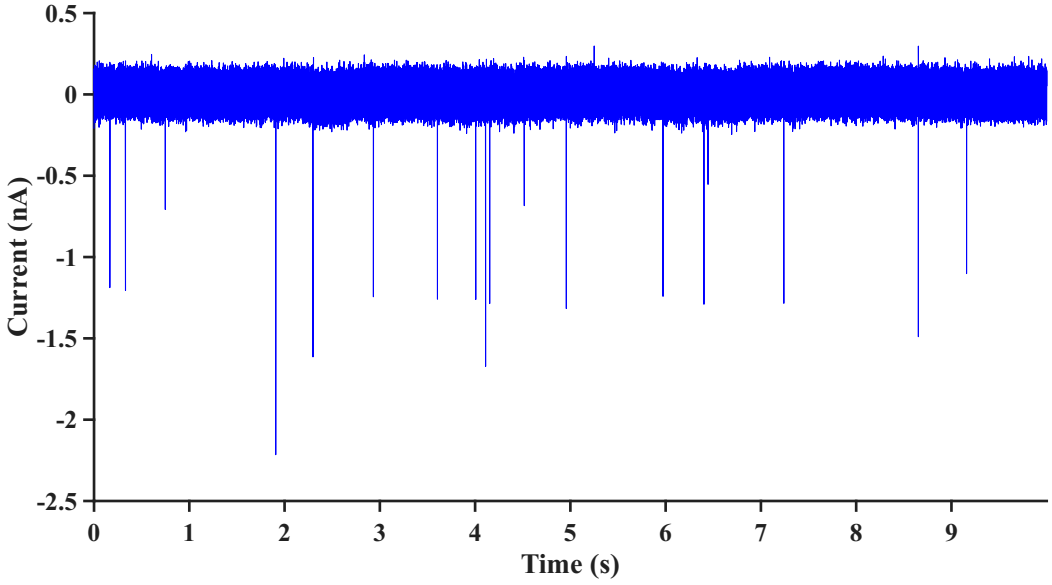


Figure 6.5: AC-channel ionic current recording from a solid-state SiN_x nanopore (10 nm nominal diameter, 25 nm membrane thickness, 1 M KCl, 300 mV bias) acquired over a 10 s interval. The open-pore DC baseline is compensated by the integrated DC-handling feedback loop of the QC01a AFE. Multiple downward current blockades corresponding to individual λ-DNA translocation events are resolved above the noise floor.

a cylindrical nanopore can be expressed as [10]:

$$G = s\left(\frac{4L}{\pi d^2} + \frac{1}{d}\right)^{-1} \tag{6.1}$$

where s is the solution conductivity, L is the effective membrane thickness, and d is the pore diameter. For the measurement conditions employed ($d = 10\,\text{nm}$, $L = 25\,\text{nm}$, $s = 11.6\,\text{S/m}$ for 1 M KCl at room temperature), Equation (6.1) yields an expected open-pore conductance of $G_{\text{exp}} = 27.7\,\text{nS}$, corresponding to an expected baseline current of $I_0 = G_{\text{exp}} \cdot V_{\text{bias}} = 8.3\,\text{nA}$ at 300 mV.

The measured open-pore baseline current prior to analyte introduction was $I_0 = 10.1\,\text{nA}$, corresponding to a measured conductance of $G_{\text{meas}} = I_0/V_{\text{bias}} = 33.7\,\text{nS}$. Inverting Equation (6.1) to back-calculate the effective pore diameter from G_{meas} yields $d_{\text{eff}} = 11.2\,\text{nm}$, in good agreement with the nominal fabricated diameter of 10 nm. The observed difference is consistent with variations in the effective pore geometry that can arise during nanopore conditioning and wetting [10]. The measured baseline current of 10.1 nA is well within the DC-handling range of the QC01a AFE, confirming that the integrated compensation loop can accommodate the open-pore baseline without driving the AC signal path into saturation.

Figure 6.5 shows the AC-channel current trace recorded over a 10 s interval following λ-DNA introduction. The open-pore DC baseline is continuously compensated by the DC-servo loop, while the AC-channel output remains centred around its nominal operating level with a stable, low-noise baseline. Multiple downward current blockades are clearly visible and are consistent with individual λ-DNA translocation

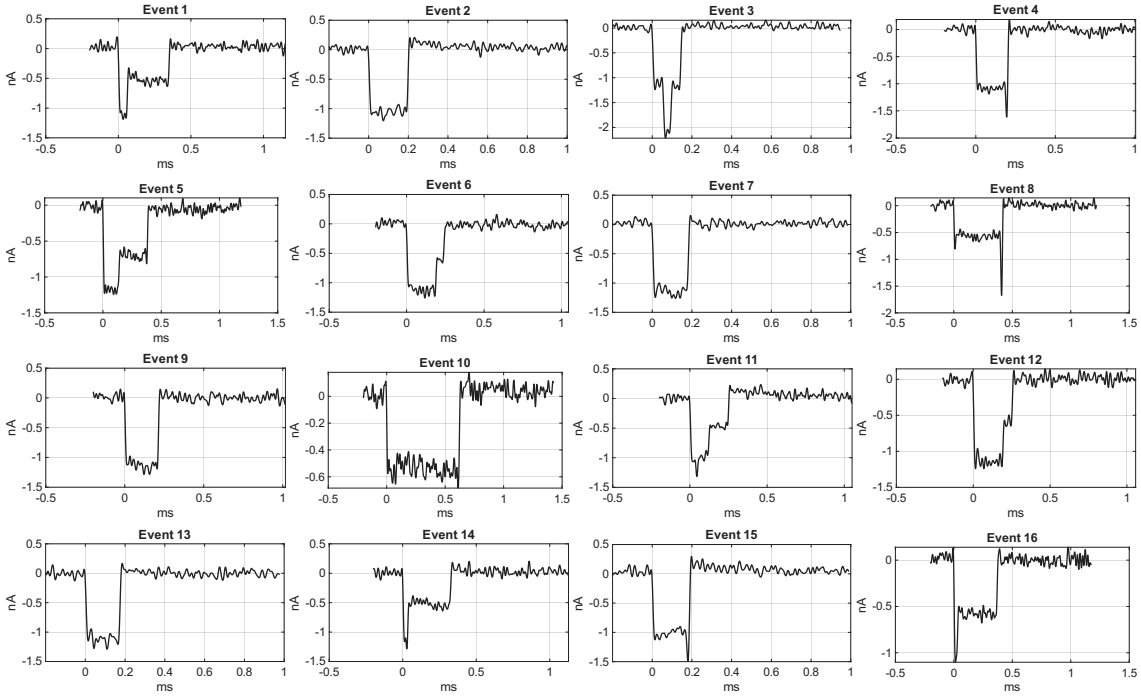


Figure 6.6: Individual λ-DNA translocation events extracted from the ionic current trace by threshold-based event detection. Each panel shows a single event on a common $\sim$1 ms time axis, illustrating the blockade amplitude, entry and exit transitions, and low-noise baseline. Events are indexed in order of appearance in the recording.

events through the nanopore. No reset artefacts or saturation events are observed within the displayed measurement interval, demonstrating continuous-time operation of the readout architecture under the tested nanopore conditions.

6.3.2 DNA Translocation Events

Individual translocation events were extracted from the AC-channel trace by applying a threshold-based event detection algorithm, using a detection threshold set at five standard deviations below the open-pore baseline. A representative selection of detected events is shown in Fig. 6.6, each plotted on a common time axis spanning approximately 1 ms.

The events exhibit the characteristic morphology of nanopore translocations: an abrupt downward transition from the open-pore level at event entry, a reduced-current interval during molecular passage through the pore, and a return toward the baseline at event exit. The 50 kHz post-processing bandwidth provides sufficient temporal resolution to resolve the sub-millisecond structures observed in the recorded events.

The blockade conductance $\Delta G = \Delta I / V_{\text{bias}}$ provides a useful normalisation of the blockade amplitude. For double-stranded DNA (dsDNA) of diameter $d_{\text{DNA}} = 2.2\,\text{nm}$ translocating in single file through the nanopore, the expected blockade conductance can be approximated as [10]:

$$\Delta G = \frac{s\pi d_{\mathrm{DNA}}^2}{4L} \tag{6.2}$$

which evaluates to $\Delta G_{\mathrm{exp}} = 4.6\,\mathrm{nS}$ for the present geometry, corresponding to an expected blockade current of $\Delta I_{\mathrm{exp}} = \Delta G_{\mathrm{exp}} \cdot V_{\mathrm{bias}} \approx 1.4\,\mathrm{nA}$ at 300 mV. The observed blockade amplitudes in Fig. 6.6 are of the same order of magnitude, consistent with the expected nA-scale current modulation associated with λ-DNA translocation through the nanopore.

The dwell times of the observed events extend from tens of microseconds to approximately one millisecond, consistent with the sub-millisecond timescales commonly observed for λ-DNA translocation through solid-state nanopores under comparable experimental conditions [10, 48]. The representative events shown here are used primarily to demonstrate the capability of the QC01a platform to resolve individual translocation signals. A comprehensive statistical analysis of the full event population, including the distributions of blockade amplitude ΔI and dwell time τ_d, lies beyond the scope of the present proof-of-concept validation and represents a direction for future experimental work.

6.4 Summary

This chapter has demonstrated the experimental validation of the QC01a-based readout platform in a complete solid-state nanopore sensing experiment. A nominal 10 nm SiN_x nanopore in 1 M KCl was interfaced with the Nanopore Reader through a dedicated microfluidic flow cell and low-parasitic interface PCB. Under a 300 mV bias, a stable open-pore current of approximately 10.1 nA was measured, while the integrated DC-handling feedback loop continuously compensated the baseline current without requiring periodic reset. Individual λ-DNA translocation events were resolved as nA-scale transient current blockades with sub-millisecond temporal structure, demonstrating single-molecule detection with the complete QC01a-based platform.

The measurements presented in this chapter constitute a proof-of-concept validation under a representative solid-state nanopore operating condition. The present experimental study was performed using a single SiN_x nanopore geometry, a fixed bias voltage, and a selected acquisition configuration. Further experimental assessment across different nanopore geometries, bias voltages, acquisition bandwidths, and sampling conditions would provide a broader evaluation of the robustness and performance of the readout platform. A direct side-by-side nanopore measurement with a commercial or previously reported current amplifier was not performed in the present study; however, the electrical performance of the proposed readout architecture is quantitatively benchmarked against representative state-of-the-art current-readout interfaces in Table 5.2.

Taken together, the results demonstrate that the proposed current readout system satisfies the principal requirements established in Chapter 1 under the tested

nanopore condition: low-noise detection of small current variations, accommodation of an nA-scale DC baseline, continuous reset-free operation, and successful integration with a solid-state nanopore sensor for single-molecule recording.

Conclusions and Outlook

Summary of Contributions

This dissertation has presented the design, implementation, and experimental validation of a novel ultra-low-noise CMOS current readout system for nanopore-based single-molecule sensing. The core contributions are as follows.

PN-junction TIA topology. A continuous-time transimpedance amplifier was proposed in which the intrinsic drain–bulk PN junction of a standard CMOS MOSFET serves as the feedback element, with the transistor gate statically biased to fully suppress channel conduction. This operating condition eliminates both flicker noise and channel thermal noise from the feedback path; the dominant residual noise is shot noise arising from junction transport, which at pA-level currents is equivalent to the thermal noise of a GΩ–TΩ passive resistor. Monte Carlo analysis demonstrated a coefficient of variation in the feedback impedance more than 340 times smaller than that of a comparable subthreshold pseudo-resistor, confirming superior robustness to process and mismatch variations.

TIA core architecture. The basic PN-junction feedback stage was extended to form the TIA core, incorporating complementary anti-parallel junction pairs for bipolar operation, a ratiometric current amplifier for linearization, and pole-zero compensation for bandwidth control. The resulting transimpedance gain $R_{TIA} = N \cdot R_{out}$ and the $-3\,\mathrm{dB}$ bandwidth $f_{-3\mathrm{dB}} = 1/(2\pi R_{out} C_{out})$ are set by well-controlled design parameters, independent of sensor capacitance variations.

DC-compensated TIA. The TIA core was augmented with a DC-servo loop employing an active integrator and a PN-junction-based transconductor to continuously divert the large DC baseline current inherent to nanopore sensing, preserving the full output swing for AC signal excursions. The architecture achieves pA-level noise resolution while accommodating nA-level DC baselines, with a simple and stable servo loop benefiting from the favorable phase characteristics of the R-TIA core.

CMOS ASIC and PCB platform. Both architectures were implemented as a monolithic ASIC and integrated into a PCB-based readout platform. Experimental characterization confirmed agreement with theoretical predictions for noise, bandwidth, and dynamic range. Nanopore sensing experiments demonstrated single-molecule translocation detection under biologically relevant conditions.

Future Directions

Multichannel scaling and array integration. The dual-channel QC01a prototype demonstrates that two independent readout cores can be integrated monolithically with negligible inter-channel crosstalk. A natural next step is to scale this architecture to a higher channel count—tens to hundreds of parallel readout cores—to support high-throughput nanopore arrays for DNA sequencing and proteomics applications. Key challenges include power density management, routing of high-impedance input nodes in a dense layout, and design of a scalable digital back-end for aggregating parallel data streams at high aggregate bandwidth.

Co-integration with solid-state nanopore fabrication. The interface PCB approach employed in this work introduces physical separation between the nanopore chip and the readout ASIC, limiting input-referred noise at high frequencies due to parasitic capacitance at the interconnect. Monolithic or near-monolithic co-integration of the readout front-end with the nanopore membrane—for example through back-end-of-line (BEOL) deposition of SiN_x membranes directly on the CMOS die, or through 3D stacking—would eliminate this parasitic loading, potentially reducing the high-frequency integrated noise by an order of magnitude and enabling bandwidths beyond 1 MHz without compromising the noise floor.

Further noise reduction through circuit techniques. While the PN-junction feedback element eliminates flicker noise from the feedback path, the residual low-frequency noise floor of the implemented TIA is still limited by the input-referred flicker noise of the OTA. Chopper stabilisation of the OTA, or correlated double sampling applied to the digitised output, are established techniques for suppressing $1/f$ noise that could extend the low-noise band below 10 Hz, enabling detection of slow conformational changes and long-dwell translocation events.

Real-time digital event detection. The current platform offloads all event detection and analysis to the host computer in post-processing. Implementing a real-time event detection and classification engine directly on the FPGA—using threshold-based detection, matched filtering, or lightweight machine learning inference—would enable on-the-fly event extraction, dramatically reducing the data volume transferred to the host and opening the path to closed-loop feedback control of the translocation process, for example through dynamic bias adjustment to modulate translocation speed.

Extension to protein nanopores and single-molecule protein sensing. The experiments in this dissertation employed solid-state SiN_x nanopores with λ-DNA as a well-characterised model analyte. Extending the platform to protein nanopores reconstituted in supported lipid bilayers would enable single-molecule protein sequencing and study of protein–ligand interactions at the single-molecule level. The DC-compensated architecture is well suited to this application, as protein nanopores typically exhibit open-pore currents in the tens to hundreds of pA range, where the full noise advantage of the PN-junction feedback element is most pronounced.

Process optimisation and technology scaling. The current ASIC is implemented in a 0.35 µm process, which offers well-characterised high-voltage devices but

is not optimised for the lowest possible $1/f$ noise. Migration to a more advanced CMOS node with lower intrinsic OTA flicker noise, or to a specialised low-noise BiCMOS process, could yield further reductions in the low-frequency noise floor. The ratiometric linearisation architecture scales naturally with technology, and its area efficiency would improve substantially in a finer geometry node.

Appendix

This appendix provides the complete pin assignment and package mechanical data for the QC01a ASIC. The device is housed in a 48-lead Quad Flat No-lead (QFN48) package with a 6 mm × 6 mm body and 0.40 mm pin pitch, designated QP-QFN48-6MM-0.40MM (QPTechnologies, part number 500391, conforming to JEDEC MO-220).

Pin Diagram

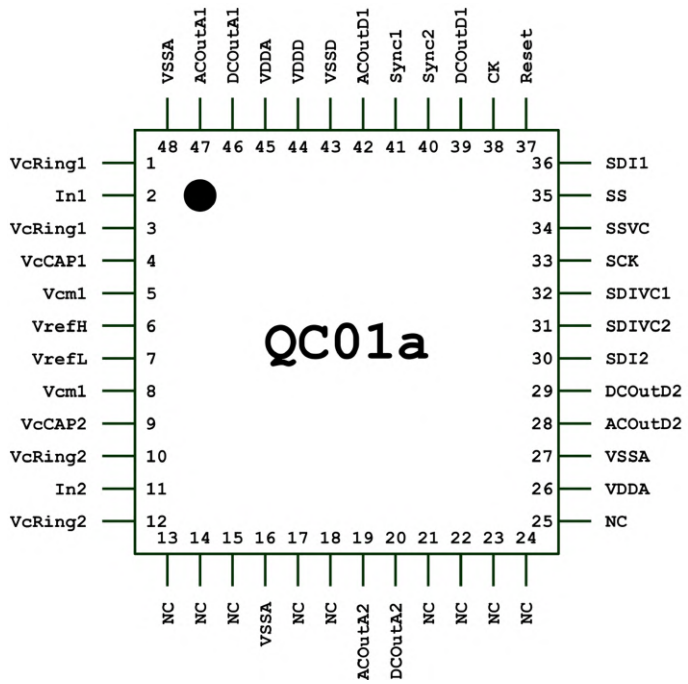


Figure 6.7: QC01a QFN48 pin diagram. Pin 1 is at the top-left corner (chamfer indicator shown).

Package Mechanical Drawing

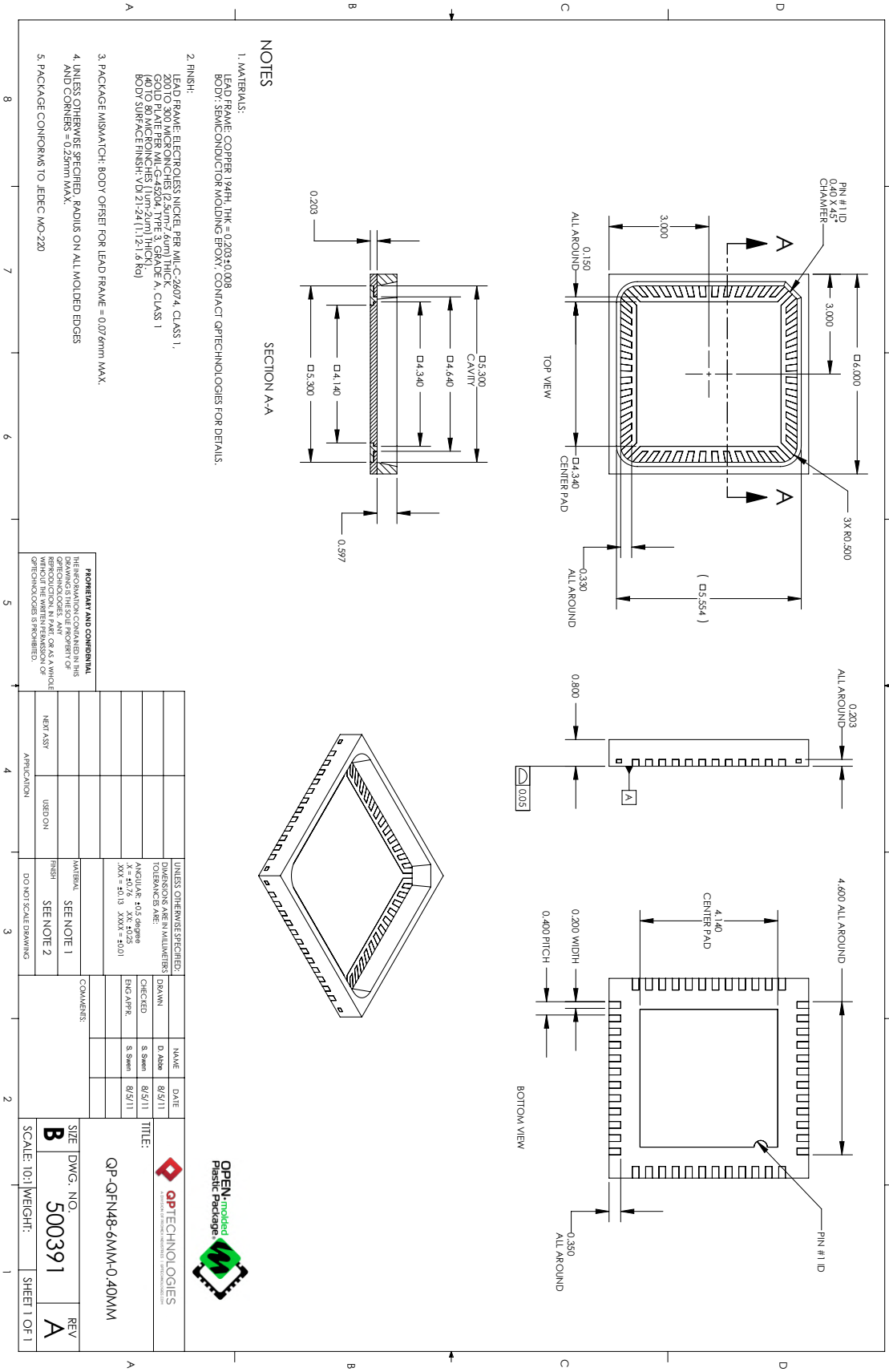


Figure 6.8: Mechanical drawing of the QP-QFN48-6MM-0.40MM package (QPTechnologies, drawing no. 500391, rev. A). Dimensions in millimetres.

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