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MODELING OF FINFET DEVICES AT CRYOGENIC TEMPERATURES

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Abstract

Cryogenic operation of advanced CMOS is fundamental for scalable quantum computing interfaces and cryogenic RF electronics, yet prevailing device models inadequately capture transistor behaviour far below ambient temperature. This thesis presents an empirical compact modeling framework for FinFET devices that extends the well-established Angelov model formulation at room temperature to accurately reproduce DC drain current characteristics from ambient down to cryogenic temperatures. The proposed model introduces temperature aware modifications that capture the dominant trends shaping DC I–V behaviour while ensuring smooth parameter evolution across the full temperature range. The approach is validated on a commercial 16-nm FinFET technology, demonstrating very good agreement with measured characteristics across bias conditions, temperatures, and maintaining numerical robustness and compact model efficiency. The formulation supports predictive DC modeling that if integrated with model of the nonlinear dynamic behaviour of the transistor, can be suitable for RF design of cryogenic integrated circuits. Beyond reproducing DC I–V curves, the methodology provides a practical path for technology bring up and PDK development at cryogenic temperatures, facilitating design portability and performance optimization for cryo-CMOS circuits. Collectively, the results establish a reliable, implementation ready model foundation for RF applications in quantum computing integrated circuits using advanced FinFET nodes.

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List of Acronyms

ADS	Advanced Design System
BSIM	Berkeley Short-channel IGFET Model
CAD	Computer-Aided Design
CMOS	Complementary Metal-Oxide Semiconductor
CLM	Channel Length Modulation
Cryo-CMOS	Cryogenic Complementary Metal-Oxide Semiconductor
DC	Direct Current
DIBL	Drain-Induced Barrier Lowering
DUT	Device Under Test
DAC	Data Access Component
FinFET	Fin Field-Effect Transistor
g_{DS}	Output Conductance
g_m	Transconductance
GIDL	Gate-Induced Drain Leakage
I_{DS}	Drain to Source Current
I-V	Current Voltage
IC	Integrated Circuit
LNA	Low Noise Amplifier
L	Channel Length of Transistor

MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
n-MOS	n-Type Metal-Oxide Semiconductor
PDK	Process Design Kit
p-MOS	p-Type Metal-Oxide Semiconductor
QC	Quantum Computing
QD	Quantum Dot
RF	Radio Frequency
RT	Room Temperature
SCE	Short-Channel Effect
SOI	Silicon On Insulator
SS	Subthreshold Swing
V_{DS}	Drain to Source Voltage
V_{th}	Threshold Voltage
V_{GS}	Gate to Source Voltage
W	Channel Width of Transistor

Chapter 1
Introduction and Background

1.1. State of the Art

Modern quantum processors consist of a small number of qubits that operate at cryogenic temperatures (millikelvin) which are controlled and read by general-purpose RF/microwave lab equipment rather than at room temperature [1, 2]. This restricts the qubit count to under 100. To execute algorithms for real-world applications that account for quantum error correction , future quantum processors would need millions of qubits. Therefore, to minimize thermal load, the control and readout circuits should be built as highly integrated chips, positioned as close to the qubits as feasible, and run at cryogenic temperatures (a few kelvin) [3]. Scaled Complementary Metal-Oxide Semiconductor (CMOS) is the only technology capable of operating at cryogenic temperatures, enabling the high degree of integration needed to successfully manipulate a large number of qubits. Furthermore, solid-state qubits made in standard CMOS can operate at higher temperatures (a few kelvin rather than millikelvin), which enabling the integration of both qubits and control/readout electronics onto a single cryogenic chip [4, 5]. Additionally, the power constraints (< 1 W @ 4 K) for the refrigerator that must cool the entire quantum processor are relaxed [6]. Solid-state qubits and suitable readout circuits operating in the analog domain, from 1 GHz to 10 GHz, are implemented using several different technologies [7]. As shown in Fig. 1.1, state-of-the-art readout topologies are essentially RF transceivers. An incident wave is directed towards the gate of a Field Effect Transistor (FET), which serves as the information unit (qubit). The reflected wave then travels via a passive circulator [8, 9] to an RF channel receiver, whose first and most important component is a low-noise amplifier (LNA) [10].

In the literature, various solutions based on 40-nm [1, 2] [3] [6] and 28-nm [11] CMOS technologies have been proposed, demonstrating that this technology is appropriate for quantum applications. This thesis addresses a critical challenge in the development of cryogenic integrated circuits by investigating the behaviour of ultra-scaled semiconductor devices, specifically 16-nm FinFET technologies, under cryogenic operating conditions. The main objective is to enable accurate modeling of Fin Field Effect Transistor (FinFET) devices at deep cryogenic temperatures, where conventional foundry-provided Process Design Kits

(PDKs) are no longer valid. While standard PDKs are typically characterized down to temperatures of approximately −80 °C, key building blocks in qubit readout electronics, such as low-noise amplifiers, are required to operate reliably at temperatures as low as 4 K. Addressing this modeling gap is essential for designing robust, high-performance cryogenic CMOS circuits.

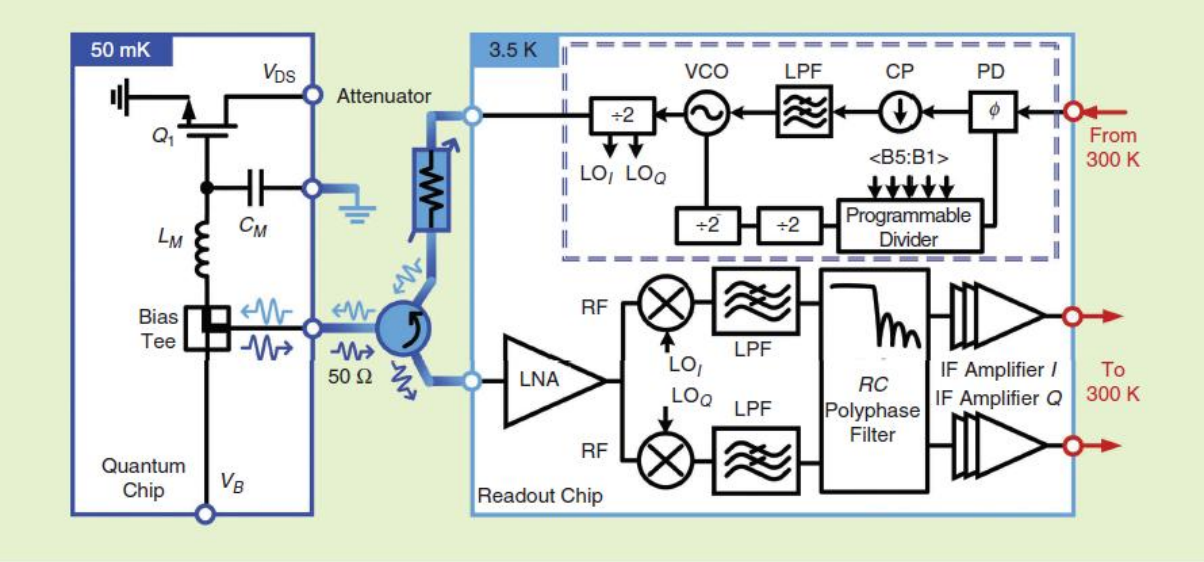

Figure1.1. The principle of gate-dispersive readout. The quantum dot receives a weak radio frequency signal produced in situ by a phased-locked loop through a circulator. The low-noise amplifier (LNA) amplifies the reflected signal and down converts it to in-phase and quadrature components (I/Q), which are then filtered and amplified. Adopted from [1]

The LNA, which has historically been realized in compound semiconductors such as InP and GaAs (HEMT) or SiGe (HBT) [10], exhibits outstanding noise performance at low temperatures below 4 K and has been the subject of a great deal of research. The Attempts to precisely describe the linear and nonlinear behaviour [12, 13] and noise [14] of LNAs down to cryogenic temperatures [10, 15] enabled the exceptional performance demonstrated by these technologies. Therefore, the absence of accurate models and modelling techniques for nanometre CMOS operating in such a difficult regime is the largest obstacle to overcome when building CMOS integrated circuits at these temperatures and frequencies.

A unified compact model that can be used for circuit design across ambient and cryogenic temperatures remains a challenge [16-18], even through numerous physics-based models that account for cryogenic effects have also been established for CMOS devices [12, 19-21]. With

ultra-scaled transistors like 16-nm FinFET, this deficiency is much more noticeable. Furthermore, major physical phenomena such as interface trapping [13, 22] and incomplete ionization [23] have not yet been appropriately incorporated into any of these models**.**

Because microwave measuring systems are inherently complicated, cryogenic operation presents difficulties for both linear and nonlinear characterization of microwave devices [24], which is the primary cause of the lack of trustworthy models. The literature reports , basic DC I/V characterization of FinFET devices [1, 6, 21] at a few kelvin. However, to date, on-wafer S-parameter measurements i.e., the microwave fundamental measurements required to derive compact models have been limited to operating up to the typical working frequency of qubit readout circuits. It is necessary to construct ad-hoc calibration standards and de-embedding processes to enable accurate small-signal characterization of either bare devices or full circuits in order to achieve accurate calibration operations up to the real device reference planes within the cryostat.

1.2. Motivation

In addition to being unreliable for operation at cryogenic temperatures, where the device behaviour not only varies with respect to room temperature (RT) but also deviates significantly from that inferred by extrapolating the parameters temperature dependence within the standard operating range, CMOS foundry models are often not optimised for high frequency design. In the worst case, this could require the development of non-standard circuit topologies due to IC performance drift. Currently, the prevailing design methodology involves using RT foundry models and standard design techniques, followed by design modifications based on physical cryogenic considerations. For example, adding resistive elements to the matching networks to equalise gain and fix the quality factor across temperatures, or adopting an adjustable bias to accommodate potential headroom issues related to threshold voltage variations. Compact models that take into amount physical processes that occur at cryogenic temperatures such as the freeze-out effect, higher threshold voltage, bandgap widening, increased mobility, reduced scattering, and sub-threshold swing degradation are well known [11]. As the input capacitance and output conductance vary with temperature, device matching also shifts by a few kelvin. The availability of a precise compact model that is directly derived from cryogenic temperature measurements is a crucial tool that enables improved design optimisation and modelling [16- 18].

This thesis aims to develop a novel device modelling technique and formulation to predict the behaviour of the DC drain current under cryogenic conditions, based on modifications to Angelov's model well known model. The implemented model can then be used for the design of integrated circuits that are part of the qubit readout circuits as, for example, in Quantum Computing. Cryogenic microwave electronic circuits play a key role in quantum computing and in several other scientific fields, including deep-space radio communications, high-energy physics experiments, and radio astronomy for the study of the cosmic microwave background.

The accurate design of such integrated circuits critically depends on the availability of reliable device models valid at cryogenic temperatures. Therefore, establishing a systematic and robust methodology for device characterization and microwave-design-oriented model extraction at cryogenic conditions is of paramount importance to the microwave and microelectronics engineering community [25]. Furthermore, this thesis presents, the cryogenic characterization and modeling of advanced (FinFET) and investigates the performance of 16 nm FinFET technology from room temperature to cryogenic temperatures [26].

1.3. Quantum Computing

Quantum computing can solve problems that would take classical computers millennia to solve; global interest and enthusiasm for it have surged. This intricate ecosystem-powered by unprecedented processing capacity and novel quantum algorithms, has attracted substantial funding from both venture capitalists and governments. Recognizing its strategic importance, the early 21st century witnessed a "Quantum Gold Rush" that accelerated research and development [27]. Quantum computing promises a transformative impact across numerous sectors, including materials science, pharmaceuticals, cybersecurity [28], finance, manufacturing, and beyond.

The idea of quantum computing gained momentum after Richard Feynman's 1981 proposal to simulate quantum systems using quantum computers (QCs) [29]. In classical computing, a bit is either 0 or 1, whereas in quantum computing, a quantum bit (qubit) exists in a superposition of $|0\rangle$ and $|1\rangle$ on the Bloch sphere. In 1994, Peter Shor introduced an algorithm that can factor large integers in polynomial time, undermining the security of RSA and other classical cryptographic systems [30]. Shor's work showcased the revolutionary potential of quantum

computing by demonstrating how quantum principles can solve problems beyond the reach of classical machines.

However, quantum systems face major technical challenges. Coherent quantum states are fragile and highly susceptible to decoherence from external noise, leading to information loss from superposition states. Since quantum algorithms require long coherence times, this fragility hampers reliable computation. Moreover, as analog devices, quantum computers are prone to calculations errors. Fault-tolerant computing techniques [31], such as surface codes for quantum error correction (derived from Kitaev's toric codes), can mitigate these errors, but implementing them is resource-intensive [32].

Two critical obstacles to building large-scale quantum computers are decoherence and operational inaccuracies [33]. In recent decades, significant progress has been made in improving gate fidelity and coherence time. Various platforms, such as photonic qubits, quantum dots [4], trapped ions, and superconducting qubits [34] have been explored, each with advantages and limitations in scalability, fabrication complexity, noise susceptibility, and operational mechanisms. Benchmarking between platforms remains challenging.

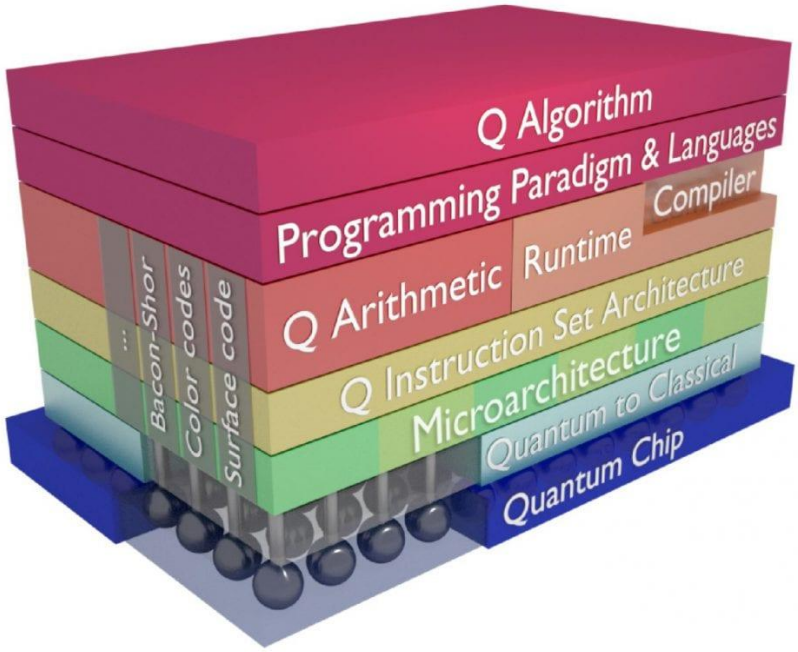

Figure 1.2. Layered architecture of a quantum computing system, from hardware to software: starting with the quantum chip, through instruction set architecture, quantum arithmetic with error correction codes, runtime and compiler, up to programming languages and quantum algorithms. Adopted from [35]

The fundamental difference between classical and quantum computing lies in the way information is stored and manipulated [36]. Classical computers store data as bits, whereas quantum computers use qubits, exploiting superposition and entanglement to address problems intractable for classical systems. For effective qubit control and readout, CMOS electronics must be placed close to the Quantum Processing Unit (QPU) [37]. Due to the limited cooling capacity of dilution refrigerators, these control electronics must have a minimal footprint. Short-channel CMOS devices need accurate modelling and characterization at cryogenic temperatures [38, 39], particularly above 1 K for monolithically integrated designs. At these temperatures, spin qubits exhibit higher resonance frequencies due to increased splitting energies, requiring faster-switching devices. Advances in ultra-short nano-geometries in non-planar devices have reduced integrated circuit area, but scaling down at cryogenic temperatures does not necessarily yield better performance.

1.3.1. Towards Large Scale Quantum Computers

The aim of "quantum supremacy" is to show that a programmed quantum computer can resolve an issue that no classical computer can in a manageable amount of time. Despite recent quantum computer implementations demonstrating quantum supremacy with 53 superconducting qubits [40], practical applications of quantum computers are still a long way off. Scaling up to a few thousand logical (ideal) qubits is necessary for quantum computers to be realistically viable. Each of these qubits may need tens of physical qubits for error correction [41].

Modern quantum computers have mostly been developed using superconducting transmon qubits. Superconducting LC resonators [42] that are defined lithographically are used to implement these qubits. Although these qubits have desirable characteristics, such as complete electrical control and excellent operational fidelity (>99.9% accuracy), they are not appropriate for scaling due to their relatively large size (0.1-1 mm^2 per qubit). Moreover, because of the cooling power constraints of the dilution chiller, these qubits normally function at 10-100 mK, reducing the quantum processor's power usage to about 100 μW [43]. Therefore, the electronic devices needed for classical control and qubit readout, such as oscillators and arbitrary waveform generators, are connected to the quantum computer via long cables and attenuators and cannot be integrated on the same chip as the qubits.

A well-liked substitute for superconducting qubits in recent years has been quantum dot-based qubits. Specifically, it has been experimentally shown that quantum dot spin qubits used in FinFETs operate at temperatures far higher than those of superconducting qubits (4 K) [44]. This significantly increases the QC's maximum power consumption to about 1.5 W [43] while reducing the required cooling power. These devices strong spin-orbit coupling enables complete electrical control of spin without additional components. These benefits, together with the fact that these qubits are smaller than 100 nm, make them a prime contender for the development of quantum computers with thousands of qubits packed onto a single chip along with their readout and control circuitry.

The majority of applications of quantum dot-based spin qubits rely on experimental laboratory technologies, and the technology is currently in its very early phases of development. The development of a monolithically integrated quantum processor requires overcoming several obstacles [41]. It is necessary to find a commercially feasible semiconductor technology that enables the deployment of high-performance classical Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) and semiconductor qubits with minimal process modification [45]. To enable the design and verification of electronic circuits and systems, it is also crucial to predict the behaviour of these devices down to cryogenic temperatures.

1.3.2. Quantum Bits

Analog and digital architectures are both found in classical computers. Digital architectures use bits to store, analyse, and send data. A classical bit, which can have a value of either 0 or 1, is the basic unit of information in classical computers. Memory cells are used to store information, and a memory register with N cells can contain up to 2^N states. Though the N-bit memory register has 2^N possible states, it can only ever be in one instantaneous state at a time, which is determined by one of the N-bit strings. The Central Processing Unit (CPU) of a traditional computer receives information from the memory and uses it to process and calculate the input bits [46]. According to a hardware-defined mapping, the processing unit outputs a single, predetermined N-bit string for every N-bit input string.

Quantum bits (qubits) are the quantum counterpart of classical bits. According to Dirac's notation, a qubit is any two-level quantum mechanical system in which information can be encoded in the base states, which are denoted by $|0\rangle$ and $|1\rangle$. Each qubit can exist in a

superposition of the two base states, as indicated by the wavefunction, according to quantum physics.

$$|\psi\rangle = \alpha_p|0\rangle + \beta_p|1\rangle \qquad (1.1)$$

With α_p and β_p representing the probability amplitudes associated with the two base state vectors, respectively. This state is represented graphically in the so-called Bloch sphere [47] in Figure 1.3.

A quantum register composed of N qubits has 2^N potential states, just like a conventional computer. On the other hand, the quantum register can be in a superposition of its 2^N base states with specific probability amplitudes or, in a classical way, bit strings and quantum operations [46] at any given time because each qubit state can be a superposition of the two base states will operate by simultaneously establishing an input-output mapping between each of these 2^N computational states. The ability to perform operations on all states in parallel defines a crucial property the processing capacity of quantum computers increases exponentially with the number of qubits.

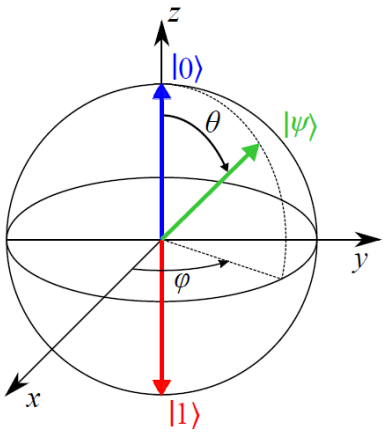

Figure 1.3. The qubit state $|\psi\rangle$ (green) is represented as a point on the surface of the Bloch sphere. The basis states $|0\rangle$ (blue) and $|1\rangle$ (red) are at the north and south poles of the Bloch sphere, respectively. A rotation by an angle θ of the state $|0\rangle$ to obtain the state $|\psi\rangle$ is an example of a single qubit operation. Adopted from [6]

However, only when the qubits interact can the entire set of quantum states be accessed. Even when N qubits are isolated, only separable states can be accessed without interaction, limiting the creation of entangled states . Specifically, isolated single-qubit quantum states can realize certain multi-qubit states, meaning that the wavefunction $|\psi\rangle$ can be decomposed analytically into distinct functions that only involve one qubit at a time. Nonetheless, certain states like Bell state$|\psi\rangle = (|00\rangle + |11\rangle)/\sqrt{2}$ need interactions between qubits because they cannot be

decomposed into separate single-qubit states. There is no classical analog for the phenomenon of entanglement, which is represented by such states. Even when two qubits are isolated from one another and do not appear to interact, their states remain connected if they are entangled.

1.3.3. Spin Qubits

In spin qubits, electron spin is used to store quantum information. Quantum Dots (QDs), which are nanostructures that can confine electrons to allow for individual spin control, are one example of a physical implementation of a spin qubit [47-49]. To order to accomplish this goal, quantum dots have been studies since their first proposal for quantum computation [50].

Quantum dots are typically produced in semiconductor heterostructures [48]. Electrons can be confined in the two other directions. Each side of the island has quasi-metallic charge reservoirs that electrons can move on and off. The source-drain voltage can controls transport across the dot, but a gate can also adjust transport using via the island's potential. In this case, charge tunnelling events can occur across the potential barriers until the energy required to add an electron to the dot exceeds the chemical potential of the leads. Pauli's exclusion principle states that no more than two electrons with opposite spins can occupy the lowest energy level in a very small quantum dot.

DC methods are frequently used for qubit state readout. As an alternative, methods for Radio Frequency (RF) [51] have been proposed for semiconductor qubit readout. Radio-frequency reflectometry and Dispersive Gate Sensing (DGS) [52] are the two primary methods developed. Quantum Point Contact (QPC), [51] a narrow channel, or a Single-Electron Transistor (SET) [53] are used in generic radio-frequency reflectometry.

1.3.4. Superconducting Qubits

Superconducting qubits are devices that are made entirely of superconducting materials and architectures. Although there are several varieties of superconducting qubits, the transmon variety is thought to be the most well-known. The transmon qubit is a nonlinear microwave resonator [42].

The resonance frequency of a harmonic oscillator can be defined as $\omega_0 = 1/\sqrt{LC}$ and the location of the parallel resistance is its quality factor $Q = R\sqrt{C/L}$. The energy levels of such a harmonic oscillator are quantized in the quantum mechanical limit in accordance with:

$$E_{n,LC} = \hbar\omega_0 \left(n + \frac{1}{2}\right) \qquad (1.3)$$

where n is a non-negative integer index, and $\hbar$ is the reduced Planck constant. This indicates that a harmonic mechanical oscillator's ground state has nonzero energy and that the subsequent energy levels are evenly spaced, with an energy spacing of $\hbar\omega$. At the oscillator resonant frequency, the energy difference between two successive energy levels is equivalent to the addition or subtraction of one microwave quantum of energy. A qubit's base states, which are $|0\rangle$ and $|1\rangle$, can be determined using the two lowest energy levels.

Superconducting qubits and quantum dot qubits [54] must be kept in dilution freezers at extremely low temperatures, usually a few Kelvin or milli-Kelvin. Furthermore, unique signals are required to manipulate each qubit, necessitating a large number of cables to connect qubits in a cooled chamber to room-temperature sensors.

1.4. Cryo-CMOS for Quantum Computing

The complicated connectivity problem on the path to large-scale quantum systems can be resolved with the introduction of cryo-CMOS technology. According to Figure 1.5, which shows the evolution of quantum computer hardware design, a traditional method can only support a small number of qubits, with instruments outside the refrigerator and individual cables connecting the qubits within.

Scientists and researchers have recently created analog and digital building blocks that operate at 4 K, enabling them to run more qubits than they could with a traditional method. Qubit read-out or control circuits can be implemented using a variety of devices working at a few Kelvin, such as mixers, (de) multiplexers, DACs (Digital-Analog Converters)/ADCs (Analog-Digital Converters), RF LNAs (Low Noise Amplifiers) [55], VCOs (Voltage-Controlled Oscillators)/PLLs (Phase-Locked Loops), and FPGAs (Field-Programmable Gate Arrays) [56].

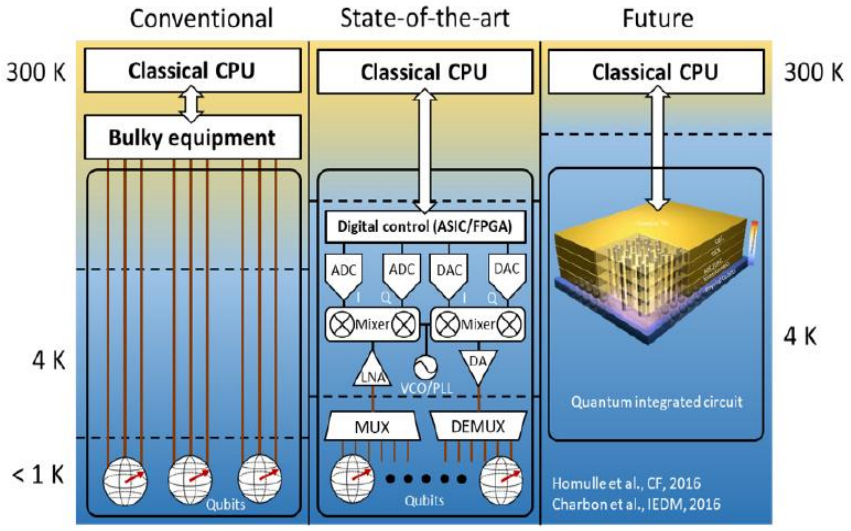

Figure 1.4. Development of hardware for quantum computers that can scale. In a traditional method, a few qubits are controlled by large, room-temperature equipment that uses separate cabling. Cutting-edge research starts with front-end electronics up to 4 K to support more qubits in a system. In the future, electronics and qubits are monolithically merged on a single chip in a QIC (Quantum Integrated Circuit). Adopted from [57, 58]

Furthermore, cryo-CMOS ASICs (Application-Specific Integrated Circuits) enabling qubit readout and control circuits have been made in 40 nm or 28 nm technologies [59].

Additionally, as shown in Figure 1.5, right column, qubits and circuits can be monolithically produced on the same device thanks to improvements in qubit operating temperature [60]. Electronics can have a larger thermal budget when qubits are operated at temperatures above one Kelvin rather than at sub-kelvin temperatures. Such a strategy improves scalability while resolving the connection issue.

A potential approach to achieving the monolithic QIC is the gate-defined spin qubit. There are two primary causes for this: (i) it can be operated at a greater working temperature [61], and (ii) it is very compatible with the CMOS process, which enables industrial manufacturing [62]. The strong quantum confinement is the cause of the latter. In a quantum dot, it results in enough energy splitting. The charging energy, defined as the energy required to add one electron to a quantum dot, is related to this discrete energy. When the thermal energy is much lower than the charging energy, quantum phenomena such as Coulomb blockade are more reliable. To improve the quantum confinement, several device shapes have been proposed, including edge-defined, triangle-shaped, and diamond-shaped channels.

1.5. Challenge

Designing Cryo-CMOS circuits with high gain and low noise within 1 W of cooling power at 4 K [3] is a difficult problem, particularly given the absence of accurate compact models for high-level electrical simulations of cryogenic ICs. According to Akturk et al. [63], transistor current-voltage performance at 100 K cannot be predicted using the distributed compact model with conventional temperature dependences. To guarantee circuit operation, designers often use a mature SPICE (Simulation Program with Integrated Circuit Emphasis) model and a room-temperature Process Design Kit (PDK). However, there is no assurance that the circuit will function at low temperatures. This method prolongs the engineering cycle and fails to validate cryogenic concepts. To enhance the current compact models used at cryogenic temperatures, it is important to incorporate new formulae or parameters.

1.6. Thesis Layout

A comprehensive compact model for the drain current generator of a16 nm FinFET, based on cryogenic DC-IV measurements at both room and cryogenic temperatures, will be described in the thesis to support the trustworthy development of cryogenic microwave electronics.

- Chapter 1 is about the introduction and background of quantum computing QC which provides the overall motivation and context for the research. It introduces the fundamental principles of quantum computing, Qubits and their types and highlights the role of advanced semiconductor devices. The conventional CMOS technologies and associated challenges at cryogenic temperatures, establish the need for a detailed investigation of FinFET devices for cryogenic and quantum applications. The objectives, scope, and key contributions of the thesis are also outlined.

- Chapter 2 presents the technological foundations of FinFET technology. It covers the evolution of FinFET, its core technology, working principle, characteristics and performance advantages over planar MOSFETs. Key device parameters and scaling challenges relevant to cryogenic temperature and radio frequencies (RF) applications.

- Chapter 3 focuses on the experimental characterization of FinFET devices at room and cryogenic temperatures . The geometry, device specifications, matrix configurations,

and Die layout are described. We have measured different FinFET devices at room and cryogenic temperatures. DC-IV characterization including transfer characteristics, output conductance, and transconductance. Also, performed a comparison of short and long-channel devices at different temperatures. An extensive measuring campaign on unit-size bare devices, both at room and cryogenic temperatures, with the goal of extracting small models. Specifically, DC - IV characterization data have been used for modelling purposes.

- Chapter 4 describes the development and refinement of compact models suitable for 16 nm FinFET technology operation at room and cryogenic temperatures. Extracted parameters from experimental data are incorporated into the modeling framework. Model accuracy is evaluated through comparison with measured results, and validation is performed across different bias and temperature conditions. The chapter concludes with a discussion on the applicability of the proposed models for integrated circuit-level simulation.

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Chapter 2
Fundamentals of FinFET Technology

2.1. Introduction

The semiconductor industry faces the constant challenge of reducing device dimensions while preserving efficiency and durability, as demand for high-performance, low-power, and compact electronic systems continues to rise. The performance, functionality, and power efficiency of integrated circuits have significantly improved over the decades due to the ongoing miniaturization of transistors, governed by Moore's Law [1]. But serious drawbacks have emerged as conventional planar Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) approach deep sub-20 nm technology nodes. Device performance has declined, and scalability has decreased due to phenomena such as drain-induced barrier lowering (DIBL) [2], threshold voltage roll-off, and increased leakage currents. [3, 4]Together, these phenomena are referred to as short-channel effects (SCEs) [5, 6]. They are caused by the inability of planar transistors to efficiently regulate the channel potential as their dimensions decrease, which limits further device scaling.

Researchers developed a unique transistor architecture, the Fin Field-Effect Transistor (FinFET), to address these pressing issues. FinFETs use a three-dimensional, multi-gate construction, in contrast to traditional planar MOSFETs, in which the conducting channel is shaped like a thin, vertical “fin” that protrudes from the substrate [7]. The gate material minimizes short-channel effects and provides improved electrostatic control over the channel by wrapping around the fin on several sides, typically three. Because of its special geometry, the FinFET can improve drive current, improve subthreshold slope [8], and lower leakage currents without sacrificing power efficiency [9]. Consequently, FinFETs outperform planar counterparts in performance, power consumption, and reliability [10].

FinFETs also provide additional benefits from a fabrication perspective. Their design allows for a more seamless transition from planar MOSFETs to three-dimensional device architectures, as it is highly compatible with current CMOS process technologies [11]. Nowadays, FinFETs are widely used in advanced process nodes, including 22 nm, 16 nm, 14 nm, 10 nm, and 7 nm, and they serve as the basis for contemporary high-performance CPUs

and system-on-chip (SoC) architectures [7, 12]. Ongoing research focuses on optimizing FinFET materials, fin shape, and gate work functions, in as well as advancing structural and electrical design to further increase device scalability , reduce variability, and improve thermal management [13, 14].

By eliminating the fundamental drawbacks of planar MOSFETs and advancing the semiconductor miniaturization roadmap, FinFET technology represents a paradigm shift in transistor design [15]. The FinFET is a key component of modern nanoelectronics, opening the door for the upcoming generation of integrated circuits and sophisticated computer systems with its exceptional performance, power efficiency, and manufacturing feasibility [16, 17].

2.2. Evolution from MOSFET to FINFET

Transistor technology has advanced significantly throughout time to meet the electronics industry's ever-increasing demands. Beginning with the conventional MOSFET and on to the 3D structured FinFET, this section explores the development of field-effect transistors.

In the development of electronic devices, the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is an essential part. By changing the voltage applied to the gate terminal, the device modulates current flow through a semiconductor material, an insulating oxide layer, and a metal gate. Although Julius Edgar Lilienfeld who patented the MOSFET concept in the 1920s, the concept was first proposed in the early 1900s. However, it wasn't until the 1960s when Bell Labs' Dawon Kahng and Martin M. Atalla created the first functional device [18- 20].

When voltage is applied to the gate of a MOSFET, an electric field is produced. A conductive channel is created by this field either by attracting carriers (enhancement mode) or by repelling carriers (depletion mode). The dynamics of the PN junction, which occurs when a P-type (positive) and N-type (negative) semiconductor are linked to form a depletion zone, are crucial to the underlying physics. One can regulate the conductivity between the source and drain terminals by applying an external voltage to this area [19]. To further clarify, let's look at the key distinction between the two main MOSFET types: pMOS and nMOS. The primary differences between these versions are the electrical characteristics and the type of carriers (electrons or holes) that participate in conduction.

Over the past few decades, the semiconductor industry has relied heavily on planar CMOS technology. However, mobility deterioration and large leakage currents resulting from the high doping concentrations required for scaling make it impossible to continue miniaturizing bulk CMOS technology [21]. Traditional MOSFET technology has drawbacks, particularly high leakage and poor reliability.

The challenge of developing integrated circuits gets more difficult as chip and system complexity rise. FinFETs are a revolutionary answer to these problems. The Fin Field-Effect Transistor (FinFET) is an evolutionary step forward from the conventional MOSFET [22]. Improved electrostatic control is provided by its three-dimensional "fin"-shaped silicon structure that extends over the substrate, as shown in Figure 2.1.

FinFET devices use a 3D wrap around gate structure that resembles a fish fin, hence the name, as opposed to the flat gate electrode used in traditional CMOS. This improves the device's electrostatic control over the channel, which in turn could improve the I_{on}/I_{off} ratio, stability, short-channel performance, and operating speed [23, 24]. These transistors provide observable advantages such as better control over short-channel effects, increased power, and improved performance scalability [25].

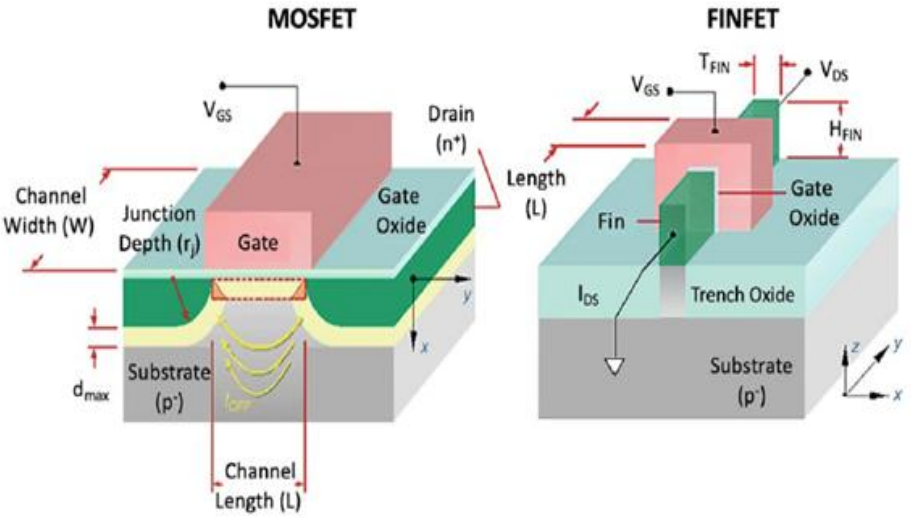

Figure 2.1. Structural comparison between MOSFET and FINFET. In the MOSFET, current flows laterally through a planar channel. In the FinFET, a vertical fin-shaped channel with height and thickness is surrounded by the gate on multiple sides, providing improved electrostatic control, reduced short-channel effects, and lower leakage compared to the planar design. Adapted from [19]

In 1999, Chenming Hu invented the "FinFET," [19, 26] short for Fin Field Effect Transistor, which marked a key milestone by packing a record number of transistors onto a chip. The problems with planar MOSFETs, particularly at the deep sub-micron sizes, were the impetus for this technical development. Although the fundamental idea is still the same as in MOSFETs, regulating the current flow between the source and drain via the gate voltage, the significant distinction is in their construction [27]. Traditionally, MOSFETs are planar devices with the gate situated above the channel. By contrast, a FinFET employs a three-dimensional fin-like structure that rises above the substrate plane.

2.3. FinFET and Its Core Technology

A FinFET is a multi-gate device, a MOSFET built on a substrate with the gate wrapped around the channel or positioned on two, three, or four sides of it [28]. Double-gate FinFETs are FinFETs with a thick oxide covering the fin. Hyperbolic silicon layers, which drastically reduce the electric field from the gate to the fin [29], can be incorporated into the design to compensate for the additional silicon. Tri-gate FinFETs are FinFETs with thin oxide coatings on the top and sides of the fin [8, 24]. Transistors can be positioned closer together to increase packing density, and the fin height can be increased to increase energy efficiency [9]. To sum up, FinFETs are a significant advancement in transistor technology that offer better control, reduced leakage, and enhanced performance , particularly in advanced semiconductor processes. The three-dimensional multi-gate design is the basis of FinFET technology, which makes it a powerful force in the manufacturing of modern semiconductors.

2.3.1. Working Principle and Characteristics of FinFET

The FinFET consists of a thin silicon fin that is positioned vertically on the substrate. With this arrangement, transistor performance is enhanced by providing improved electrostatic control of the channel. FinFETs employ a tri-gate design with three-sided gate control and represent an intermediate step toward gate-all-around (GAA) architectures, in which the gate surrounds the channel, enabling even stronger electrostatic control [30]. This gate-all-around design differs from the conventional planar MOSFET, which has the gate on the top surface.

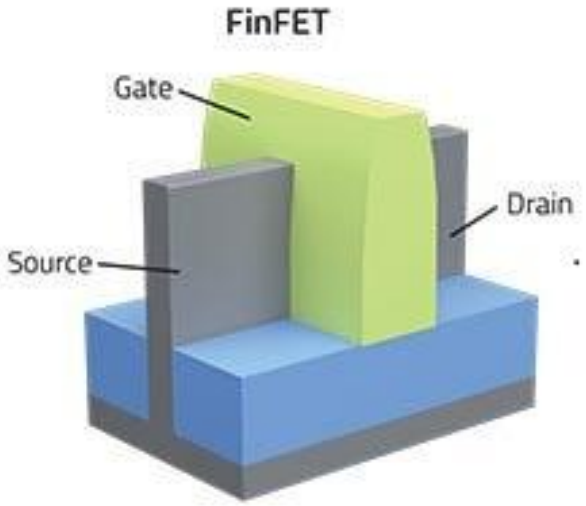

Figure 2.2. Three-dimensional schematic of a FinFET device structure.

In FinFETs, applying a gate voltage generates an electrostatic field that modulates the current flowing through the fin between the source and drain terminals, thereby turning the device on or off. The three-dimensional construction reduces leakage current in the off state and allows for more efficient channel regulation [31]. By addressing the problems caused by shorter channel lengths, the multi-gate architecture's front and rear gates offer improved electrostatic control over the channel. By mitigating short-channel effects induced by aggressive channel scaling, the multi-gate architecture improves subthreshold behaviour and reduces leakage current, thereby enhancing energy efficiency.

2.4. FinFET Structure Classification

The following are some categories under which FinFETs can be divided.

2.4.1. Based on Physical Structures

FinFET technology can be divided into two primary categories: SOI (silicon on insulator) FinFETs and Bulk FinFETs. Each kind has unique operating and structural characteristics. Because they share a substrate, the individual fins in bulk FinFETs are physically connected. Conversely, physically isolated fins that do not make direct contact are a characteristic of SOI FinFETs [10, 32]. Figure 2.3 shows the fundamental differences between these two FinFET types. The procedure of switching from planar MOSFETs to bulk FinFETs is rather simple because bulk FinFETs closely match the conventional planar MOSFET structure. Because of their ease of integration and structural similarity, bulk FinFETs are preferred by many businesses. Nevertheless, engineers continue to debate whether Bulk FinFETs or SOI FinFETs

are better, given factors such as cost and performance [33, 34]. The complex interaction of these factors and specific design specifications determines which type is most convenient to use.

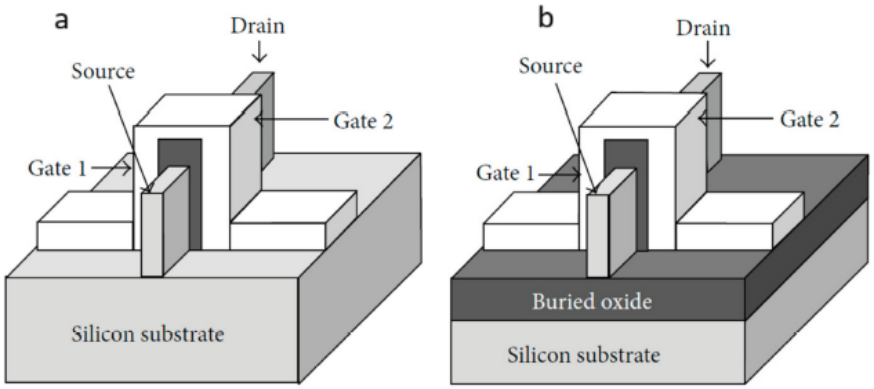

Figure 2.3. Structure schematic of (a) Bulk FinFET and (b) SOI FinFET. Adopted from [10]

2.4.2. Based on the Number of Terminals

Based on the number of terminals, FinFETs can be divided into: Independent Gate (IG) FinFETs, which have four terminals, and Short Gate (SG) FinFETs, which have three. Their structural layout is the primary difference between these two groups. IG FETs have gates that are physically insulated by a dielectric layer, whereas SG FinFETs have two gates, that are shorted and physically coupled to one another. The structural variations between these two FinFET types are shown graphically in Figure 2.4.

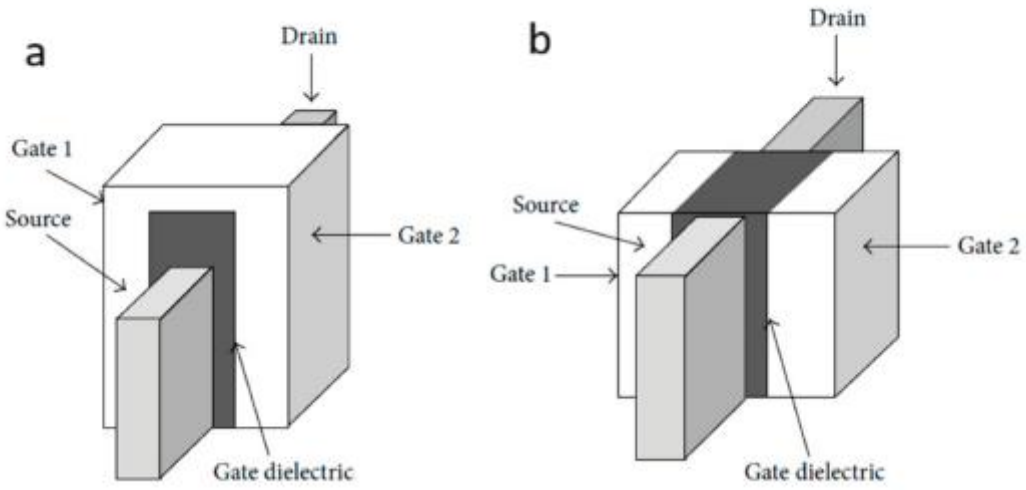

Figure 2.4. Structure schematic of (a) SG FinFET and (b) IG FinFET. Adopted from [10]

There is a noticeable difference between SG and IG FETs: SG FETs have higher I_{on} and I_{off} values, because both gates control the channel. On the other hand, by enabling the application of different voltages and signals to the gate terminals, IG FETs offer more controllability over transistors. However, a more thorough fabrication approach is required due to the increased flexibility of IG FETs [9, 32]. Furthermore, because of their special ability to modulate the voltage of one gate, either up or down, via the other gate, IG FETs offer an improved I_{on}/I_{off} ratio. As a result, IG FETs are more appropriate for power management applications [10].

2.4.3. Based on Dielectric Thickness

As shown in Figure 2.5 FinFETs can also be classified by dielectric thickness into double-gate (DG) and tri-gate FinFETs. A hard mask is used on top of the transistor structure in DG FinFETs to guarantee that the effective channel width is twice the fin height (2n × Fin height) [35]. A split transistor is the name given to this kind of FinFET. Tri-gate FinFETs, on the other hand, have a distinct characteristic. The effective channel width in tri-gate FinFETs is equal to the channel width of the DG FinFET plus the fin width (W_{fin}) when the dielectric thickness decreased. Thus, with tri-gate FinFETs, the overall channel width is computed as $2n\times$ Finheight + W_{fin} [1, 36]. Because tri-gate FinFETs have reduced gate-to-source capacitance due to this design change, they perform better and offer clear advantages in applications such as sensors, memory devices (SRAM), radar signal processors, smart cameras and RF circuits. The device's electrostatic integrity is maintained [9, 36, 37].

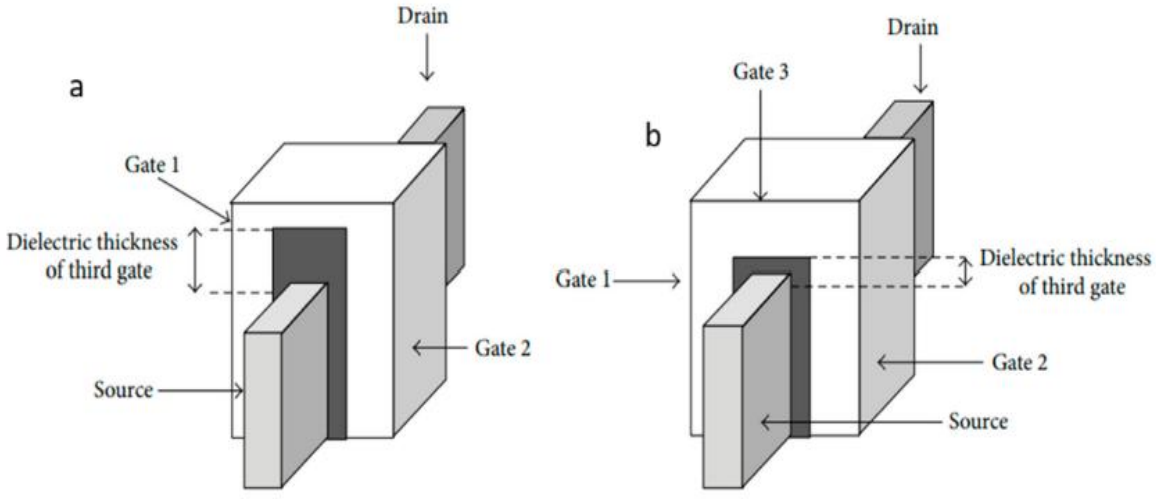

Figure 2.5. Schematic of (a) DG FinFET and (b) tri-gate FinFET. Adopted from [10]

2.5. Physics of FinFET

The electrical performance of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) has been progressively limited by the physical constraints inherent in planar device topologies as they continue to scale down into the nanometre region. Short-channel effects (SCEs) become a significant concern at such small dimensions. These effects occur when the drain potential begins to significantly affect the channel region's electrostatics, making it harder for the gate to regulate carrier flow. As a result, the subthreshold leakage current (I_{off}) increases, impairing switching behaviour and increasesing static power consumption. In low-power and mobile applications, where excessive leakage immediately reduces energy efficiency and shortens battery life, this issue is particularly problematic.

Earlier scaling strategies aimed to improve gate control by reducing the gate oxide thickness and using high-k dielectric materials to overcome these issues in conventional planar MOSFETs [38]. Thinner gate oxides improve the electrostatic control of the gate over the channel by increasing the gate capacitance. However, substantial gate leakage and gate-induced drain leakage (GIDL) [10] were caused by quantum mechanical tunnelling when the oxide thickness reached the atomic scale [39]. A new device architecture was required to provide greater gate control without relying exclusively on ultra-thin oxides, due to these phenomena, which made further planar scaling impracticable [38].

FinFET's physics is centred on its multi-gate, three-dimensional structure, which allows for improved electrostatic control. Leakage is decreased, current-driving capabilities are enhanced, and short-channel effects are effectively mitigated by this design. Because of its exceptional scalability and transconductance, it is the foundation of contemporary CMOS technology, supporting both high-frequency analog systems and sophisticated digital circuitry. Since the FinFET bridges the gap between traditional planar MOSFETs and the new gate-all-around transistor topologies that will shape the future of nanoelectronics, it is a significant technological milestone.

2.5.1. RF FinFET

In microwave and radio-frequency (RF) applications, FinFETs offer several key benefits. Low-noise amplifiers (LNAs), voltage-controlled oscillators (VCOs), and radio frequency switches are among the components that benefit greatly from their high transconductance and low

parasitic capacitances, which improve gain and frequency response. The tri-gate structure's greater electrostatic control also reduces distortion and noise, two factors critical to high-performance analog circuits [1].

The maximum oscillation frequency (f_{max}) and the cut-off frequency (f_t) are two important metrics commonly used to characterize the high-frequency performance of FinFETs. The ratio of the transconductance to the total gate capacitance determines the cut-off frequency (f_t), which is the frequency at which the device's current gain reaches unity [40]. Both extrinsic parasitic effects (such as contact and interconnect resistances) and intrinsic features (such as channel resistance, capacitance, and carrier velocity) affect the maximum oscillation frequency (f_{max}), which sets the upper limit for power gain [7]. To achieve the intended high-frequency response, device geometries must be optimized and precise FinFET modelling requires an understanding of these factors.

2.5.2. Electrostatics of Tri-Gate FinFET

Poisson's equation can be used to model the Tri-Gate FinFET as a three-surface controlled device with a potential distribution within the fin**.**

$$\nabla^2\psi(x,y,z) = -\frac{q}{\varepsilon_{si}}(p - n + N_D^+ - N_A^-) \qquad (2.1)$$

where ψ is the electrostatic potential inside the FinFET channel, q is the charge of an electron, p is hole concentration, n is the electron concentration, ε_{si} is the permittivity of silicon, N_D^+ and N_A^- are the ionized donor and acceptor concentrations, respectively [4]. In RF FinFETs, the space-charge term is insignificant in an intrinsic or lightly doped channel, thereby minimizing mobility degradation [3]. The potential inside the fin roughly satisfies Laplace's equation:

$$\nabla^2\psi(x,y,z) = 0 \qquad (2.2)$$

Analytical solutions show that the gate potential exerts near-ideal control over the surface potential, extending deeply into the fin [41]. This represents the effective gate capacitance per unit width:

$$C_{ox,eq} = \frac{\varepsilon_{ox}}{T_{ox}}(2H_{fin} + T_{fin}) \qquad (2.3)$$

C_{ox} effective gate oxide conductance, ε_{ox} permittivity of gate oxide, T_{ox} is the thickness of gate oxide, $H_{fin}\ and\ T_{fin}$ are the height and thickness of the fin. In microwave frequency operation, this improved gate coupling boosts gain and transconductance [26, 42].

2.5.3. High-Frequency Behavior

The cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) define the device performance at microwave frequencies [40].

$$f_T = \frac{g_m}{2\pi(C_{gs}+ C_{gd})} \tag{2.4}$$

where the intrinsic gate-source and gate-drain capacitances are denoted by C_{gs} and C_{gd}, respectively.

By enhancing channel screening, the tri-gate design lowers C_{gd} and increases f_t.

The maximum oscillation frequency, which considers parasitic resistances, is written as follows:

$$f_{MAX} = \frac{f_T}{2\sqrt{g_d\,(R_g + R_S)C_{gd}}} \tag{2.5}$$

Where R_g stands for drain conductance, R_s for source resistance, and g_d for gate resistance.

By optimizing fin height and gate material resistivity 16 nm FinFETs can achieve $f_t \approx 300 - 400$ GHz and $f_{max} \approx 250–350$ GHz [43] enabling their use in millimetre wave circuits.

2.5.4. Velocity Saturation and Ballistic Transport

Carriers can achieve saturation velocity v_{sat} (~1 × 10^7 cm/s) at short gate lengths (L_g = 16 nm), which limits the drain current [44].

The limited current due to velocity-saturation is determined by:

$$I_{sat} = W_{eff}C_{ox,eq}(V_{gs} - V_{th})v_{sat} \tag{2.6}$$

W_{eff} is the effective width, V_{gs} is the gate source voltage and V_{th} is the threshold voltage. Quasi-ballistic transport takes place in deeply scaled FinFETs, where the carrier mean free path (~ 10 nm) is similar to L_g.

Ballistic transport improves f_T and g_m because carriers move across the channel with little scattering.

2.5.5. Output Conductance and Intrinsic Gain

The change in drain current with drain voltage is represented by the output conductance (g_o):

$$g_o = \frac{\partial I_{ds}}{\partial V_{ds}} = \frac{I_{ds}}{V_A} \quad (2.7)$$

where V_A denotes the early voltage and the drain current is denoted by I_{ds} [45].

High output resistance in FinFETs results from superior channel control ($r_o = \frac{1}{g_o}$), yielding large intrinsic gain ($g_m r_o$),this is essential for microwave applications in low-noise amplifiers [7, 46].

2.5.6. Charge Control and Transconductance

A Tri-Gate FinFET's inversion charge per unit length can be represented as follows:

$$Q_{inv} = C_{ox,eq}(V_{gs} - V_{th}) \quad (2.8)$$

Where the drift-diffusion form is followed by the drain current (I_{ds}) under strong inversion:

$$I_{ds} = \mu_{eff} C_{ox,eq} \frac{W_{eff}}{L_g}(V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2} \quad (2.9)$$

where $W_{eff} = (2H_{fin} + T_{fin})$ represents the conducting channel's overall effective width [47].

The cut-off frequency and RF gain are directly impacted by the small-signal transconductance, which is:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \mu_{eff} C_{ox,eq} \frac{W_{eff}}{L_g} V_{ds} \quad (2.10)$$

μ_{eff} is the effective carrier mobility. At the same gate length, g_m in FinFETs is usually 30–50% higher than in comparable planar MOSFETs due to the tri-gate geometry. FinFETs are therefore well suited for microwave gain stages.

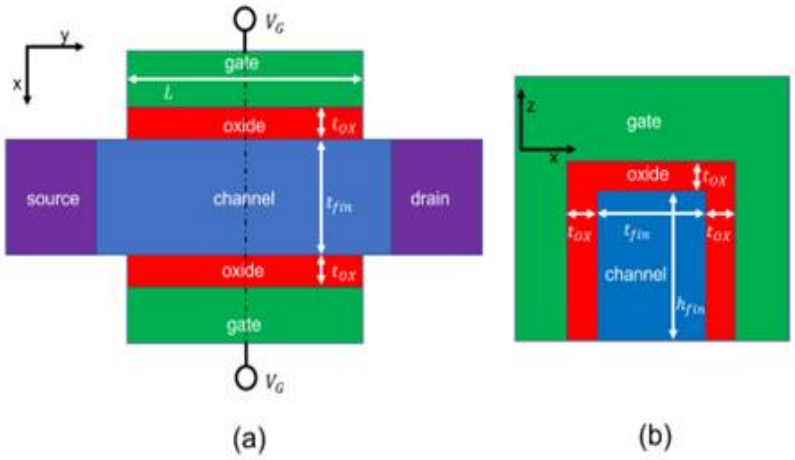

Figure 2.6. Cross sectional view of FinFET in the (a) x-y plane (along the channel) and (b) z-x plane (perpendicular to the channel). Adopted from [48]

2.6. FinFET Device Structure and Band Diagram

A FinFET's cross-section and the structure's band diagram along the x-axis in inversion are displayed in Figures 2.6 and 2.7, respectively. For the FinFET in thermal equilibrium, the one-dimensional Poisson's equation is as follows, assuming gradual channel approximation (GCA) and considering just mobile carriers (such as electrons in an NMOS FinFET):

$$\frac{\delta^2\phi(x)}{\delta x^2} = \frac{q}{\epsilon_{Si}}\left(n_i e^{\frac{q[\phi(x)-\phi_B]}{k_B T}} + N_A\right) \qquad (2.11)$$

In this case, $\phi(x)$ represents the electrostatic potential in the channel [48], q the electronic charge magnitude, ϵ_{Si} the channel's dielectric constant, n_i the intrinsic carrier concentration, k_B the Boltzmann constant, and T the temperature. N_A is the channel doping, and ϕ_B is as follows:

$$\phi_B = \frac{K_B T}{q} \ln\left(\frac{N_A}{n_i}\right) \qquad (2.12)$$

The advanced FinFET nodes ($N_A \approx 10^{13}$–10^{14}) are unintentionally dopped [49]. Transconductance, on-current, and process variance among devices are all improved as a result. Furthermore, the use of an undoped channel reduces the coupling of the channel surface potential to the body and drain of the device, improving gate control of the channel, subthreshold slope, and lowering DIBL (impact of VDS on threshold voltage).

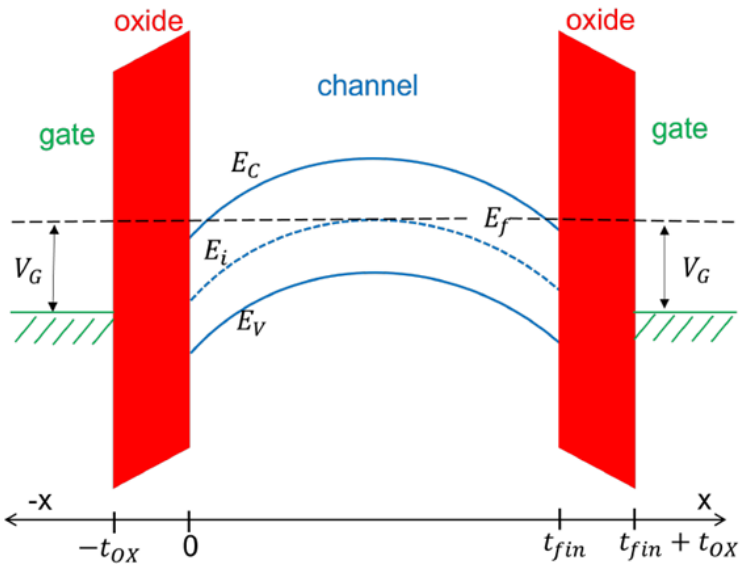

Figure 2.7. Energy band diagram of a DG FinFET device in inversion along the x direction (perpendicular to the channel) in the middle of the channel. Adopted from [48, 49]

2.6.1. Threshold Voltage

The metal-semiconductor work function difference is the primary factor determining the threshold voltage in FinFET devices [50]. However, further contributions from the conduction and valence bands splitting into sub bands due to quantum confinement in the devices also become substantial for FinFET devices with a fin width (tfin) smaller than 10 nm**.** By combining these effects and ignoring the dopants negligible contribution [51], the threshold voltage (V_t) may be written as follows:

$$V_t = \phi_{ms} + \frac{SS}{(k_B T/q)\ln(10)} \frac{0.3763}{(m_e ff/m_0) t_{fin}^2} \qquad (2.13)$$

Here, SS is the subthreshold swing, m_{eff}/m_0 is the ratio of the confined carrier's effective mass (m_{eff}) to its rest mass (m_0), and ϕ_{ms} is the gate metal work function in relation to that of intrinsic silicon.

2.6.2. Saturation Current

Because of the large lateral field induced by the applied V_{DS} along the channel, the device's drift velocity saturated as the drain-source voltage is raised above V_{DSAT}. When $V_{DS} > V_{DSAT}$ and $V_{GS} > V_t$, the device is operating in the saturation area [51]. The current may be written as follows:

$$I_{DS} = \frac{W_{eff}}{L} C_{ox} \mu_{eff}(V_{GS}, V_{DS})(V_{GS} - V_t)^{n} (1 + \lambda V_{DS}) \quad (2.14)$$

Here, λ is the channel length modulation parameter, n is a parameter that takes into consideration the degree of velocity saturation in the channel (n = 1 for a fully velocity saturated channel), and μeff (V_{GS}, V_{DS}) is the effective mobility owing to velocity saturation.

2.7. Phenomena in FinFET

2.7.1. Corner Effect

Although reducing the fin-width effectively reduces short-channel effects, there is a risk that FinFET performance will suffer. The increase in parasitic drain/source resistance is responsible for this degradation, lowering the device's drive current and transconductance [52]. The "corner effect" refers to the increased subthreshold leakage current concentration at the fin's corners as a result of the previously indicated circumstances [1, 53]. Additionally, the device's temperature increases because narrower fins make it more difficult for heat to transfer. This issue is resolved by the more rounded curved profile of FinFET manufacturing [54].

2.7.2. Quantum Effect

The electrostatic influence of the gate on the top and sides of the fin diminishes with increasing fin thickness, causing the device to behave more like a bulk MOSFET and reducing the benefits of the FinFET topology. In contrast, the density of accessible electron (or hole) states decreases in a very thin FinFET. Although energetic electrons and holes usually have a large number of "free states" at the band edges, quantum effects in extremely thin fins reduce the density of available states there [55].As a result, it takes more energy for electrons and holes to occupy states above the band edge and be free to conduct device current [1, 52].

2.8. Various Materials Used in FinFETs

2.8.1. Materials Used in FinFET Fabrication

FinFET-based Dual KK-structure, InGaAs-on-Insulator FinFET, double-gate based n-FinFET using Hafnium oxide, SOI-FinFETs, MOSFET (multi-gate), Deeply Scaled CMOS, FinFET, Selective Epitaxial Si Growth in FinFET, and Atomic Layer Deposition (ALD) in FinFET were among the materials used and examined in the study. A simulation of an n-FinFET using different gate materials, including gold, molybdenum, and aluminium, was conducted [35].

The FinFET structure's asymmetric drain extension dual-KK structure is essential for optimizing characteristics like maximum oscillation frequency (f_{max}) and cutoff frequency (f_T). One kind of spacer dielectric material utilised in the production of nanoscale devices like FinFETs is called dual-kk. Two distinct high-k dielectric materials are combined and placed on the device's source and drain sides, respectively. When comparing the asymmetric drain extension dual-KK structure to the dual-K structure, the former shows higher efficiency.

Another notable material for FinFET is In-GaAs-on-Insulator, which achieves record performance with gate lengths up to 20 nm and a widths of up to 10 nm [56, 57]. It is optimized based on the trade-off between on/off states. The use of hafnium oxide in the design and simulation of double gate n-FinFETs for 22 nm and 20 nm technologies reduces leakage current. When combined with gold gate metal, hafnium oxide, which has a high-k dielectric constant as a gate dielectric, shows a higher I_{ON}/I_{OFF} ratio than aluminium [58]. Fully depleted nMOS and pMOS FinFETs with fin widths as small as 5 nm and fin heights of 65 nm have been successfully demonstrated within the silicon-on-insulator (SOI) FinFET framework [59].

2.8.2. Gate Dielectric Material

The semiconductor industry is using high-k gate dielectrics in double-gate transistors to balance energy consumption and minimizes leakage current. With high-k dielectric materials, the multi-gate device shows promise for growth beyond bulk planar CMOS by utilising robust electrostatic control over the channel. Improvements in electrical performance, current ratio (I_{ON}/I_{OFF}), and DIBL are observed by varying the gate-lap length and adding a high-k gate insulating material to the FinFET device structure at the 10 nm technology node [60]. Notably, the HfO_2 gate oxide exhibits a high drain current, and current performance is directly affected by a drop in its k value. To increase efficiency and reduce SCEs, high-k dielectric materials must be used in FinFET devices with short channel lengths. The main goal of the industry is to build FinFETs using cutting-edge dielectric materials that lower gate leakage current, such as Al_2O_3, SiO_2, HfO_2, Si_3N_4, ZrO_2, TiO_2, Y_2O_3, Ta_2O_5, and $LaZrO_2$. The use of high-k dielectric materials mitigates difficulties and lowers power consumption even when direct tunneling occurs due to a decrease in the thickness of the gate oxide layer. Gate dielectrics are advantageous for DG FinFETs because they limit current flow across the gate, offering benefits such as increased drain current, reduced leakage current, and improved electrical characteristics when higher-quality gate dielectric materials are used.

Three distinct electrical properties of FinFETs are examined in relation to the use of various gate dielectrics. When examining V_{th} fluctuations, TiO_2 shows a higher V_{th} resulting in better performance. Furthermore, TiO_2 has a lower SS due to its high dielectric constant and reduced leakage current, as evidenced by sub-threshold swing values [61]. Additionally, TiO_2 outperforms other dielectric gate materials by 96% in controlling current flow across the gate channel, as indicated by DIBL values. When used with high-k dielectric materials, the multi-gate architecture improves electric circuit speed while reducing device-related challenges. In short-channel devices, high-k-value dielectric materials such as TiO_2 are required to lower leakage current [62, 63]. A high dielectric constant typically yields a maximum I_{on}/I_{off} ratio, which is essential for electronic signal processing and loudspeaker applications.

According to the International Technology Roadmap for Semiconductors (ITRS), $LaZrO_2$ is a state-of-the-art material with a broad energy band-gap and a high dielectric constant. It has been used in 14 nm FinFETs [62, 63]. It exhibits a better I_{on}/I_{off} ratio and lower I_{off} than SiO_2. With a high-k dielectric gate material, the device's electrostatic potential increases towards the drain terminal, increasing gate capacitance and reducing DIBL. Compared to SiO_2, the on-current increases (by 2.7), the off-current decreases (by 101), and the SS and DIBL are reduced by 10% and 76%, respectively, in high-k gate dielectrics such as $LaZrO_2$ [64]. As a gate dielectric, TiO_2 enhances threshold voltage and lessens short-channel effects, whereas HfO_2 functions as a long-lasting high-k dielectric oxide material with Leakage current is much lower than SiO_2 [65, 66]. With a higher dielectric constant than conventional SiO_2, these high-k dielectric materials offer reduced current leakage and greater heat resistance.

2.8.3. Channel Material

Studies on the performance of FinFETs with various channel materials have been carried out [1, 24]. In one study, researchers used Si, GaAs, SiGe, and SiC_3, C as channel materials to design and simulate an SOI FinFET device. The FinFET device with a silicon channel showed the maximum Ion (5.03×10^{-6} A), whereas the GaAs device had a low subthreshold swing (SS) of 58 mV/dec . Additionally, devices using SiC3C had the lowest I_{off} (7.00×10^{-19} A) and the highest I_{on}/I_{off} ratio (1.90×10^{11}) [67].

Additionally, studies have shown that using GaN and GaAs as channel materials can improve DIBL characteristics. GaN outperformed the other materials in terms of threshold voltage roll-off. GaSb was the worst material for the channel, exhibiting extremely poor short channel effect

characteristics [68, 69]. Additionally, using CNTs and graphene can decrease energy consumption, increase speed, and enhance the I_{ON}/I_{OFF} ratio [70].

2.9. Advantages of FinFET

2.9.1. Low Power Consumption

An advantage of FinFET devices is their ability to lower gate leakage current. When no externally supplied voltage is applied, the internal current in a metal oxide semiconductor (MOS) device is referred to as gate leakage current [71]. The primary causes of this current are the surface state of the semiconductor and the thermally induced migration of electrons in semiconductor materials. The manufacturing method, surface state density, and material quality are among the factors that affect the magnitude of the leakage current [72]. It is damaging for several reasons. First, it immediately increases power dissipation, which raises the circuit's static power consumption. Second, the circuit's stability and dependability may be compromised if the heat produced by this power loss raises the circuit temperature. Compared to planar devices, FinFET devices enable the use of thicker gate oxides, which significantly reduces gate leakage current, because of their ability to suppress the short-channel effect and enhance gate controllability.

2.9.2. Higher Speed

The speed at which the subthreshold swing measures a transistor switches between its on and off states. Ideally, this switch should be a binary value. This implies that the voltage should approach the saturation current when it exceeds V_t and return to zero when it falls below V_t. Any current that falls below the threshold is generally undesirable. It is recommended to cross the threshold area quickly to ensure timely gadget utilization, thereby reducing unnecessary heat generation and power waste [73]. At room temperature, the subthreshold swing (SS) limit is now 60 mV/dec, and as devices get smaller, it becomes harder to reduce it further. In a FinFET, the lower slope of the threshold also decreases and approaches the optimal value of 60 mV/dec as the silicon Fin's thickness decreases. This is because the channel's gate control ability and the short channel's blocking effect both progressively increase as the surrounding thickness decreases.

2.10. Challenges and Prospects

As the chip manufacturing process continues to shrink, FINFET devices struggle to handle sizes below 5 nanometres, and the short channel effect and leakage current have returned.

Additionally, a FinFET transistor may now have only one fin due to miniaturisation , the fins must be widened.[71, 74] After a certain height, though, it becomes challenging to keep the fins upright under internal voltage as they get taller. Constructing a FinFET structure is challenges [9]. GAAFET is the most likely method to replace FINFET. The GAAFET is a better version of the 3D FinFET. The transistor's structure has changed once more in this technology, instead of fins, the drain and gate now resemble tiny sticks that pass vertically through the gate, allowing the gate to be wrapped around the source and discharged [22].

The gate now appears as a fin, whereas the source, drain, and semiconductor also appear as fins. Thus, the concepts and implementation principles of GAAFET and 3D FinFET are quite similar [1]. The gate current control is further enhanced because the source and drain semiconductors are separated by three to four contact areas which are further subdivided into multiple four contact regions. Furthermore, this GAA architecture can address the FinFET fin pitch reduction issue as well as issues like capacitive effects which are mostly driven by gate pitch reduction. These characteristics enable the manufacturing of a process smaller than FINFET [75].

2.10.1. Structural Advancements in FinFETs

Although FinFETs push semiconductor technology beyond the 22 nm fabrication barrier and greatly reduce the short channel effects (SCE) present in conventional MOSFETs, their effectiveness decreases as manufacturing moves closer to the 5-7 nm scale. Problems include the physical limitations of the materials and the proximity of the fins, which can cause leakage to recur. Two main technological optimization paths have emerged to maintain Moore's Law and improve FinFET performance structural modifications to of FinFETs and the investigation of new constituent materials. Continuous enhancements have been pursued since the introduction of the FinFET fin-like structure. Due to restrictions in the etching process, the original FinFET geometries were slightly slanted trapezoidal forms rather than vertical fins. However, because of the through effect at the base of the fin and controllability issues, such forms posed potential dangers for large-scale integration. This led to the evolution of the FinFET design into a taller, rectangular form starting at the 14 nm node. In addition to increasing the device's drive capacity per unit area, this change lessened the effect of the bottom parasitic transistor on off-state leakage current [76]. The decrease in the number of fins per FinFET presents a significant challenge as chip manufacturing continues to shrink. Furthermore, increasing fin height has limits, as internal stress makes it difficult to maintain

vertical integrity, rendering the conventional fin structure unsuitable for advanced fabrication techniques. Building on the idea of expanding the gate-to-channel contact area for improved channel control, researchers proposed the Gate-All-Around Field-Effect Transistor (GAAFET) structure. Because of their symmetrical electric field distribution and quasi-one-dimensional ballistic transport, GAAFETs—which have gates that completely enclose the channel—offer better SCE control, lower leakage currents, and enhanced device drive capabilities. Furthermore, a depletion zone at zero gate bias is naturally forms due to the low doping concentration in the source/drain extension zones, which effectively extending the electrical gate and reducing the impact of substrate bias and SCE [9].

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Chapter 3
Cryogenic Characterization of FinFET

3.1. Introduction

The development of microelectronics has been propelled for more than 5 decades by the ongoing scaling of complementary metal-oxide-semiconductor (CMOS) technology. By reducing transistor feature sizes from the micrometre to the nanometre regime in accordance with Moore's Law [1], larger integration densities, faster speeds, and lower power consumption are now possible. But as gate lengths approach sub-20 nm [2], planar transistors face increased variability, leakage currents, and severe short-channel effects (SCEs), which limit further performance gains [3]. Advanced nodes are increasingly adopting three-dimensional device topologies, such as the Fin Field-Effect Transistor (FinFET), to overcome these difficulties.

When compared to its planar CMOS equivalents, FinFET technology offers significant improvements in transistor density, switching performance, and leakage reduction in contemporary integrated circuits [4].

Because of their exceptional scalability and manufacturability, FinFET devices manufactured at this scale serve as the basis for modern high-performance and low-power applications. For this reason, it is crucial to accurately characterized the technology under relevant conditions for specific applications. In this chapter, the DC-IV characterization of FinFETs is described, with a special focus on the temperature-dependant behaviour down to cryogenic temperatures. The structure, layout configuration, and electrical testing methods needed to assess device performance are described in this chapter. Both n-type and p-type FinFET transistors with different geometries are included in the die, enabling thorough evaluation of important parameters and the impact of cryogenic temperatures on them. Key device properties such as output conductance and transconductance, were extracted from measurements DC-IV at different temperatures.

3.2. FinFET Device Geometry

The fabricated FinFET devices have fins patterned using advanced techniques and are based on a tri-gate design. To achieve ideal gate control and low leakage, the fin pitch, height, and width are chosen for a 16-nm process design.

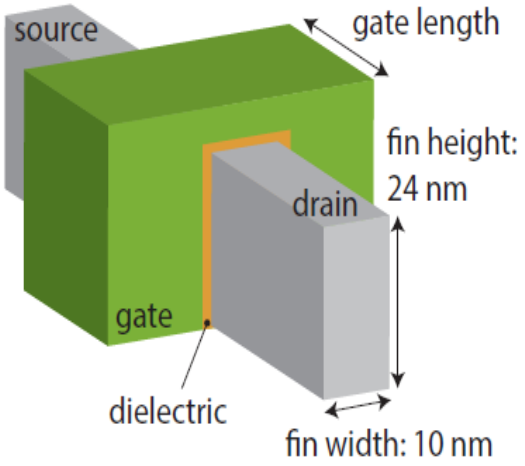

Figure 3.1. FinFET trigate adopted from [5]

Depending on the test setting and required driving current, each transistor may have numerous fins and gate fingers. Figure 3.1 illustrates the layout of the FinFET devices which have an identical "single-fin" structure with a 24 nm height and a 10 nm width, the effective width, W is 58 nm, following the definition:

$$W_{eff} = N_{fin} \times 2H_{fin} + W_{fin}$$

where N_{fin} represents how many fins each device has and H_{fin} represents the height of the fin. Through parallel replication, the number of fingers N_{finger} further scales the overall device width.

3.2.1. Device Specification and Die Structure

The manufactured die has an organized matrix of FinFET devices, both n-type and p-type, intended to investigate a wide range of electrical and physical properties across different device

geometries. While maintaining layout symmetry and electrical uniformity, the matrix design makes it easier to conduct comparative research across device geometries.

The die design's device matrix, shown in Figure 3.2, is divided into five rows and twelve columns, with 60 devices in total (30 nMOS and 30 pMOS). Each device can be characterised individually due to the dedicated pad connection. Devices with different finger numbers (1– 100), fin counts (2–20), and channel lengths (L = 16–240 nm) can all be characterised with this configuration.

In Table 3.1: The Primary Matrix Configuration is Summarised

Quantity	Value
Channel Length	16 nm – 240 nm
Device types	nMOS, pMOS
Matrix size	4 x 12
Fin number	1 - 20
Finger number	1 - 100
Differential pairs	6
Total pad count	140 (8 x 14)

3.2.2. Die Layout

The purpose of the 16 nm FinFET die was to provide an experimental platform for evaluating the electrical performance of the technologies across a variety of temperatures from 300 K down to 2.95 K. For methodical electrical characterisation, the design incorporates test structures, differential pairs, and matched nMOS and pMOS FinFETs.

The total die area is 1.5 mm × 1.7 mm. As shown in Figure 3.2, the die has 8 x 14 pads dedicated to nMOS and pMOS FinFETs, with a 55 µm pitch and 70 µm × 100 µm cell size. The pad dedicated to the gate and drain ports is shown in Figure 3.2 along with the Bulk and Source pads. Vdd and Gnd pads in figure 3.2 are used to bias the ESD protection circuit.

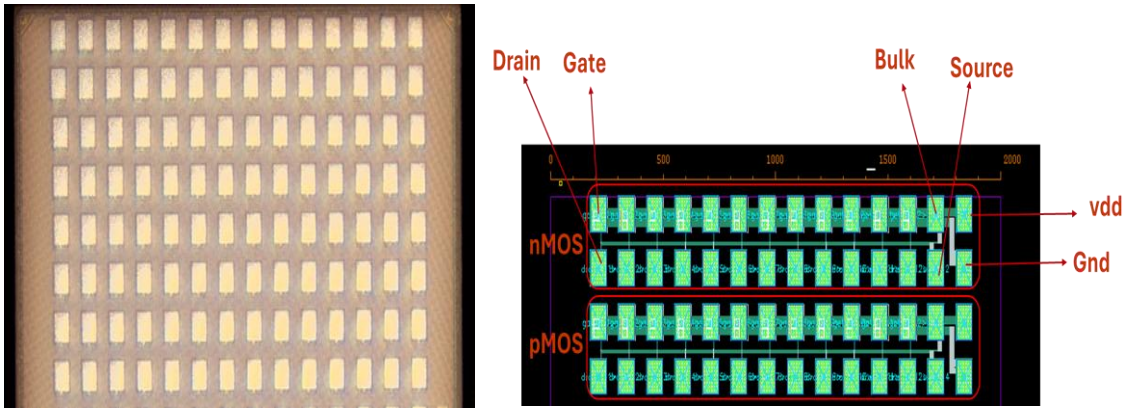

Figure 3.2. Die micrograph for 16nm FinFET test-structures (left) and layout with highlighted nMOS & pMOS pads (right).

3.3. DC IV Characterization

The transfer and output characteristics provide a general overview of how FinFETs operate at cryogenic temperatures. Key device parameters are extracted from the I–V curves, and their temperature dependence is discussed.

3.3.1. Cryogenic Measurements

The characterization of room temperature and cryogenic electrical behaviour of a commercial 16-nm CMOS FinFET technology is described in this section. FinFET technology, featuring strong quantum confinement in its ultra-thin channel, is an excellent candidate for the future implementation of the qubit itself. Measurements of the devices at cryogenic temperatures are carried out at the Advanced Quantum Architecture Laboratory (AQUA) at EPFL's School of Engineering.

3.3.2. Transfer Characteristics

For investigating the behaviour of a field-effect transistor (FET), one of the most basic electrical measurements is the drain to source current versus drain to source voltage (Ids–Vds) characteristics under DC operation. They provide information on channel modulation, carrier transport processes, and the transitions between operational regimes including the linear, saturation, and subthreshold regions. These curves are especially significant for multi-gate devices such as FinFETs because they show the efficiency of short-channel suppression at nanometre-scale dimensions and the extent of electrostatic control provided by the fin design [5]. The measured I_{ds}–V_{ds} characteristics for n-channel and p-channel FinFET devices with

different effective device widths (W) and channel lengths (L) at three different temperatures 2.95 K, 150 K, and 300 K are displayed in Figure 3.3. The n-channel FinFETs with configurations Nch_W2x1_L16, Nch_W2x1_L240 and Nch_W2x100_L240, are represented by the top three plots, while the corresponding p-channel FinFETs with the same geometric parameters are represented by the bottom three plots. For a series of gate to source /source to gate voltages (V_{GS}/V_{SG}) increased in predetermined increments, each curve shows the drain current as the drain to source voltage (V_{DS}) rises from 0 V to 1.1 V. The measurement ranges of V_{GS} and V_{SG} for N and P-channel devices respectively are reported in table 3.2 for each plots shown in figure 3.3.

Table 3.2. (a) Reported Values of V_{GS} in N Channel for Different Geometries at Different Temperatures

	Nch_W2x1_L16	**Nch _W2x1_L240**	**Nch _W2x100_L240**
T = 2.95 K	V_{GS} = 0.40 to 0.90 V	V_{GS} = 0.55 to 1.05 V	V_{GS} = 0.50 to 1.00 V
T = 150 K	V_{GS} = 0.40 to 0.90 V	V_{GS} = 0.45 to 0.95 V	V_{GS} = 0.35 to 0.85 V
T = 300 K	V_{GS} = 0.20 to 0.80 V	V_{GS} = 0.30 to 0.80 V	V_{GS} = 0.30 to 0.80 V

Table 3.2. (b) Reported Values of V_{SG} in P Channel for Different Geometries at Different Temperatures

	Pch_W2x1_L16	**Pch _W2x1_L240**	**Pch _W2x100_L240**
T = 2.95 K	V_{SG} = 0.90 to 0.40 V	V_{SG} = 1.10 to 0.60 V	V_{SG} = 1.05 to 0.55 V
T = 150 K	V_{SG} = 0.90 to 0.40 V	V_{SG} = 1.0 to 0.50 V	V_{SG} = 0.95 to 0.45 V
T = 300 K	V_{SG} = 0.80 to 0.30 V	V_{SG} = 0.80 to 0.30 V	V_{SG} = 0.80 to 0.30 V

The n-channel FinFET measured I_{ds}–V_{ds} characteristics show a temperature dependence across all gate to source biases and notable differences between the linear and saturation regions [6]. The drain to source current increases smoothly with V_{ds} at 300 K, exhibiting clearly defined saturation behaviour at higher drain voltages. The temperature sensitivity of carrier transport in the channel is demonstrated by the saturation current (I_{dsat}), which sharply drops when the temperature is dropped to 150 K and 2.95 K.

Two interrelated physical processes are the main causes of the decrease in I_{ds} with decreasing temperature: (1) decreased carrier mobility as a result of increased impurity and interface scattering dominance at low temperatures, and (2) decreased intrinsic carrier concentration in silicon, which lowers the total channel charge density for a given gate bias.

Carrier transport in the channel is dominated by phonon scattering at higher temperatures. The probability of electron-phonon interactions, which lower mobility while concurrently raising the intrinsic carrier concentration, is increased by thermal vibrations of the silicon lattice. Phonon scattering diminishes with decreasing temperature, which should improve carrier mobility. However, at cryogenic and near-cryogenic temperatures (below ~200 K), Coulomb scattering from ionised dopants and interface traps becomes the limiting factor in practical FinFET architectures, particularly those constructed with strongly doped source/drain extensions. As a result, although intrinsic phonon-limited mobility increases, freeze-out effects at the channel and contacts as well as a decrease in carrier density cause the overall current to decrease [7] . This is especially clear in the 150 K and 2.95 K plots, where the current magnitude is less across the bias range.

The saturation region of the n-channel device also exhibits a clear temperature dependence. In the saturation region, for V_{gs} above the V_{th}, the saturated current increases as temperature decreases for all geometries.

Considering varying channel lengths we can observe that, at a given temperature, the measured currents for n-channel FinFETs (W2x1 L = 16 nm) are greater than those for devices (W2x1, L = 240 nm), which is in line with expectation. Comparing different sizes of the same L, such as W2x1 and W2x100, we can observe that, for V_{gs} above the V_{th} at a given temperature, the current of the W2x1is lower than that of the W2x100, which is in line with expectations.

However, the temperature sensitivity is also more noticeable in shorter devices, where increased electrostatic coupling between the drain and channel and decreased thermionic emission make drain-induced barrier lowering (DIBL) [8] more important at low temperatures [9, 10]. On the other hand, because the greater overall conduction cross-section partially compensates for carrier freeze-out, large devices (e.g., W = 2×100 fins) [11] sustain higher drain currents even at low temperatures.

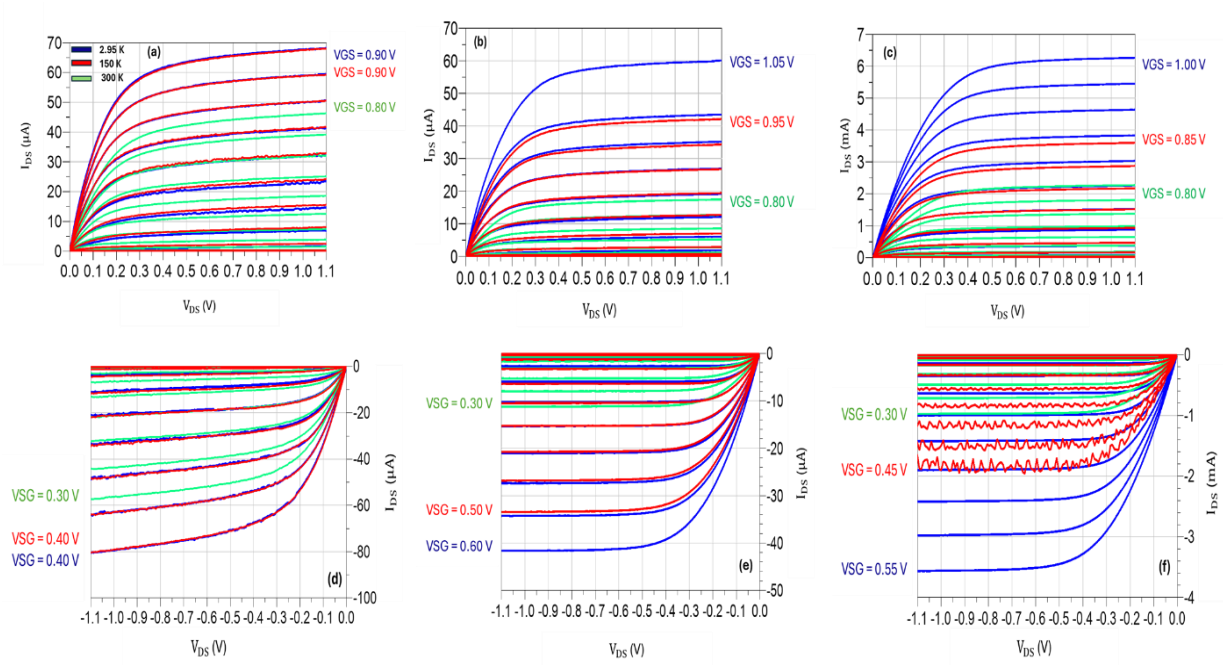

Figure 3.3. Temperature-dependent I_{DS}–V_{DS} characteristics of n-type (a) W2x1_L16 (b) W2x1_L240 (c)W2x100_L240 and p-type (d) W2x1_L16 (e) W2x1_L240 (f)W2x100_L240 FinFETs for different channel lengths (L = 16 nm, 240 nm) and effective widths. The values of V_{SG} and V_{GS} are reported in the table 3.2 (a,b) with the step size of 0.05 V. Green curves represent 300 K, red curves represent 150 K, , and blue curves represent 2.95 K measurements.

The measured p-channel FinFET characteristics, displayed in the lower set of plots in Figure 3.3, exhibit negative drain to source current that correlates with hole conduction but otherwise behaves qualitatively similarly to their n-channel counterparts. Similar to n-channel devices, in the saturation region for V_{gs} above the V_{th} , the drain to source current decreases when the temperature drops. But with p-channel devices, this decrease is usually more noticeable. This is because hole mobility is reduced and hole transport is more sensitive to temperature changes, especially when interface traps and surface roughness scattering are present. The p-channel

devices exhibit a well-developed saturation region and smooth I_{ds}–V_{ds} transitions at room temperature 300 K. The drain to source current drops and the curves become somehow “less saturated” at high drain voltages when the temperature is lowered to 2.95 K and 150 K, which are signs of increasing series resistance and decreased inversion charge density [12].

The p-channel devices exhibit a significant decrease in the slope of the linear region at low temperatures (particularly at 150 K), indicating a drop in effective hole mobility (μ_p). Even as phonon scattering decreases at low temperatures, trap-assisted conduction and carrier freeze-out become more prevalent, degrading total conduction.

Geometry has an effect that is similar, as seen in n-channel devices. The total current is smaller for long-channel devices (W2x1 L = 240 nm) with respect to devices with W2x1 and L= 16 nm, but the temperature-induced changes are more gradual, indicating less DIBL sensitivity and more stable electrostatic regulation. The proportionate scaling of total current with device width is confirmed by the broad p-channel device (W = 2×100 fins), which shows a notable rise in drain current magnitude.

All observed FinFET devices exhibit a consistent physically coherent temperature dependence when compared between the two device types. The interaction of carrier mobility, threshold voltage shift, and dopant ionisation processes is the main cause of the decrease in drain to source current with decreasing temperature.

The measured transfer characteristics (I_{ds}–V_{gs}) of n-channel and p-channel FinFET devices with varied effective widths and channel lengths (L = 16 nm and L = 240 nm) are shown in Figure 3.4. To investigate the temperature dependence of the electrical behaviour these measurements were taken at different temperatures, i.e., 150 K, 2.95 K and 300 K. For a given drain bias, each plot shows the drain to source current (I_{ds}) as a function of gate to source voltage (V_{gs}). The drain current for the n-channel FinFETs (top set of plots) rises with increasing gate voltage [13]. Fundamental semiconductor transport processes are responsible for the evident temperature dependence of transfer curves [14].

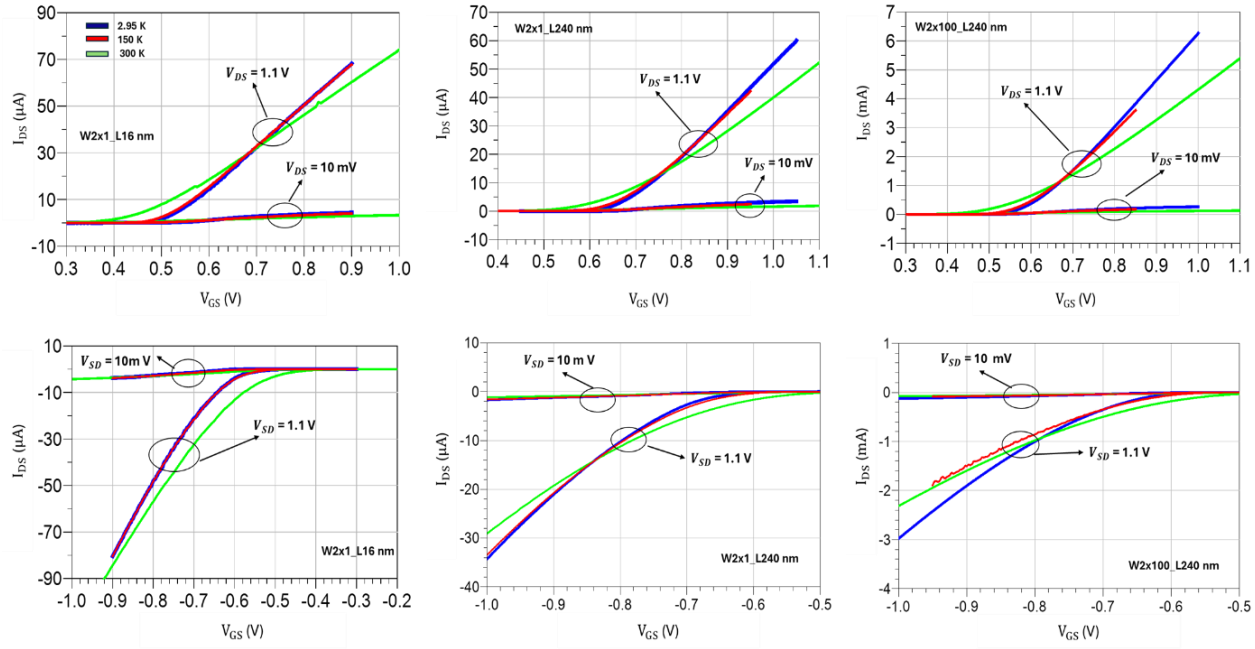

Figure 3.4. I_{DS}–V_{GS} characteristics for multiple n-channel (top row) and p-channel (bottom row) FinFET devices with channel lengths of 16 nm and 240 nm, measured at V_{DS} = 10 mV and 1.1 V for n-channel and at V_{SD} = 10 mV and 1.1 V for p-channel.

As the temperature drops, the threshold voltage (V_{th}) of the n-channel devices exhibits a little positive shift. This is a common behaviour driven by the decrease in the intrinsic carrier concentration and the resulting rise in the surface potential required to induce inversion [15]. Despite improved gate control, the on-current (I_{on}) falls at lower temperatures. This can be explained by decreased carrier mobility, which is dominated by impurity and surface roughness scattering in the cryogenic region [16]. Additionally, there is a discernible difference in I_{ds} between short-channel and long-channel devices. This is caused by the shorter gate-length devices higher gate coupling, increased electric field in the channel, and decreased channel resistance [17].

In comparison with n-channel devices, the p-channel FinFETs transfer characteristics (bottom set of plots in Figure 3.4) show the expected mirror symmetry, with hole conduction represented by negative drain to source current. In saturation region, for V_{gs} above V_{th}, the drain to source current decreases (increases in magnitude) for a given gate to source voltage when the temperature drops from 300 K to 150 K. As the temperature drops, the p-FinFETs threshold voltage shifts slightly towards more negative gate voltages, which is consistent with a decrease in the intrinsic carrier density and a shift in the precise position of the Fermi level within the silicon bandgap [18]. Similar to n-type devices, for given W2x1 device, shorter

channel lengths (L = 16 nm) provide higher (in magnitude) I_{ds} than longer channel lengths (L= 240 nm).

The geometry-dependent comparison of L = 16 nm and L = 240 nm devices shows that longer devices have superior subthreshold control and lower DIBL[19].In contrast shorter FinFETs offer larger drive currents, but are more susceptible to short-channel effects [7, 20].

3.3.3. Output Conductance

The output conductance is defined as $g_{ds} = \partial I_{ds}/\partial V_{ds} \mid_{vgs=constant}$ and drain to source current–drain to source voltage (I_{ds}–V_{ds}) characteristics for three n-channel FinFET devices were measured at the temperatures of 2.95 K, 150 K, and 300 K with a fixed gate bias of V_{gs} = 0.8 V. Since these results are based on measurements rather than simulations, they accurately capture the intrinsic electrical behaviour of the fabricated devices both at cryogenic and room-temperature conditions [21].

The I_{ds}-V_{ds} plots shown in Figure 3.5 demonstrate the expected shift from a linear (ohmic) region at low drain voltage to a saturation region at higher drain to source voltage across all device geometries. The channel pinch-off and velocity-saturation phenomena characteristic of nanoscale FinFETs cause the drain to source current to increase monotonically with V_{ds} and eventually reach a saturation peak [22]. The lowest current among the three temperature conditions occurs at 300 K because of increased carrier dispersion and resistance due to larger lattice vibrations. The I_{ds} increases with decreasing temperature up to about 150 K. Below 150 K the I_{ds} remains stable at the same value. These indicate that below a certain temperature the I_d-V_d characteristics do not exhibit big changes. These trends remain across all three device geometries, indicating that temperature plays a major role in controlling conduction in scaled FinFETs.

The spacing between the temperature-dependent curves is constant regardless of absolute values, confirming that the underlying physical mechanisms scale proportionately with geometry [23].

The output conductance (g_{ds}) directly reflects the trends observed in the I_{ds}–V_{ds} plot. At very low drain to source voltages, g_{ds} has a large initial value in all devices, corresponding to the

linear region where I_d increases sharply with V_d. The shift towards saturation, when the channel becomes pinched off and I_{ds} becomes more insensitive to V_{ds}, is shown by the rapid decrease in g_{ds} as V_{ds} increases. Strong saturation behaviour and good channel-length modulation characteristics are indicated by g_{ds} approaching values close to zero at large V_{ds} (usually beyond 0.4–0.5 V), as shown in Figure 3.5.

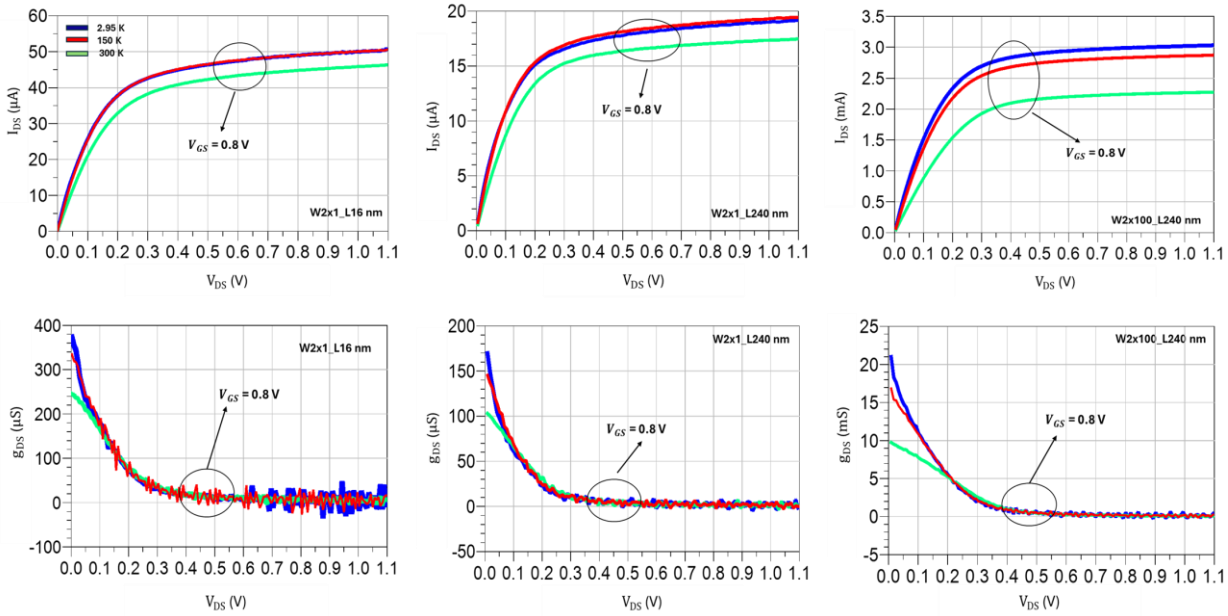

Figure 3.5. I_{DS} –V_{DS} characteristics of n-channel FinFET devices(top row) with different channel lengths (L = 16 nm and L = 240 nm) and effective widths (W2×1 and W2×100), measured at a fixed gate to source voltage of V_{GS} = 0.8 V. The corresponding output conductance (g_{DS}) plots (bottom row), extracted from the same I_{DS} –V_{DS} data, are shown below for each device geometry.

The magnitude of g_{ds} is greatly affected by temperature. Due to significantly increased mobility and decreased series resistance, which raises the initial slope of I_{ds}–V_{ds}, the conductance peak around V_{ds} = 0 V is maximum at 2.95 K. The g_{ds} values at all temperatures converge as V_{ds} approaches the saturation region, suggesting that cryogenic conditions mainly impact the linear region and have less of an impact on saturated transport [24]. g_{ds} falls between the low-temperature and room-temperature values. Higher phonon scattering at 300 K causes the initial slope of I_{ds} against V_{ds} to decrease, resulting in the lowest g_{ds} peak and a more progressive decrease.

The longer-channel device has lower conductance than the short-channel device due to its reduced sensitivity to shifts in the electric field along the channel, whereas the short-channel

device exhibits the greatest g_{ds} values because of its greater sensitivity to changes in V_{ds} [25]. While the same temperature-dependent trends continue, the broad W = 2 × 100 device, which has a considerably greater driving current, shows g_{ds} in the milli siemens range. All devices exhibit extremely low saturation g_{ds}, indicating little channel-length modulation across temperatures and good channel control.

It is evident from the combined I_{ds}–V_{ds} and g_{ds} data that the conduction behaviour of FinFET devices is simultaneously determined by temperature and geometry. Room-temperature operation decreases mobility and decreases both values, cryogenic temperatures improve mobility and increase both the drain to source current and the first output conductance [26]. Strong electrostatic integrity is demonstrated by the fact that all devices converge to low output conductance in the saturation region despite these variances.

The p-channel FinFET devices measured output characteristics (I_{ds} –V_{ds}) with a fixed gate bias of V_{SG} = 0.7 V were acquired at three different temperatures and are shown in Figure 3.6. When the devices reach the channel pinch-off, the drain to source current saturates after initially increasing approximately linearly in the low V_{ds} region. Owing to enhanced carrier mobility and reduced series resistance, the largest drain to source current is observed at 300 K. As the temperature is reduced to 150 K and then to 2.95 K, the on-current decreases significantly. Although phonon scattering is suppressed at lower temperatures, Coulomb and impurity scattering, together with interface trap effects and possible dopant freeze-out, become dominant at cryogenic temperatures, leading to an overall degradation of carrier mobility. This behaviour contrasts with that typically observed in n-channel devices, where reduced phonon scattering often results in enhanced low-temperature performance. The near-linear region's I_{ds}–V_{ds} characteristic is flatter and more resistive as a result of the reduction in thermally activated carriers at low temperatures, which also reduces subsurface leakage.

The devices shape also influences the magnitude of the drain to source current. Devices with a wider effective fin width (e.g., W = 2×100 nm) generate greater absolute current levels, but structures with a longer channel length (e.g., L = 240 nm) exhibit lower current due to increased channel resistance.

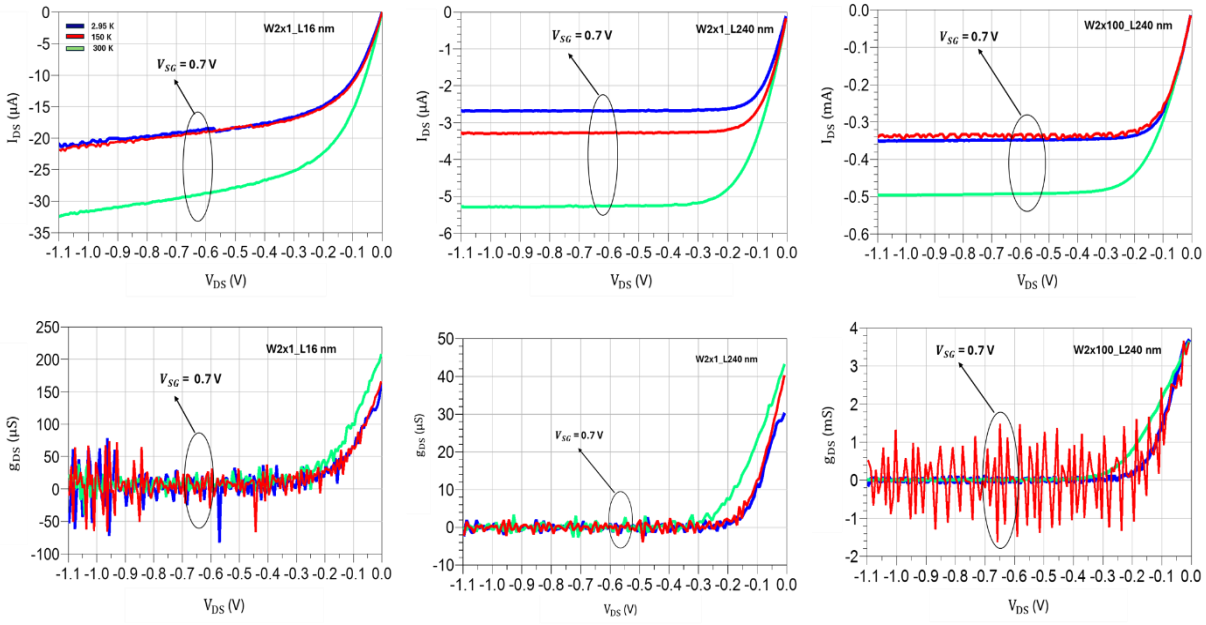

Figure 3.6. Drain to source current versus drain to source voltage (I_{DS} –V_{DS}) for three p - channel FinFET geometries (top row)at a fixed source to gate bias of 0.7 V. The lower row shows the corresponding output conductance (g_{DS})(bottom row) as a function of drain to source voltage for each device.

All devices exhibit the same monotonic trend [27] of decreasing current with decreasing temperature, even with geometrical variation. The low-temperature curves show a more sudden increase in drain to source current in the high-V_{ds} region as shown in Figure 3.6 (W2x1_L240, W2x100_L240), which is compatible with less carrier scattering and an earlier start of velocity-saturation-dominated conduction.

The extracted output conductance g_{ds} further emphasises the effects of temperature. In the saturation region the g_{ds} is close to zero and increases progressively with increased drain bias [22]. The measured conductance exhibits greater degrees of oscillations at cryogenic temperatures, particularly at low V_{ds}. Increased sensitivity to interface traps, carrier freeze-out occurrences, and quantisation effects which become important around 150 K and especially at 2.95 K are the causes of these oscillations [28, 29]. For all geometries, g_{ds} increases with V_{ds}, indicating the rapid increase in drain current in the high-field regime. Because of better channel management and less drain-induced barrier lowering (DIBL), devices with longer channels have lower conductance. On the other hand, because of their greater effective conduction cross-section, larger devices exhibit higher g_{ds} [30].

Measurements show that P-channel FinFETs exhibit cryogenic transport behaviour, with lower drain to source current, higher low-bias resistance, and more dramatic output-conductance swings at low temperatures.

3.3.4. Transconductance

At a constant drain to source voltage of V_{DS} = 1.1 V the observed transconductance $g_m = \partial I_{ds}/\partial V_{gs} \mid_{Vds=constant}$ vs gate to source voltage (V_{gs}) characteristics provide important insight into the temperature-dependent carrier transport processes [31] within the manufactured n-channel and p-channel FinFETs. The comparison charts at 2.95 K, 150 K, and 300 K indicate how carrier mobility, threshold voltage V_{th} and thermal effects interact.

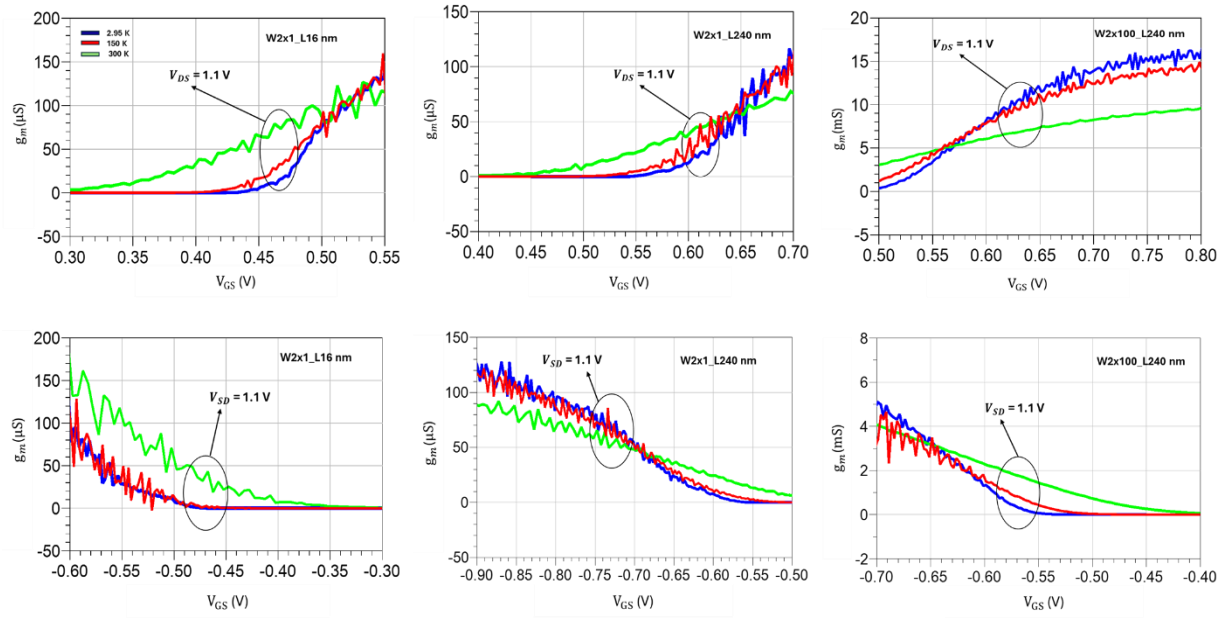

Figure 3.7. Transconductance (gm) characteristics of n-channel at V_{DS} = 1.1 V (top row) and p-channel at V_{SD} = 1.1 V (bottom row) FinFET devices with different geometries.

The curve at 150 K which begins conduction at a higher V_{gs} shows that cooling to 150 K causes a constant positive shift in the threshold voltage for the n-channel devices. The temperature dependence of the Fermi level and the intrinsic carrier concentration, which require a larger gate field to reach the threshold inversion charge density, are the main causes of the estimated V_{th} increase at cryogenic temperatures. More importantly, the measurements performed at 150 K show a considerable increase in the g_m peak. This enhancement results directly from the substantial reduction in phonon scattering (lattice vibrations) at low temperatures, which increases electron mobility. This impact is particularly apparent in the high-current Nch_W2x100_L240 device, where the 150 K curve shows a steeper slope and a greater peak,

both of which indicate improved carrier transport efficiency. A "crossover" is seen at high gate voltages in the Nch_W2x1 devices, where the 150 K and 2.95 K transconductance drops above the value at room temperature. This implies that the low-temperature mobility advantage is mitigated when other scattering processes, including surface roughness scattering, become prominent at high vertical electric fields (strong inversion), even as phonon scattering is decreases [32].

On the other side, at cryogenic temperatures, the p-channel devices show an even more obvious and apparent performance improvement. The p-channel equivalent of the V_{th} shift seen in the n-channel devices, the threshold voltage for p-channel devices moves to a less positive V_{gs} (a more negative V_{th} magnitude). The striking rise in peak transconductance at 150 K for all observed p-channel geometries is the main finding.

3.4. Comparative Analysis of Long and Short Devices at Ambient and Cryogenic Temperature

Fundamental variations resulting from device scaling are revealed by the electrical characteristics of the short-channel (W2x1_L16) and long-channel (W2x1_L240) FinFETs for both n- and p-channel devices at 300 K [33]. The I_{ds}–V_{ds} characteristics show that, in comparison to their long-channel counterparts, the short-channel devices generate substantially higher drain to source current across all gate to source voltages. The shorter channel length, which decreases the effective channel resistance and forces the carrier transport towards the velocity-saturation region even at comparatively low drain to source voltages, is the main cause of this increase [34]. Increased current levels arise from carriers reaching their saturation velocity significantly earlier as the electric field within the short channel grows rapidly with applied V_{ds}. The long-channel devices, on the various side, function primarily under classical drift-diffusion transport, and the reduced electric field distribution throughout the channel restricts the current, resulting in significantly lower I_d values.

The two devices saturation behaviours also show a substantial difference in the saturation region. Strong channel-length modulation (CLM), brought about by the drain depletion region intruding into the channel as V_{ds} increases and thereby shortening the channel length, is shown by this slow increase in current. As a result, the output conductance of the short-channel devices is larger than that of the long-channel devices, whose I_{ds}–V_{ds} curves saturate more effectively with less dependency on V_{ds}. Because of the strong electric-field coupling at nanoscale

geometries, the shorter devices significantly diverge from the ideal square-law behaviour associated with standard MOSFET performance, whereas the long-channel devices maintain characteristics closer to it.

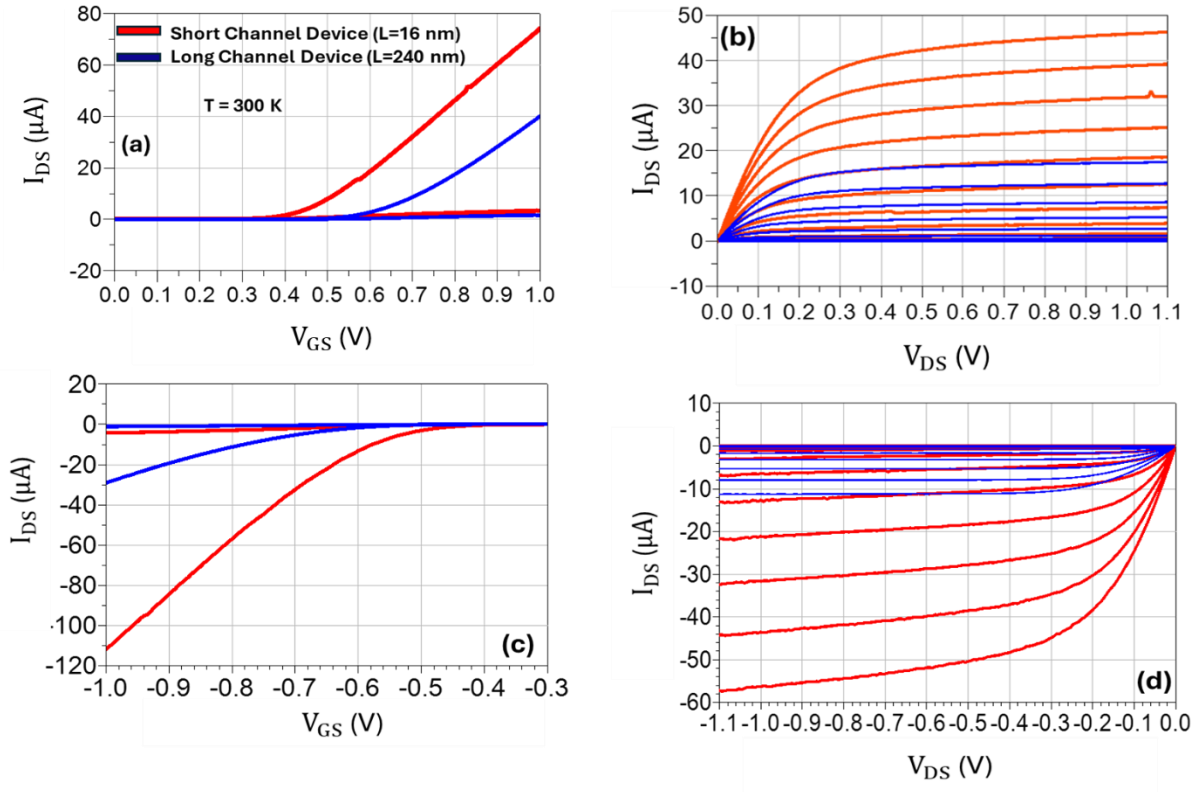

Figure 3.8. I_{DS} - V_{DS} and I_{DS} – V_{GS} characteristics of n-channel (a, b) and p-channel (c, d) FinFET devices measured at 300 K. These plots highlight the impact of channel length on drain current.

The two channel lengths are further distinguished by drain-induced barrier lowering (DIBL) [35]. Even at low gate to source voltages, the drain potential in short-channel devices greatly affects the channel barrier profile by raising the drain to source current and decreasing the energy barrier at the source end [36]. The compression of the I_{ds}–V_{ds} curves at low V_{gs} values for the L = 16 nm devices shows this effect, indicating that the drain has a significant electrostatic impact on the channel [37]. Long-channel devices, on the other hand, exhibit low DIBL because the gate maintains dominant control over the channel potential, limiting unnecessary drain-driven modulation. Although the absolute current levels vary because of the reduced hole mobility, the same patterns are also seen in p-channel devices [38]. However, the p-MOSFETs behave similarly, with short-channel models exhibiting larger drain to source current magnitude, stronger CLM, and more sensitivity to the drain field [39, 40].

Further understanding of the scaling-induced impact is offered by the I_{ds}–V_{gs} characteristics. Because of increased field-driven transport, the short-channel devices exhibit greater on-state current, validating the improved current-driving performance expected from extreme channel-length reduction. [35]. As a result, the subthreshold characteristics degrade, and the slope becomes less steep. The long-channel devices show a more consistent threshold voltage as compared to short channel devices, indicating better gate control across the whole channel region. Their subthreshold region continues to have a greater slope, which is consistent with the drain having less of an impact on the occurrence of channel barriers.

Similar trends are seen in the I_{ds}–V_{gs} responses of p-channel devices as shown in figure 3.8 (c, d). The short p-channel devices exhibit a marked increase in drain to source current magnitude and a worsened subthreshold slope, indicating that short-channel effects are structurally present in both carrier polarities and are not exclusive to n-channel operation. The long p-channel devices behave considerably more in line with theory, maintaining improved electrostatic control, decreased DIBL, and lower off-state current [41].

The conventional trade-off in FinFET scaling is demonstrated by an experimental comparison of long- and short-channel devices. Reducing the channel length causes non-ideal behaviours including greater CLM, stronger DIBL, threshold-voltage roll-off and decreased subthreshold slope, even as it also significantly increases drive current and improves switching performance. Figure 3.9 shows a comparison at 2.95 K. The channel mobility approaches its ballistic limit at 2.95 K due to the significant reduction of phonon scattering. In these circumstances, the longer device continues to show a more linear and classical drift-diffusion-like increase in I_{ds} with V_{ds}, whereas the short-channel device shows more abrupt current saturation, indicating the onset of velocity saturation or quasi-ballistic transport much earlier [42]. The output characteristics of the short-channel n-device are highly sensitive to gate overdrive as a result, increasing V_{gs} produces a progressively larger separation between the corresponding drain to source current curves showing significant transconductance even in the cryogenic domain.

Similar characteristics are observed for the p-channel devices studied under the same conditions, although the V_{ds} dependency and absolute current magnitudes vary because of the higher carrier freeze-out effects at cryogenic temperatures and the intrinsically lower mobility of holes [43]. The enhanced curvature at low drain voltage suggests stronger tunnelling

contributions or contact-limited behaviour as shown in figure 3.9 (d), The short-channel p- device again delivers significantly higher magnitude drain to source currents. The short-channel device exhibits early saturation and a more nonlinear onset of conduction in contrast to the long-channel p-device, which displays an increasing almost perfect saturation region. This behaviour reveals that short-channel effects are magnified by cryogenic operation because of decreased thermal energy and diffusion currents, giving the electrostatic integrity of the short device even more essential [44].

The I_{ds}-V_{gs} curves slope at 2.95 K, which also indicates the approach to quantum-limited switching behaviour and a reduced impact of thermally induced scattering [45, 46]. In the meantime, the long-channel device retains a slower and smoother turn-on, which is indicative of drift-dominated transport and less susceptible to drain-induced barrier modulation. Similar trends can be seen in the p-channel transfer curve, the long-channel device shows more consistent and standard FinFET behaviour, whereas the short-channel device shows greater on-state current and more visible gate sensitivity. This is consistent with drain-induced barrier lowering (DIBL), which is made less effective at nanoscale channel lengths by increased electrostatic coupling between the drain and channel.

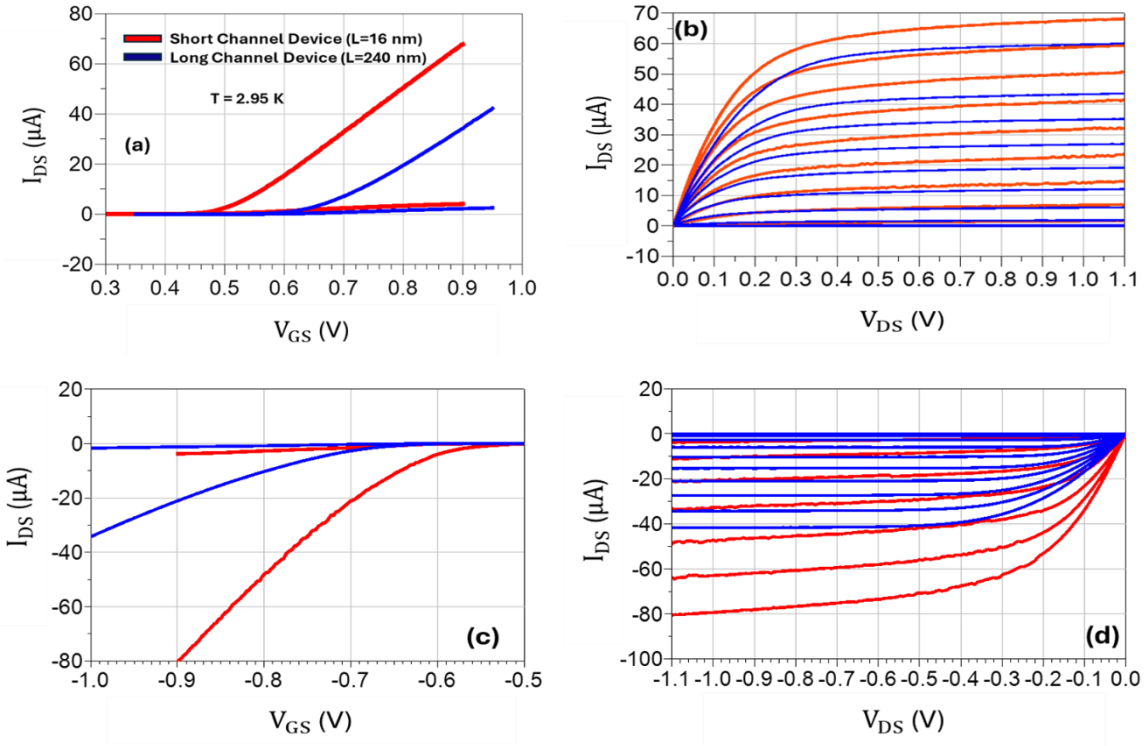

Figure 3.9. I_{DS} - V_{DS} and I_{DS} – V_{GS} characteristics of n-channel (a, b) and p-channel (c, d) FinFET devices measured at 2.95 K

High-speed cryogenic electronics benefit from short-channel devices with greater on-current, steeper switching slopes, and stronger gate control. However, they also experience higher drain-induced barrier lowering, early saturation, and threshold voltage decrease due to enhanced short-channel effects. Long-channel devices exhibit more stable and predictable behaviour with less susceptibility to drain bias and less short-channel effects, although having lower power currents.

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Chapter 4
Compact Modeling and Model Validation

In this chapter is described a new empirical formulation for modelling the DC drain-current behaviour of CMOS technology devices oriented to quantum computing application. The proposed model is based on the well-known Angelov's model, that has been properly modified to include the capability of reproducing the transistor DC I-V characteristics from ambient down to cryogenic temperature. The approach has been successfully applied to 16-nm FinFET technology, showing very good performance in terms of model accuracy.

The main target of the proposed model is to provide designers with a design tool complementary to the foundry PDK, helping them to predict the transistor performance at cryogenic temperatures and accounting for it during the design of integrated circuits.

Angelov's model offers a simpler formulation compared to commonly used models for CMOS technologies (e.g., BSIM), which rely on physical parameters. Moreover, its parameters can be quickly extracted from a few measurements under the operating conditions of interest [1] ensuring excellent accuracy. Another advantage is that it can be easily extended to model the nonlinear dynamic behaviour of the transistors at microwave frequencies in cryogenic conditions by using, for example, measured S-parameters at different cryogenic temperatures.

4.1. Compact Modeling

Compact modeling provides simplified, accurate mathematical descriptions of semiconductor devices for use in circuit simulation and integrated circuit (IC) design [2, 3]. By allowing circuit simulators to predict device behaviour under different operating conditions, based on technology-dependent characteristics acquired from a specific manufacturing process, these models serve as the foundation of computer-aided design (CAD) tools [4, 5].

As metal-oxide-semiconductor field-effect transistor (MOSFET) technology has evolved, also been the development of small variants [6, 7]. Early MOSFET compact models were mainly developed to describe the static and low-frequency I–V behaviour of devices operating in strong inversion. This level of precision was adequate at the time to satisfy industrial design specifications. However, contemporary CMOS technology [8] allows operating frequencies up

to the tens of GHz and functions in mild, moderate, and severe inversion regions. Because of this, modern compact models need to properly represent device behaviour over a significantly wider range of bias and performance.

Compact models are an essential part of the process design kit (PDK) in today's IC design environment [9], serving as the primary interface between circuit designers and device engineers [10]. Compact models that account for geometry, bias, temperature, DC, AC, radio-frequency, and noise effects must be both computationally efficient and physically predictive as device dimensions continue to scale into the nanometre [11-13].

Based on the physical quantity used to characterize the device behaviour, contemporary MOSFET compact models are often divided into three main modelling approaches: I-V based models, surface potential based models, and charge based models [14]**.** Because I-V models are empirical, flexible, and simple to use, they have historically dominated industrial applications. Surface-potential-based and charge-based models, on the other hand, were initially more common in academic and research environments and emphasize physical accuracy with fewer empirical factors.

Physics-based compact models have been increasingly popular in industry in recent years due to improvements in their maturity, accuracy, and flexibility [15]. This change has enabled for these models to maintain excellent predictive performance for cutting-edge technologies while supporting state-of-the-art IC design needs [16, 17].

By combining a core model with extra sub-models that take real-device effects into account, compact device models precisely describe the terminal I–V behaviour of devices [18]. The core model, which constitutes a very tiny amount of the total model code for MOSFETs [19], describes the ideal large-device I–V characteristics of a target technology. Short-channel effects, output conductance, quantum mechanical processes, nonuniform doping, gate leakage, band-to-band tunnelling, noise, non-quasistatic effects, intrinsic input resistance, and strain are among the non-ideal factors included in the model implementation [20, 21].

Compact models act as a connection between process development and circuit design within the larger technology CAD (TCAD) framework [22]. Through reverse modelling approaches,

they not only make realistic circuit simulation but also help assess manufacturing feasibility and guide the fabrication of next-generation integrated circuits [23].

4.2. Introduction of BSIM

One of the most popular compact transistor models designed to solve the difficulties of modelling nanoscale MOSFETs is the Berkeley Short-channel IGFET Model (BSIM) [24]. BSIM, developed at the University of California, Berkeley, provides a comprehensive, physically based description of MOSFET behaviour across various operating regions, including cutoff, linear, and saturation modes. In contrast to earlier models, BSIM includes comprehensive formulations of charge conservation, electrostatics, and carrier transport, allowing accurate modelling of both DC and AC properties across a broad range of bias conditions and geometries [25, 26].

The BSIM architecture has changed throughout the years to reflect advancements in semiconductor technology. For many years, early versions like BSIM3, tailored for deep-submicron planar CMOS technologies, became the industry standard [27]. BSIM4 was created to offer improved precision and scalability by further device scaling, the addition of metal gates, strain engineering, and high-k gate dielectrics [28]. BSIM4 is suitable for complex CMOS nodes due to its enhanced modelling of short-channel effects, gate leakage currents, non-quasi-static effects, noise behaviour, and temperature dependency. More recently, multi-gate devices like FinFETs [29] and gate-all-around transistors have been supported by extensions like BSIM-CMG [30].

The BSIM model's brief and physics-based formulation, which enables effective implementation in circuit simulators [31] while retaining high accuracy, is one of its primary advantages [11]. Technology characterization is made easier and meaningful parameter extraction from measured data is made possible by the strong relationship between model parameters and physical device attributes. Because BSIM maintains a compromise between computational efficiency and physical rigour, it is widely used as a standard MOSFET model in industrial design [32] processes and electronic design automation (EDA) tools. The main drawback of extracting a custom BSIM model is that accurate knowledge of physical parameters is required to achieve accurate predictions.

Reliable analog, RF, and mixed-signal design is made possible by the BSIM model, which is essential in circuit-level modelling environments like ADS [14, 33]. Through exact modelling of transistor nonlinearities, capacitances, and high-frequency behaviour with precision, BSIM enables researchers and designers to assess circuit performance under practical operating conditions. As a result, using the BSIM model in simulation-based research [34] ensures adherence to industry standards and increases the reliability of design and analysis findings reported in scientific studies [35].

In this work, starting from the DC IV measurement reported in the previous Chapter, a BSIM compact model was extracted for the 16-nm FinFET. A simplified set of parameters is shown in Table 4.1. To reduce the difference between the simulated and measured drain current under various bias parameters, including output and transfer characteristics, the parameter extraction procedure was carried out by means of numerical optimization procedure implemented directly in ADS. Figure 4.1 shows the comparison between the measurements and the model after the numerical optimization of the parameters.

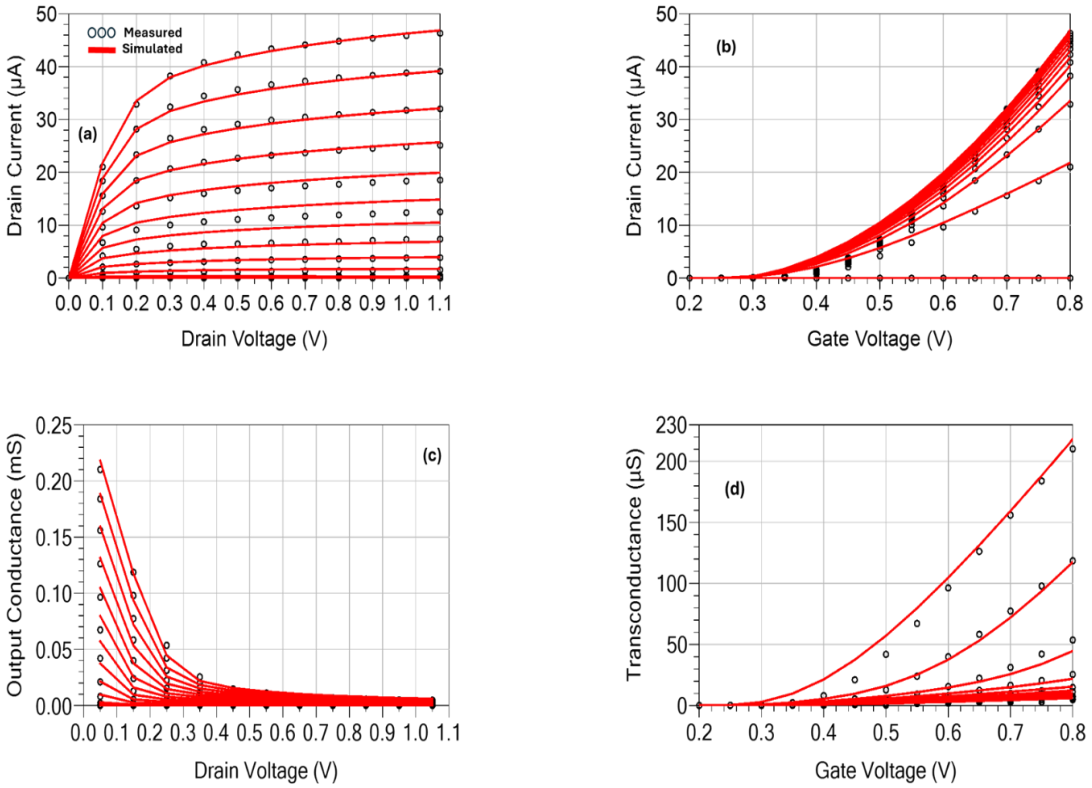


Figure 4.1. Measured (symbols) and BSIM simulated (lines) DC and small-signal characteristics of the W2x1_L16nm FinFET: (a) output characteristics, (b) transfer characteristics, (c) output conductance, and (d) transconductance.

Table 4.1: Parameters of Optimized BSIM Model

Parameters	Description	Values	Unit
μ_0	Mobility	403	$cm^2/V.s$
U_A	First-order mobility degradation coefficient	7.66	m/V
U_B	Second-order mobility degradation	7.29	$(m/V)^2$
V_{th0}	Threshold voltage	*0.38*	V
VSAT	Saturation velocity	100	m/s
A_0	Bulk charge effect coefficient for channel length	2.91	Dimensionless
K1	First order body effect coefficient	1.60	$V^{1/2}$
K2	Second order body effect coefficient	0.51	Dimensionless
K3	Narrow width coefficient	69.73	Dimensionless
K_{ETA}	Body-bias coefficient of the bulk charge effect	1.40	1/V
R_{sh}	Parasitic resistance	1.21	Ω^{-2}
Toxm	Nominal Tox	2.28	m
W_{INT}	Width offset from fitting parameter without bias effect	-9.20	m
L INT	Length offset fitting parameter without bias effect	0.06	m
D WG	Coefficient of W_{eff}'s gate dependence	-0.49	m/V
D WB	Coefficient of W_{eff}'s body bias dependence	-1.70	$m/V^{1/2}$
Tox	Gate oxide thickness	1.94	m
N_{FACTOR}	Subthreshold swing factor	0.60	Dimensionless
ETA0	*DIBL* coefficient in subthreshold region	3.56	Dimensionless
E TAB	Body-bias coefficient for the sub-threshold *DIBL* effect	0.23	1/V
P_{CLM}	Channel length modulation parameter	2.65	Dimensionless

As it can be seen, the model is able to accurately reproduce the DC IV behaviour. The shift from the linear to the saturation region is accurately captured by the simulated output characteristics, which almost match the measured data across the whole drain voltage range, as shown in Figure 4.1(a). This shows that the model accurately captures carrier transport, velocity saturation, and channel modulation effects. The accuracy of the determined parameters is further demonstrated by the transfer characteristics in Figure 4.1(b), especially in the strong inversion region where the model matches the nonlinear rise of drain current with gate voltage.

The simulated and measured output conductance as a function of drain voltage is shown in Figure 4.1(c), where it can be seen that the model accurately captures the decreasing trend with increasing drain bias, showing an adequate representation of channel-length modulation and drain-induced effects. The transconductance against gate voltage, at fixed drain bias of V_{ds} = 1.1 V, is displayed in Figure 4.1(d), where the simulated results closely match the measured data, showing correct mobility and gate-control related parameter extraction. Non-ideal phenomena such as interface trap states, changes in contact resistance, and limitations of the BSIM formulation in the subthreshold region might be responsible for minor deviations observed at low drain voltages and near the threshold [36].

4.3. Angelov's Model

Angelov's model [37] is one of the efficient compact models for active devices in microwave electronics. The Angelov's model is an empirical large-signal transistor model that was first created to correctly describe the nonlinear behaviour of field-effect transistors (FETs), particularly MESFETs and HEMTs, in high-frequency and high-power applications [38]. The model's ability to properly and effectively show the change from linear operation to current saturation can be very useful for power amplifier design [39]. The Angelov's model uses hyperbolic tangent functions to represent the behaviour of the drain current vs the drain and gate voltages, ensuring smooth derivatives and enhanced numerical stability during harmonic balance simulations. This mathematical framework accurately captures gain compression, soft saturation, and bias-dependent nonlinearities.

The construction of the drain current as a function of an effective gate voltage, expressed as a nonlinear expansion around the threshold voltage, is a fundamental characteristic of Angelov's model [40]. This method offers more flexibility in fitting observed DC IV characteristics across a variety of operational regions, including saturation, linear, and subthreshold regions. The

Angelov's model [41] allows for accurate fitting of experimental I–V data while preserving continuity and smoothness throughout every region of operation by employing a set of coefficients that regulate the slope, curvature, and higher-order nonlinear effects [42].

To accurately simulate the device's dynamic response at microwave frequencies, Angelov's model includes nonlinear charge models. Accurate S-parameter prediction, load-pull behaviour, and large-signal performance measures including output power, efficiency, and adjacent channel power ratio (ACPR) depend on charge equations [43, 44].

The Angelov's model is frequently used as a common nonlinear device model for circuit design in commercial electronic design automation (EDA) tools, such as Advanced Design System (ADS) [45]. Because it finds a good balance between modelling accuracy, computational efficiency, and parameter extraction complexity, it is quite popular [46]. Despite its empirical origins, the model's structure represents important physical device behaviours, making it appropriate for both academic study and design-oriented simulations [13]. The Angelov's model remains a reliable modelling technique for large-signal RF simulation in both industry and research. It has been widely applied in the analysis and design of microwave power amplifiers, nonlinear circuit blocks, and high-frequency systems.

4.3.1. Drain Current Formulation

The mathematical formulation adopted in this work is based on the empirical description proposed by Angelov, which has been simplified with respect to its original expression [41], as reported in equations (4.1) and (4.2):

$$I_D = I_{pk0}[1 + \tanh(\psi)]\tanh(\alpha V_D)\,(1 + \lambda V_D) \qquad (4.1)$$

$$\psi = P_1\big(V_G - V_{pks}\big) + P_2\big(V_G - V_{pks}\big)^2 + P_3\big(V_G - V_{pks}\big)^3 \qquad (4.2)$$

where V_G and V_D are the gate-source and the gate-drain voltages respectively, whereas I_{pk0}, α, λ, P_1, P_2, P_3, and V_{pks} are parameters to be identified. The general expression of ψ is a polynomial expansion, usually of the 3rd order, that can be further expanded to improve accuracy although increasing the model complexity. Here, to keep the model as simple as possible, the 2nd order term has been omitted, as it did not provide any significant improvement in model accuracy during the identification phase. The reduced equation (4.2) can be rewritten as:

$$\psi = P_1\left(V_G - V_{pks}\right) + P_3\left(V_G - V_{pks}\right)^3 \qquad (4.3)$$

Table 4.2: Parameters of Angelov's Model

Parameters	Description	Unit	Values
I_{pk0}	Current scaling factor	A	32.28
λ	Transition steepness	1/V	0.21
α	Gate related voltage	1/V	5.96
V_{pks}	Shift voltage	V	0.74
P_1	Threshold voltage	1/V	3.55
P_2	Threshold voltage	$1/V^2$	0.50
P_3	Adjust transconductance	$1/V^3$	17.29

In the original formulation [41], the thermal effects are included by introducing a linear dependence on temperature on the parameters I_{pk0}, i.e. the drain current for the maximum transconductance, and the fitting parameter P_1, which determines the transconductance and the threshold voltage.

4.4. Cryogenic Model Extension

A linear temperature dependence is not sufficiently accurate for the model to reproduce device behaviour from ambient down to cryogenic temperatures. In Figure 4.2, we show some DC I- V measurements performed on an n-type FinFET with 2 fins, 1 finger and a gate length of 16 nm at different temperatures. In these plots, the dependence of the device threshold, transconductance and output conductance on temperature is well evident. It is also interesting to observe that the largest variation appears moving from room temperature (i.e., 300 K) down to 77 K. For lower temperatures, down to 2.95 K, the behaviour of the transistor is approximately unchanged, as clearly visible looking at the plots of the transconductance and the output conductance with temperature in Figure 4.2 (b) and Figure 4.2 (d) [36].

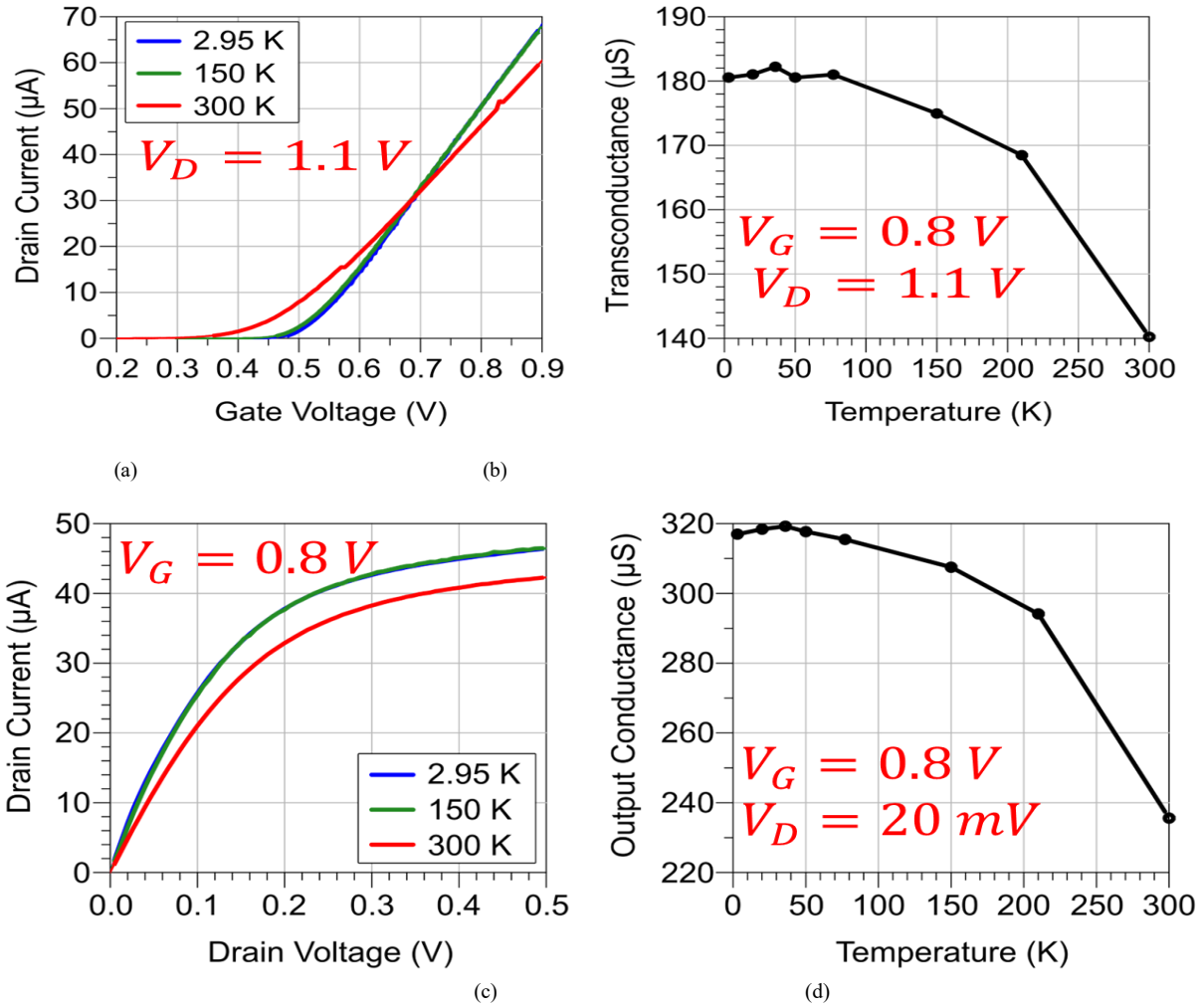


Figure 4.2. Measured DC I/V characteristics on the selected FinFET. (a) I_D vs. V_G at V_D = 1.1 V (b) Transconductance at V_G = 0.8 V and V_D = 1.1 V, (c) I_D vs. V_D at V_G = 0.8 V, (d) output conductance at V_G = 0.8 V and V_D = 20 mV for different temperatures.

In agreement with the previous results, the model defined by equations (4.1) and (4.3) have been modified by introducing some temperature dependent functions to reproduce such a kind of behaviour. Specifically, parameters P_1, P_3, and α have been redefined as:

$$P_1(T) = A_{P1}\left[1 + B_{P1}\tanh\left(C_{P1}\left(T - T_{ref}\right)\right)\right] \qquad (4.4)$$

$$P_3(T) = A_{P3}\left[1 + B_{P3}\tanh\left(C_{P3}\left(T - T_{ref}\right)\right)\right] \qquad (4.5)$$

$$\alpha(T) = A_{\alpha}\left[1 + B_{\alpha}\tanh\left(C_{\alpha}\left(T - T_{ref}\right)\right)\right] \qquad (4.6)$$

where T_{ref} is the reference temperature and A_x, B_x, and C_x are fitting cryo-parameters to be identified. The new expressions for P_1 and P_3 are responsible for modelling the temperature dependence of the threshold voltage and the transconductance, whereas α acts in the linear region of the I-V characteristics, thereby determining the transistor output conductance [36].

4.5. Model Identification

We applied the previously described modelling formulation to an n-type FinFET with 2 fins, 1 finger and a gate length of 16 nm. This device has been fully characterised by means of DC I-V measurements at temperature ranging from 2.95 K to 300 K [36], as reported in the previous chapter.

The model has been implemented and extracted in Keysight Advanced Design System (ADS). Model parameters have been firstly identified for $T = T_{ref}$ (i.e., 300 K), starting from the initial values directly derived from DC I-V measurements as described in [1], followed by a numerical optimization. Then, measurements at different temperatures (i.e., 2.95 K and 150 K) have been exploited for identifying the cryo-parameters of equations (4.4), (4.5) and (4.6).

A DC I–V simulation testbench was built in ADS and used for the extraction of Angelov model parameters. The schematic is shown in Figure 4.3.

The circuit is made up of the model, which is represented by X1. The drain-voltage source (SRC2) sweeps V_d linearly from 0 V to 1 V. The gate bias V_g is varied within the desired range (V_g start, V_g stop, V_g step) using a Parameter Sweep block (Sweep1) to create the family of transfer characteristics.

A Data Access Component (DAC) that reads the experimentally obtained dataset file "Nch_2X1_L16" imports in the CAD environment the measured data needed for parameter extraction and model validation. The simulator can access the measured drain current as a function of temperature, gate voltage, and drain voltage since the DAC is set up for linear interpolation in a rectangular domain. The correctness of the Angelov model parameters may be quantitatively evaluated at the reference temperature of 300 K for the different V_g and V_d and comparing the simulated drain current with the interpolated observed data [45].

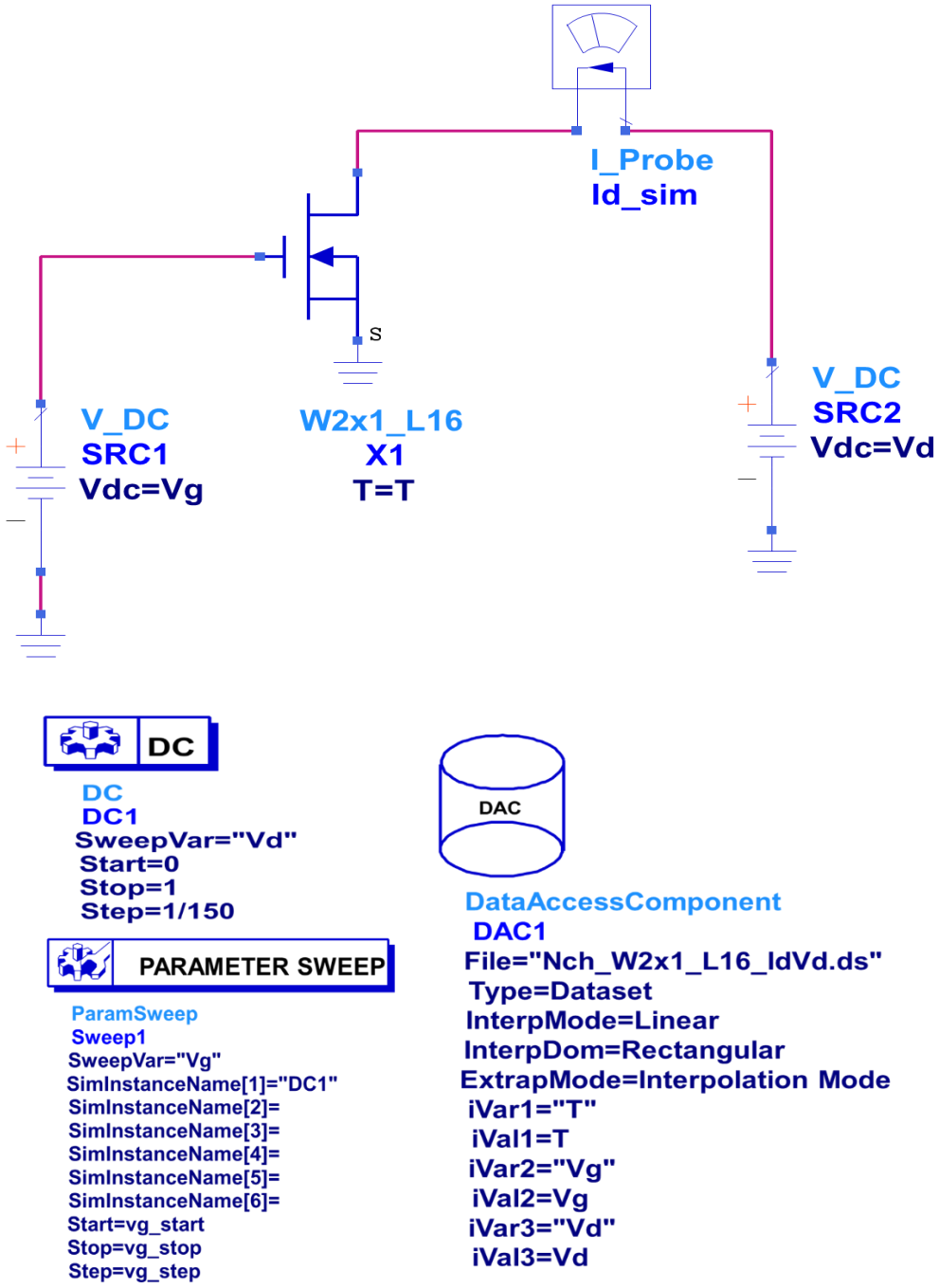


Figure 4.3. Schematic of the DC I–V simulation testbench used for optimization and validation of the Angelov model at 300 K. The circuit implements nested sweeps of gate and drain voltages, while the Data Access Component (DAC) imports the measured I_d–V_d dataset for comparison with the simulated drain current.

Table 4.3 shows the values of parameters after the numerical optimization against the measured DC IV characteristics at different temperatures.

Table 4.3: Parameters for Angelov's Model Validation

Parameters	Description	Unit	Values
A_{P1}	Linear shaping factor	Dimensionless	3.82
B_{P1}	Scaling factor	Dimensionless	0.26
C_{P1}	Linear Vgs coefficient	A/V	-0.0076
A_{P3}	Nonlinear shaping factor	Dimensionless	19.14
B_{P3}	Nonlinear scaling factor	Dimensionless	2.52
C_{P3}	Cubic nonlinearity coefficient	A/V^3	0.0095
A_{α}	Shaping factor	Dimensionless	5.57
B_{α}	Scaling coefficient	Dimensionless	0.20
C_{α}	Asymmetry coefficient	A/V^2	0.014
T_{ref}	Reference temperature	K	300

4.6. Validation at Reference Temperature

As a first validation, we want to compare the accuracy achieved by the proposed model formulation to a very established solution, i.e., the BSIM model [36], whose extraction has been described in the previous section. Both models were implemented and identified in ADS to fit the device behaviour of the DUT at 300 K temperature.

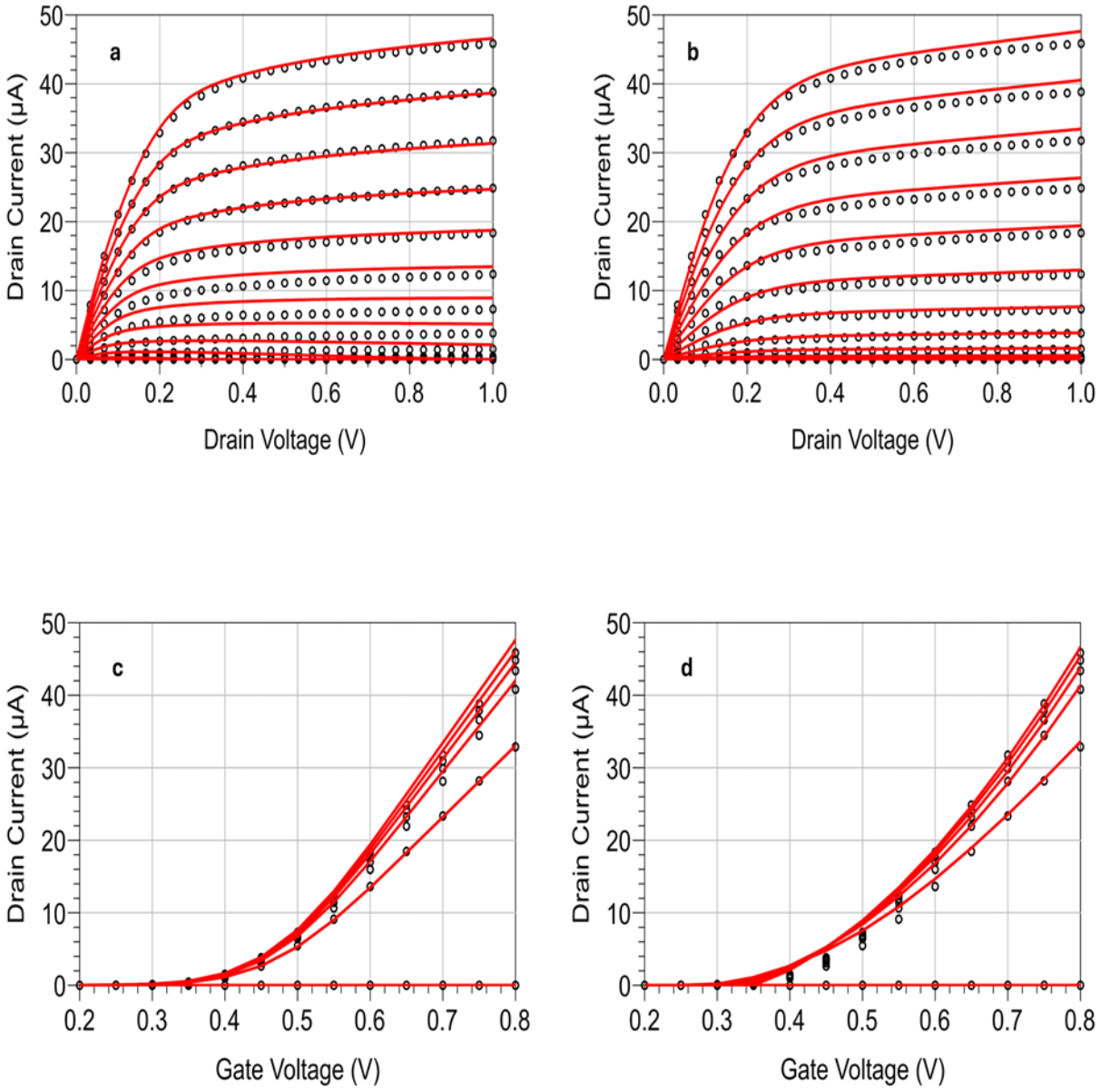
A comparison between simulated and measured data results is shown in Figure 4.4.

Table 4.4: Variables and their Sweep Ranges

Variables	Sweep
V_{ds}	0 to 1 V
V_{gs}	0.2 to 0.8 V

The BSIM model shows a good accuracy in predicting device behaviour. The discrepancies may be related to the fact that some of the model parameters, related to the technological process,

are not made available by the foundry and have been optimized during the model identification process. However, this may lead to suboptimal values, thus reducing the model accuracy.



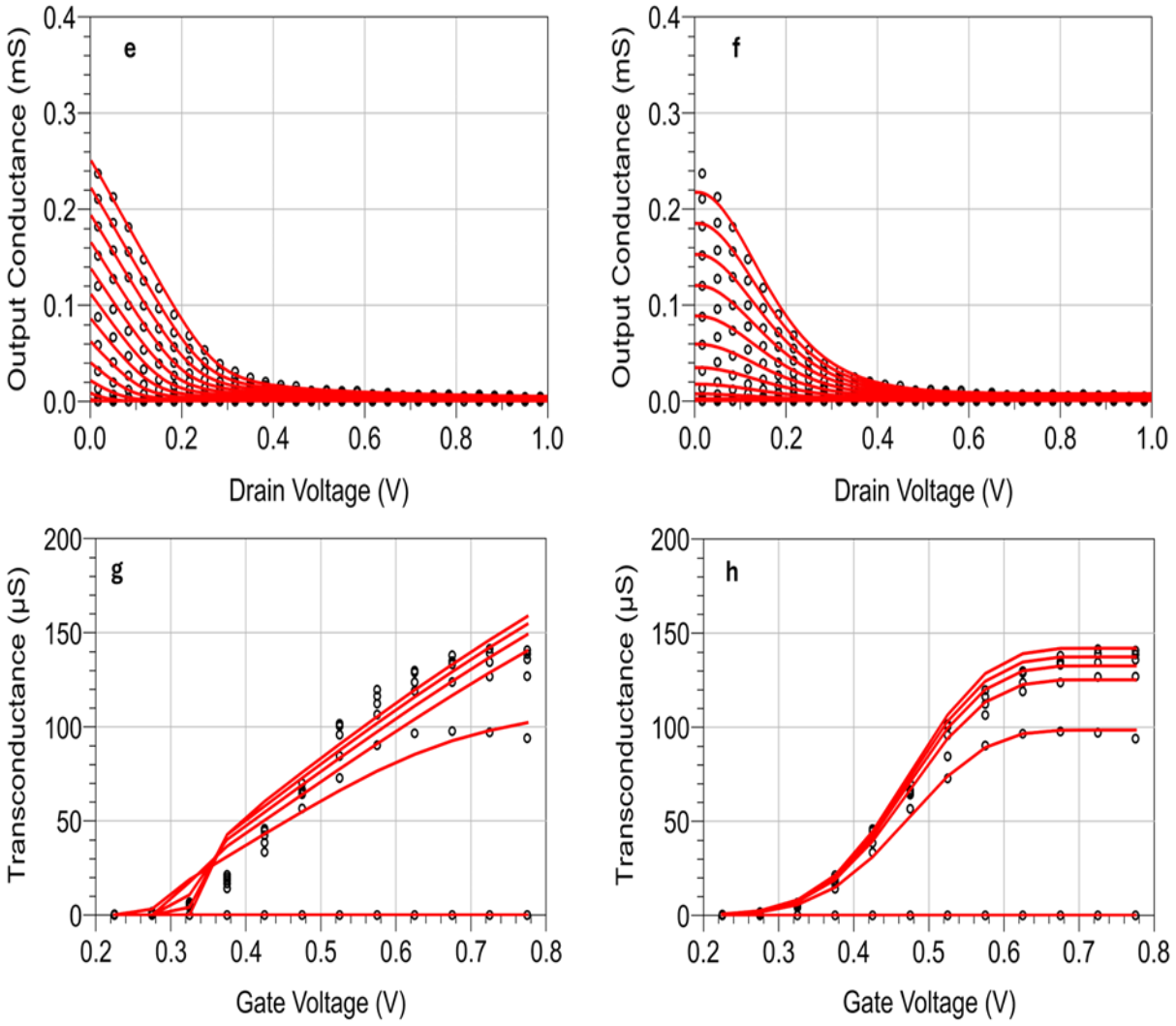


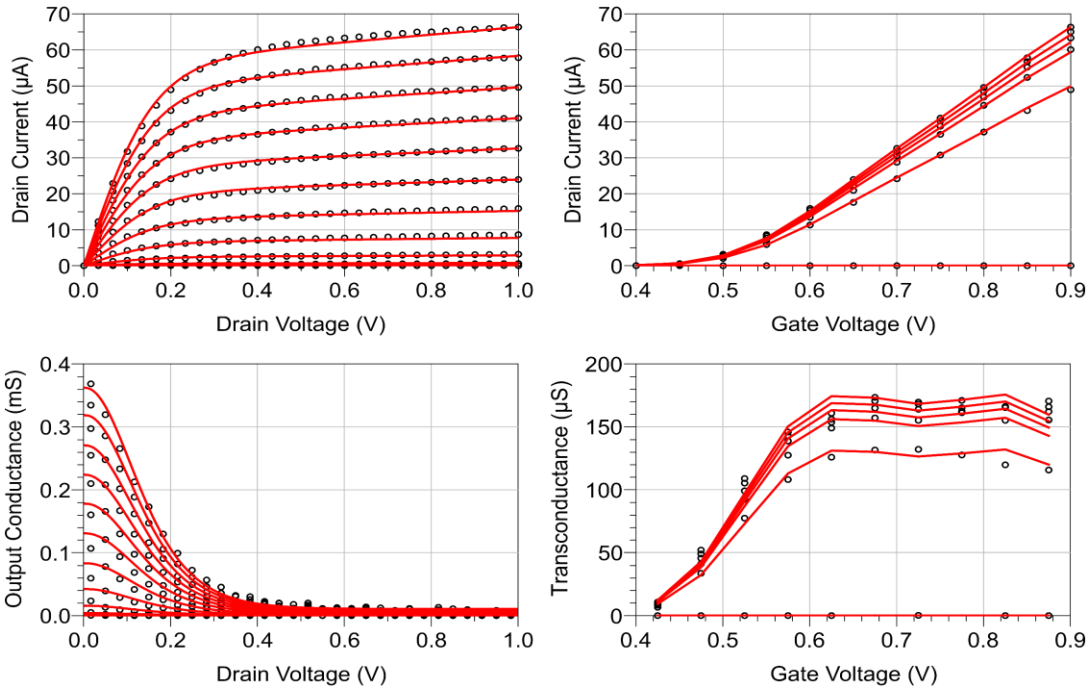
Figure 4.4. Comparison between BSIM (left) vs proposed (right) models at 300 K. Measurements (symbols) and simulations (solid lines). (a,b) I_D vs V_D for V_G from 0.2 V to 0.8 V, step 50 mV (c,d) I_D vs V_G for V_D from 0 V to 1 V, step 0.2 V, (e,f) output conductance vs V_D for V_G from 0.2 V to 0.8 V, step 50 mV, (g,h) transconductance vs V_G for V_D from 0 V to 1 V, step 0.2 V.

The proposed model offers a very good level of accuracy. The transconductances, i.e., the derivative of the drain current with respect to the gate voltage, is very well reproduced, with an excellent prediction of the threshold voltage [30]. The main discrepancy is related to the output conductance in the linear region of the transistor, whereas very good results are achieved under saturation. The capability of reaching such a high level of accuracy without the need for technological information is a great advantage of the proposed empirical model [37].

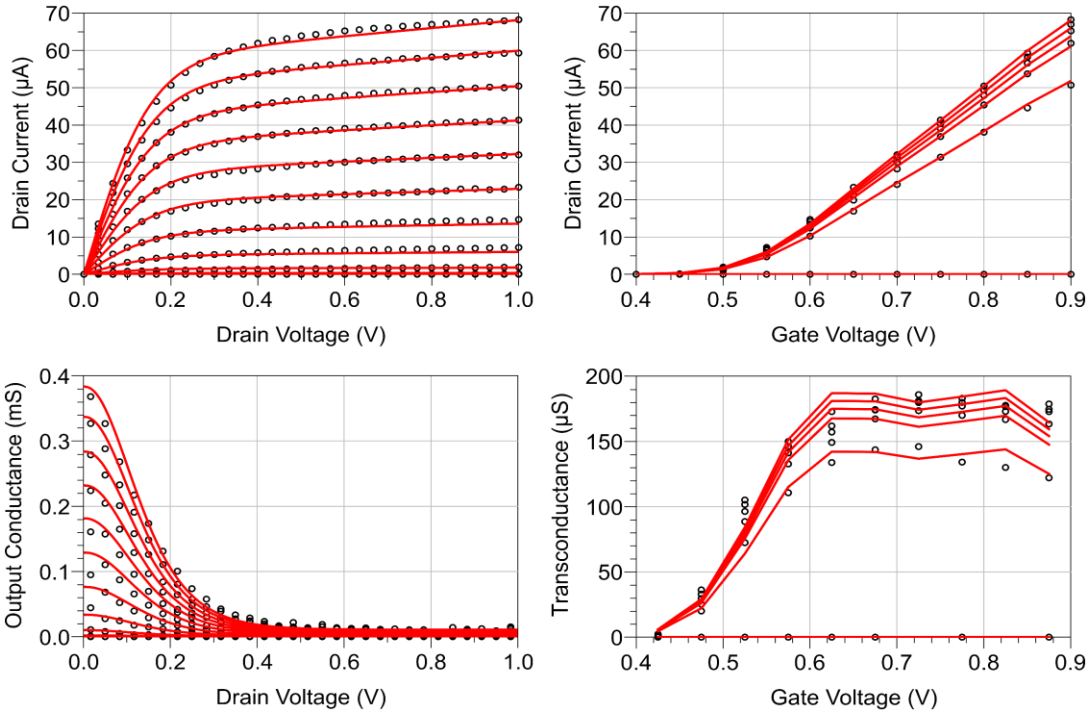
4.7. Validation of the Thermal Model

We are now presenting the model capability of predicting the device behaviour down to cryogenic temperature [36]. To this aim, we report a comparison between measured and

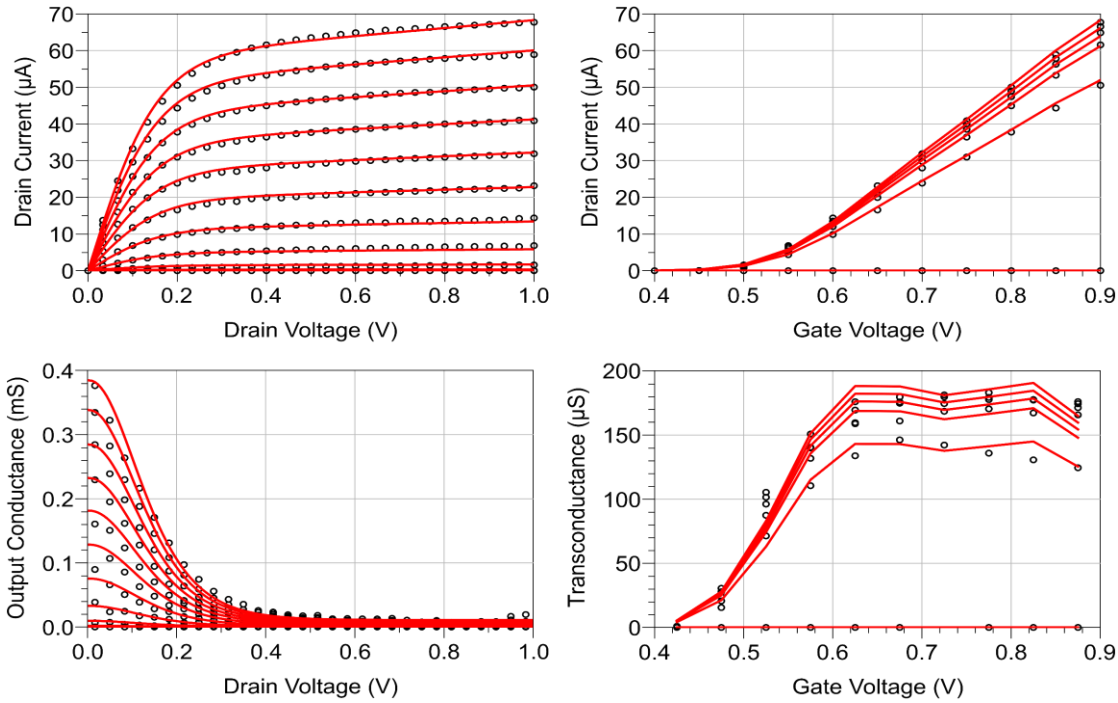
simulated DC I-V characteristics carried out at 2.95 K, 77 K and 210 K in Figure 4.5. It is important to note that 77 K and 210 K measurements were not part of the datasets used during identification.



(a)



(b)



(c)

Figure.4.5. Comparison between the measured (symbols) and simulated (lines) with the proposed model DC I-V characteristics, output conductance transconductance at (a) T = 210 K, (b) T = 77 K, and (c) T = 2.95 K.

The fitting of the DC I-V characteristics, transconductance and output conductance is very good at each temperature, especially on the output conductance at low drain voltages. The increase in the saturation current at cryogenic temperatures due to the increased carrier mobility is very well reproduced together with the variation of the gate threshold voltage. We note that the 210 K and 77 K cases were not included in the identification phase. The capability of the model to reproduce the device behaviour also in these cases proves the robustness of the proposed approach.

The temperature dependence of MOSFET characteristics is governed by the combined influence of several physical mechanisms, primarily the variation of carrier mobility and the shift of the threshold voltage with temperature[47]. Under specific bias conditions, these temperature-dependent effects may compensate each other, leading to operating points where the electrical characteristics of the device become nearly independent of temperature [48]. These conditions are commonly referred to as zero temperature coefficient (ZTC) bias points [49, 50]. For the drain current this behaviour is known as the current zero temperature coefficient (CZTC) point, which is the bias condition at which the drain-current temperature

derivative approaches zero ($\partial I_D / \partial T \approx 0$). Similarly, the transconductance zero temperature coefficient (GZTC) point is defined as the bias condition at which the temperature dependence of the transconductance is minimized ($\partial g_m / \partial T \approx 0$). [51]. Identifying these bias conditions is highly significant for designing temperature-stable circuits, notably in cryogenic electronics and analog/RF applications. Because of this, examining the temperature dependence of the DC characteristics and their higher-order derivatives can provide better understanding of device behaviour and enable in-depth validation of compact models that operate over a wide range of temperatures [52, 53].

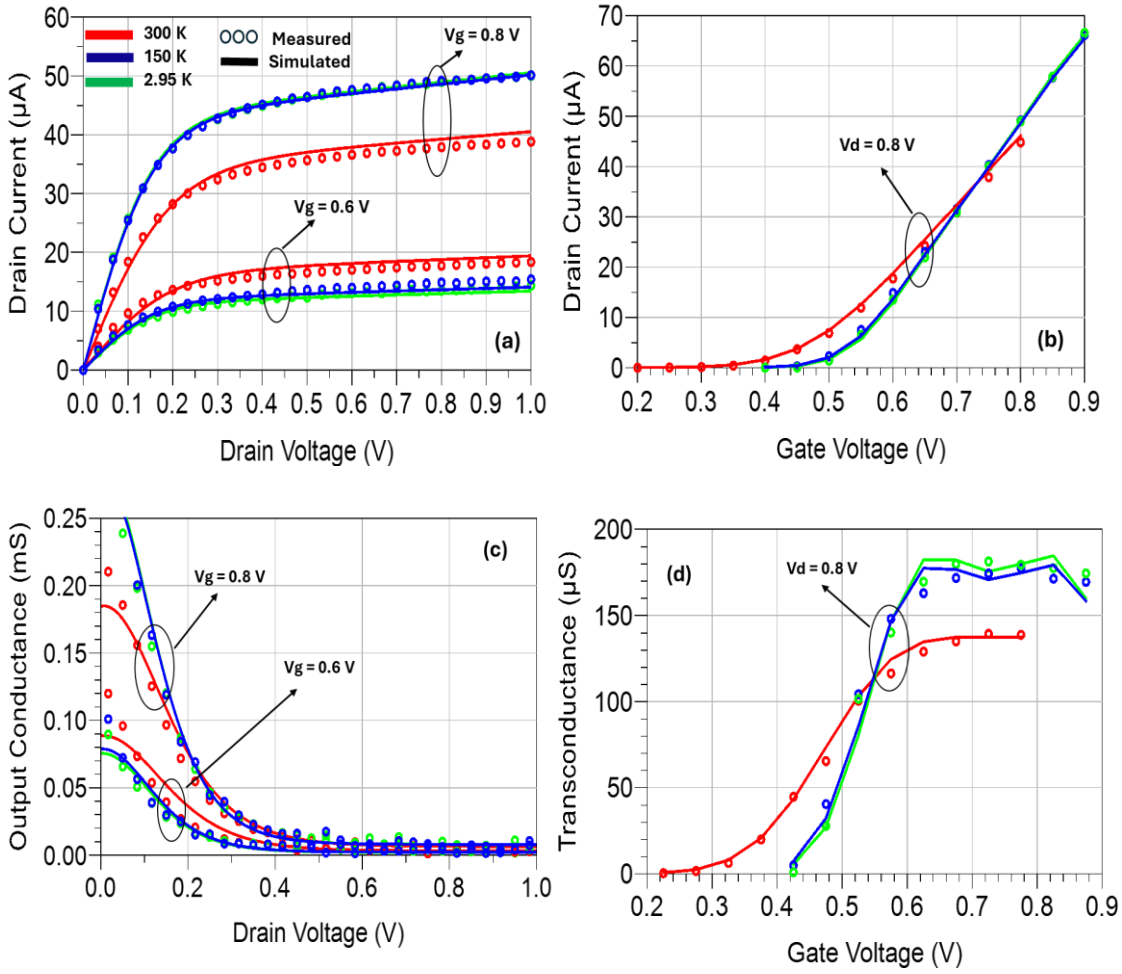


Figure 4.6. Measured (symbols) and simulated (lines) device characteristics at 300 K, 150 K, and 2.95 K: (a) I_d–V_d at V_g = 0.6 V and 0.8 V, (b)) I_d–V_g at V_d = 0.8 V,(c) output conductance versus V and (d) transconductance versus V_g.

The simulated and measured I_d-V_d output characteristics for three temperatures at various gate voltages are shown in Figure 4.6(a). The modified Angelov's model captures the effects of temperature as evidenced by the good agreement between measured and simulated data.The I_d - V_g transfer characteristics at a fixed drain bias of V_{ds}= 0.8 V are shown in Figure 4.6(b). As the temperature drops, there is an apparent increase in the threshold voltage. This behaviour is incorporated into the Angelov's model as demonstrated by the way the simulated curves match the measured data, especially in the subthreshold and moderate-inversion regions.

The output conductance g_{ds} extracted from the I_d-V_d data is displayed in Figure 4.6(c). As expected, g_{ds} approaches a nearly zero value at saturation at all temperatures as drain voltage increases. The model is in good agreement with measurements, suggesting that the derived parameters accurately reflect the actual device behaviour.

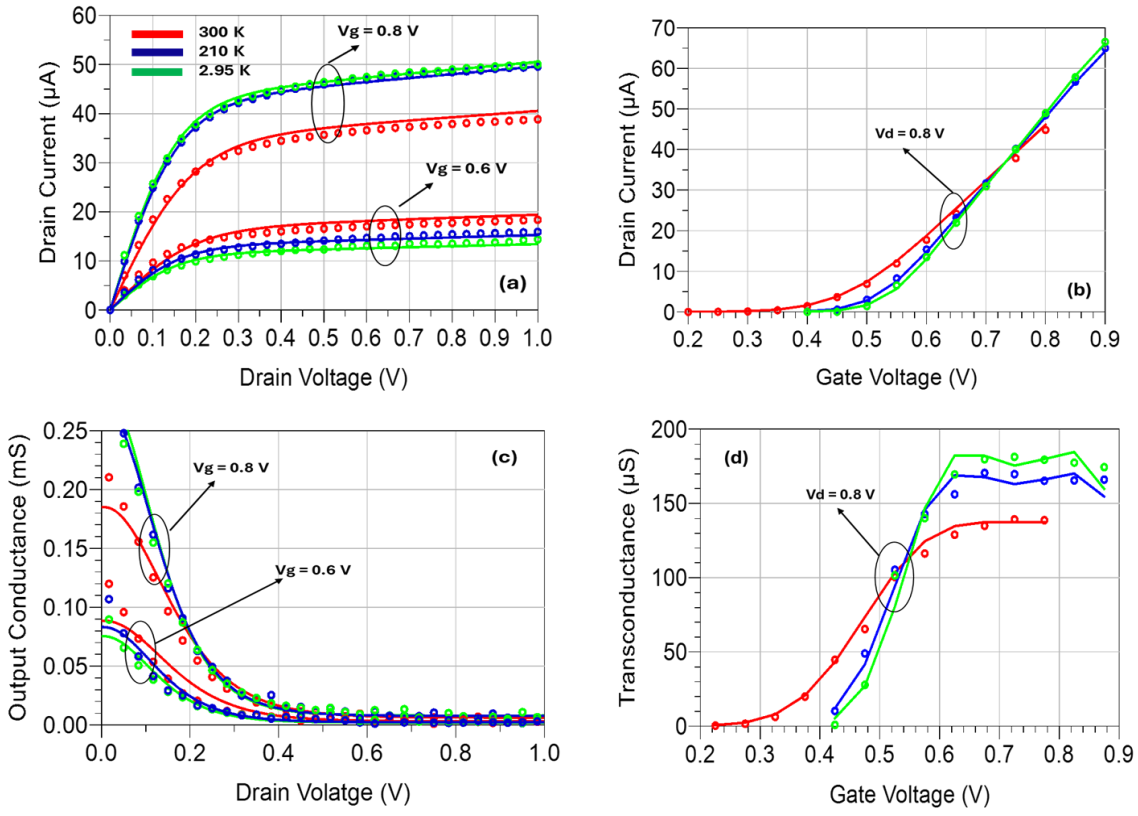


Figure 4.7. Validation of the proposed model at 300 K, 210 K, and 2.95 K Measured (circles), Simulated (solid lines) (a) I_d–V_d characteristics at V_g = 0.6 V and 0.8 V (b) I_d–V_g curves at V_d = 0.8 V, capturing the temperature-dependent threshold voltage shift (c) Extracted output conductance g_d at V_g = 0.6 V and 0.8 V (d) Transconductance g_m at V_d = 0.8 V, showing mobility enhancement and the g_m peak shift under cryogenic conditions.

The output conductance g_{ds} extracted from the I_d-V_d data is displayed in Figure 4.6(c). As expected, g_{ds} approaches a nearly zero value at saturation at all temperatures as drain voltage increases. The model is in good agreement with measurements, suggesting that the derived parameters accurately reflect the actual device behaviour.

Furthermore, for $V_{ds} = 0.8$ V, Figure 4.6(d) shows the transconductance g_m as a function of the gate voltage. The peak transconductance rises significantly as the temperature drops. By adding explicit temperature dependency to model formulation, it takes these effects into consideration. The validity of the extracted model parameters for characterizing transconductance behaviour from cryogenic to room temperature is confirmed by the simulated g_m curves, which match the amplitude and shape of what has been seen throughout all temperatures.

The predictions at 210 K are reported in Figure 4.7. Since this temperature is not included in the identification phase, the results validate the model from cryogenic to ambient temperatures.

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Conclusion

This thesis has developed and validated an empirical compact modeling framework for FinFET devices operating from ambient down to cryogenic temperatures, with a primary focus on a 16 nm technology node. Through a coordinated program of measurement, modeling, and optimization, the work bridges device level physics and circuit level needs for RF and quantum computing oriented cryo CMOS.

Comprehensive DC characterization was performed for both n- and p-type FinFETs across multiple geometries, encompassing short and long-channel variants. The measured DC IV characteristics were acquired across temperature to quantify performance evolution and to isolate geometry dependent effects. These data established a consistent reference for evaluating cryogenic behaviour and informed the choice of modeling constructs and parameter trends.

Building on these measurements, an empirical compact modeling methodology was formulated and applied to the 16 nm FinFET platform. Model parameters were optimized to reflect temperature dependencies and geometry scaling, and the resulting simulations were benchmarked against the experimental dataset. The strong agreement between simulated and measured DC characteristics across device polarities, channel lengths, and temperatures demonstrates the fidelity and robustness of the approach.

A central contribution of this thesis is a new empirical formulation for the DC drain current in FinFETs that remains accurate from room temperature to cryogenic conditions. The formulation captures key cryogenic phenomena at the compact model level while preserving computational efficiency and compatibility with standard circuit simulation.

The results have several implications. First, the demonstrated model measurement agreement enables reliable DC operating point prediction at cryogenic temperatures, which is foundational for biasing, linearity, and gain planning in RF front ends and cryo-CMOS control circuits. Second, the explicit treatment of device size dependencies offers practical guidance for selecting channel lengths and widths/fins to balance drive strength, output resistance, and transconductance in cryogenic conditions. Third, the availability of a compact, empirical formulation facilitates rapid integration into PDK level flows to accelerate circuit prototyping for quantum technologies.

In summary, the thesis delivers: (i) a broad experimental baseline of DC cryogenic behaviour for advanced node FinFETs across device types and geometries (ii) an empirically grounded, temperature and geometry aware compact modeling strategy for 16 nm FinFETs (iii) parameter optimization and verification against measurements with good agreement and (iv) a new empirical drain-current formulation ready to be integrated in a complete RF model for cryogenic RF and quantum computing contexts. Together, these advances provide a practical foundation for accurate device level prediction and PDK ready compact modeling at cryogenic temperatures, enabling more confident circuit design for next generation cryo-electronic and quantum systems.

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