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Charge transport in ultrathin silicon-on-insulator films for advanced device applications

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Abstract

The always increasing volume of processed data, together with the continuous demand for higher performance and lower power consumption, has driven the relentless scaling of microelectronic components. As transistor architectures advance toward the Ångström era, the introduction of ultrathin silicon (Si) films and nanoscale three-dimensional (3D) architectures became essential to achieve better electrostatic control of the channel and improve device performance. At the same time, the slowdown of performance improvement by standard scaling in conventional CMOS technology has motivated the exploration of new alternative architectures and emerging computational paradigms, including unconventional computing and quantum electronics. These trends highlight the need for new material engineering strategies and doping methodologies capable of supporting both continued scaling and novel device functionalities.

Doping at the nanoscale remains a central and unresolved challenge, particularly for Si nanostructures with reduced dimensionality, where quantum confinement, interface effects, and dopant segregation strongly influence electrical behavior. Silicon-on-insulator (SOI) substrates, with their inherently electrically isolated and well-controlled device layer, offer exceptional tunability in key parameters such as interface quality, doping concentration, and film thickness. These characteristics make SOI an ideal platform for investigating and understanding the properties of doped two-dimensional (2D) Si films. Moreover, the versatility and maturity of Si and SOI technologies provide a robust foundation for developing new device strategies that extend *beyond CMOS*.

Standard top-down doping processes, such as diffusion and ion implantation, face fundamental limitations as Si films approach the 2D regime. The reduced dimensionality enhances quantum confinement, interface, and surface effects, which strongly affect dopant incorporation and activation. Short diffusion length, dopant segregation, and implantation-induced lattice damage lead to poor control over concentration profiles and degradation of the film, making it increasingly difficult to achieve uniform and predictable electrical properties in ultrathin Si nanofilms. Interest is now increasing in bottom-up approaches to overcome the limitations of previous technologies. Among the proposed strategies, polymeric precision doping stands out for its unique potential to achieve precise control, scalability, and compatibility with existing fabrication processes.

In the first part, this work investigates the applicability of this alternative bottom-up

approach to achieve predictable semiconductor doping of ultrathin Si films in a wide range of dopant concentration. A set of dedicated processing techniques was developed to provide accurate and tunable independent control over both device layer thickness and dopant concentration, which was varied over two orders of magnitude. In addition, specific test structures were designed and integrated into the fabrication process to enable systematic electrical characterization and quantitative analysis of the properties of the film.

This research explores the intricate interplay between different fundamental phenomena induced by dopant confinement, with particular attention to the role of non-passivated interface states at the Si/SiO_2 interface and their impact on carrier concentration and mobility. The influence of different capping layers and interface conditions was also investigated, as well as the effect of dielectric mismatch between Si and its surroundings. The behavior of the metal–insulator transition in ultrathin films is analyzed, together with the observation of quantum phenomena emerging at high dopant concentrations and in 2D conduction regime. The experimental results show the opportunity for engineering exchange interactions and realizing artificial graphene-like electronic structures in doped Si films, by introducing controlled topological characteristics into the device layer.

The second part of this work focuses on the realization of advanced device architectures on the SOI platform. A first approach details the preparation protocol and examines transfer characteristics of multi-electrode devices based on networks of phosphorus donors. Understanding the fundamental properties and physics of the material enables the design of devices with tailored functionalities. These devices demonstrated negative differential resistance, an essential feature necessary for implementing nonlinear operations and solving linearly inseparable classification problems.

An alternative approach exploits single-electron tunneling through nanoscale potential wells formed around dopant clusters, acting as quantum dots. The feasibility of co-doping in Si nanochannels, even at high concentrations, was explored as a strategy to enhance device stability, reproducibility, and yield. By taking advantage of Coulomb blockade to control charges at the individual level, these devices offer a promising route toward high-temperature operation and ultralow-power electronics.

Overall, this work investigates the physical characteristics that drive the structural, electronic, and transport properties in doped ultrathin Si nanofilms and presents device applications developed to take advantage of the doped SOI platform. By bridging the atomistic mecahnisms associated to dopant incoprporaiton and activation with the properties of the material and devices, this fundamental study aims to provide the foundation for empirical models of doping at the nanoscale and for versatile fabrication strategies for the next-generation and *beyond-CMOS* Si-based technologies.

Chapter 1

Introduction

In the world of semiconductor science, the controlled doping of silicon (Si), the cornerstone material of modern electronics, undoubtedly marked a turning point in the evolution of research of all subsequent materials and defined today's information. The remarkable ability to tailor the electrical properties of Si through the controlled and intentional incorporation of impurity atoms has, over the decades, driven continuous innovation and miniaturization, shaping the microelectronic revolution and inspiring an always expanding landscape of materials, processes, and device architectures.

In this chapter, I present the concepts of semiconductor doping, introducing both conventional techniques and alternative approaches that are compatible with the reduced dimensions imposed by the continue device miniaturization. I describe the challenges associated with achieving controlled doping at the nanoscale and the advantages of employing a well-controllable system, the silicon-on-insulator (SOI) substrate, as the platform to investigate the complex interplay of many different physical phenomena. Finally, I introduce the alternative bottom-up doping strategy that constitutes the basis of this work and review the most recent results obtained with this technique prior to this thesis.

1.1 Semiconductor doping

Electronic devices widely rely on a specific class of materials among all those present in nature: semiconductors. Besides their mechanical and chemical properties, the choice of semiconductor materials is primarily dictated by the electrical characteristics and, most importantly, by the possibility to precisely tune and control them. The electrical conductivity σ (in S/cm) of such materials lies between those of insulators and metals. Their peculiar characteristic is that σ is extremely sensitive to external stimuli such as temperature, light, magnetic field, and small concentrations of impurity atoms.

The initial conceptual breakthrough associated with the invention of integrated circuits, was the realization by Noyce and Kilby that multiple transistors could be made in the same piece of Si, achieving monolithic integration and revolutionizing electronics [1, 2]. The

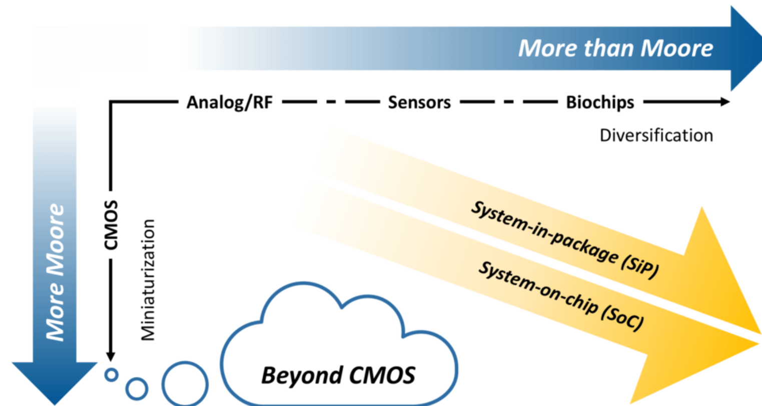


Figure 1.1: Integration of novel approaches to CMOS technology as discussed in the International Roadmap for Devices and Systems (IRDS) in 2022. Adapted from [5].

widespread success and subsequent evolution of this monolithic integration was fundamentally enabled by the unique properties of the Si material, primarily its compatibility with the complementary metal–oxide–semiconductor (CMOS) platform. CMOS is the most widely employed technology for integrated circuits. It enables high integration density, low power consumption, and large-scale processing [3, 4].

From its very beginning, the semiconductor industry has aggressively pushed towards device miniaturization. The main reason behind this continuous downscaling is that reducing the dimensions of transistors increases the density of devices per unit area, resulting, at the same time, in higher computational power and lower energy consumption. These two factors have led to the exponential growth in performance and reduction in cost that characterize modern microprocessors [5].

An historical observation by Gordon Moore is that the market demand for functionality per chip doubles every 1.5 to 2 years. He also observed that performance (in millions of instructions per second, MIPS) also doubles every 1.5 to 2 years [6]. Although viewed by some as a "self-fulfilling" prophecy, *Moore's Law* has been a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for more than 50 years [5].

Currently, semiconductor manufacturing has reached the 3 nm technology node. However, further scaling is increasingly getting more difficult by the physical limits of top-down lithographic processes, interconnect parasitics effects, and quantum mechanical phenomena. Interest is now increasing in bottom-up approaches to overcome the limitations of previous technologies. These challenges are leading to a gradual slowdown in the pace predicted by *Moore's Law* in shrinking transistor dimensions.

To overcome these barriers, the semiconductor community has identified three main strategic directions for future progress: *More Moore*, *More Than Moore*, and *Beyond CMOS* (Figure 1.1) [5].

More Moore. *More Moore* continues the conventional CMOS scaling paradigm by improving device architecture and geometry, gate stacks materials, high-k oxides, and process control to sustain further performance and density improvements. Strain engineering, and innovations in patterning techniques such as extreme ultraviolet (EUV) lithography are prominent examples. Nevertheless, power dissipation and short-channel effects could remain critical bottlenecks.

More Than Moore. Rather than directly reducing dimensions, *More Than Moore* focuses on enhancing new functionalities by exploiting the heterogeneous integration of other technologies on a single chip or package. It allows for non-digital functionalities (radio-frequency communication, power control, passive components, sensors, actuators) to migrate from the system board-level into the package (SiP) or onto the chip (SoC). It is a complementary technology option that can be combined with *More Moore* to create new high value systems. Research in this field is driven by application needs, rather than technology requirements. During the last decade, multifunctional devices have become the building blocks of virtually every application field imaginable, from the internet of everything to artificial intelligence (AI) [5].

Beyond CMOS. *Beyond CMOS* explores entirely new information processing paradigms, architectures, and physical mechanisms. This includes spintronics, ferroelectric and phase-change devices, 2D materials, and quantum computing. In these approaches, the medium used to carry the information may shift from electrical charge to spin, polarization, or photonic excitations, or the architecture itself may evolve toward neuromorphic or quantum systems. Bottom-up nanofabrication and molecular-scale engineering thus emerge as powerful tools to develop new materials and architectures for *beyond CMOS* electronics.

Because of the importance of bottom-up approaches in future semiconductor development, this work focuses on the application of a self-assembling approach for a mild, fully bottom-up alternative to achieve one of the most critical steps in semiconductor device fabrication: *doping*. Doping, i.e. the controlled and intentional introduction of impurity atoms into the lattice structure (typically between 0.0001 % and 1 %), plays a fundamental role in defining the electrical properties of semiconductors. It allows precise modulation of the Fermi level position, carrier concentration, and conductivity, ultimately enabling key device functionalities.

In crystalline Si, doping typically involves substituting a Si atom with a Group III or Group V element. A phosphorus (P, Group V) atom donates one excess electron, weakly bound and easily thermally ionized, thus introducing a negative charge carrier, an electron and forming *n*-type Si (Si:P). Conversely, a boron (B, Group III) atom accepts an electron, creating a positively charged hole that acts as a mobile carrier with higher effective mass, resulting in *p*-type Si (Si:B) [7]. The most common donor impurities in Si include phosphorus

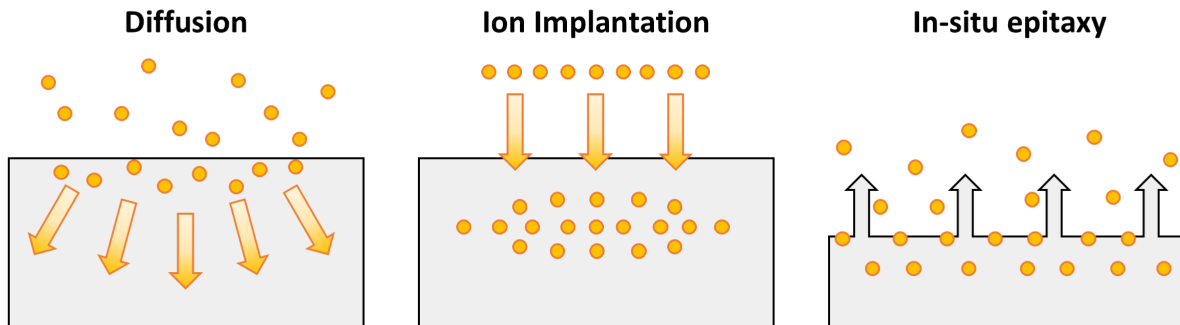


Figure 1.2: Schematic representation of the three main processes employed to achieve semiconductor doping.

(P), arsenic (As), and antimony (Sb), while acceptors are boron (B), gallium (Ga), and indium (In).

The intentional introduction of such dopants introduces discrete energy levels within the bandgap, near the conduction or valence bands, modifying carrier concentration and mobility. Dopant–defect interactions, clustering, and activation kinetics play a major role in determining the final electrical behavior of doped Si. Moreover, at high concentrations, exceeding the solid solubility limit, dopant atoms tend to cluster, leading to electrical deactivation and altered band structure. These complex interactions highlight the criticality of controlling dopant distribution, activation, and diffusion during processing, which is essential for modern CMOS fabrication.

At the state-of-the-art, semiconductor crystals are doped using three main processes: *diffusion*, *ion implantation*, and *in-situ epitaxial incorporation* (Figure 1.2). Each technique offers distinct advantages and limitations in terms of precision, throughput, and damage control. In the following paragraphs, I summarize the fundamental working principles of each conventional doping technique, discussing their distinct advantages and associated challenges.

Diffusion

In diffusion doping, the semiconductor substrate is exposed to a dopant source at elevated annealing temperatures ($T_A \sim 800 - 1100\,^{\circ}C$), typically in a quartz furnace. Various dopant sources are employed, from gaseous to solid. Dopant atoms diffuse into the substrate due to concentration gradients, governed by Fick's laws [8]. Two primary diffusion regimes exist: [8]

1. **Constant-source diffusion:** a constant dopant concentration is maintained at the surface throughout the process, typically in vapor phase, yielding a complementary error-function (erfc) concentration profile.

2. **Limited-source diffusion:** a finite dopant dose is pre-deposited on the surface, and diffusion proceeds with decreasing surface concentration, yielding a Gaussian-like profile.

Diffusion offers a simple and mild mechanism, with no lattice damage and high throughput, making it particularly suitable for large-area doping such as in solar cells. However, the highly isotropic dopant scattering motion driving diffusion, results in significant lateral spreading. This effect greatly reduces spatial control, which must be achieved following a different protocol. The ratio between lateral and vertical penetration of impurities is of the order of 65–80 % [7]. Moreover, diffusion produces profiles with gradients of concentrations rather than abrupt junctions, which can negatively affect breakdown voltage, device performance and electrical isolation. Larger spacing between adjacent devices or doped regions is required to prevent undesired interactions, making conventional diffusion inappropriate for ultra scaled applications.

Ion Implantation

In advanced technology nodes, diffusion alone is insufficient, motivating the adoption of a technique characterized by a higher anisotropy, ion implantation.

Ion implantation consists of a beam of ionized particles with a certain energy that are introduced into the target substrate. Ion implantation guarantees precise control of the dopant dose by monitoring the current of ions. Moreover, changing the energy of the beam from keV to a few MeV, the depth of the implanted region varies from few nanometers to several micrometers [7]. The width of the dopant profile in the substrate also varies as a function of the beam energy [9].

As ions penetrate the crystal, they lose energy through two primary mechanisms:

$$\frac{dE}{dx} = S_n(E) + S_e(E) \tag{1.1}$$

where $S_n(E)$ is the nuclear stopping power, elastic collisions with lattice atoms, and $S_e(E)$ is the electronic stopping power, inelastic interactions with the electron cloud.

The resulting dopant distribution follows a Gaussian profile along the beam direction [9]:

$$C(x) = C_0 \exp\left[-\frac{(x - R_p)^2}{2\sigma_p^2}\right] \tag{1.2}$$

where R_p is the projected range (mean penetration depth) and σ_p the projected straggle (standard deviation). The maximum concentration of dopants is not at the surface but at depth R_p.

The ion distribution perpendicularly to the incidence axis is also described by a Gaussian curve with standard deviation $\sigma_\perp$, the lateral straggle. The typical values are generally smaller than in diffusion doping, making ion implantation more suitable for doping of small structures.

Ion implantation provides excellent dose and depth control and is highly reproducible. However, it is highly directional and not compatible with 3D nanostructures. Moreover, it induces damages to the lattice, amorphization of the crystal and end-of-range defects that require additional post-implantation annealing for dopant activation and recrystallization, which often cannot be recovered completely even after the thermal treatment.

In-situ Epitaxial Incorporation

With the recent development of ultrascaled structures, in-situ doping became a widely employed bottom-up approach, especially in advanced CMOS applications such as source and drain extensions, SiGe heterostructures, and quantum well devices.

In-situ doping, or epitaxial incorporation, involves introducing dopant precursors during the epitaxial growth of the substrate or nanostructure directly. The dopant atoms are incorporated substitutionally as the crystal grows, enabling atomically abrupt and highly uniform dopant distributions. During Si epitaxy, tuning the precursor flow rates and growth temperature, it is possible to precisely vary dopant concentration and depth. This method is ideal for forming ultra-shallow junctions and delta-doped layers, as dopant incorporation occurs under equilibrium conditions without any post-growth thermal treatment and subsequent diffusion [10].

Despite its advantages, the incorporation efficiency of dopants strongly depends on surface kinetics and growth conditions, leading to non-linear and material-dependent behavior. High dopant concentrations can degrade the crystalline quality of the epitaxial layer, promoting defect formation and stacking faults. In-situ incorporation remains extremely costly and complex, requiring precise control over all the processing parameters. Moreover, because dopants are already introduced during growth, control of the dose and its spatial distribution is significantly limited without additional masking or etching steps.

To achieve abrupt or highly localized concentration profiles, these conventional techniques are complemented by advanced approaches such as delta-doping, modulation doping, and non-equilibrium solid solubility [11, 12, 13, 14].

Over the decades, progress in doping chemistry and process engineering has enabled precise tailoring of dopant profiles at the nanometer scale, supporting both continuous device scaling and novel architectures for CMOS, solar cells, and sensors [15]. However, despite this maturity, achieving high activation, minimal diffusion, and predictable dopant behavior at ultralow or ultrahigh concentrations and particularly in nanoscale geometries, remains a major challenge.

1.2 Doping at the nanoscale

In order to follow the well-known *Moore's law* already introduced [6], and driven by the continuous search for higher performance and energy efficiency, semiconductor-based microelectronic devices have been characterized by the continuous scaling down of their

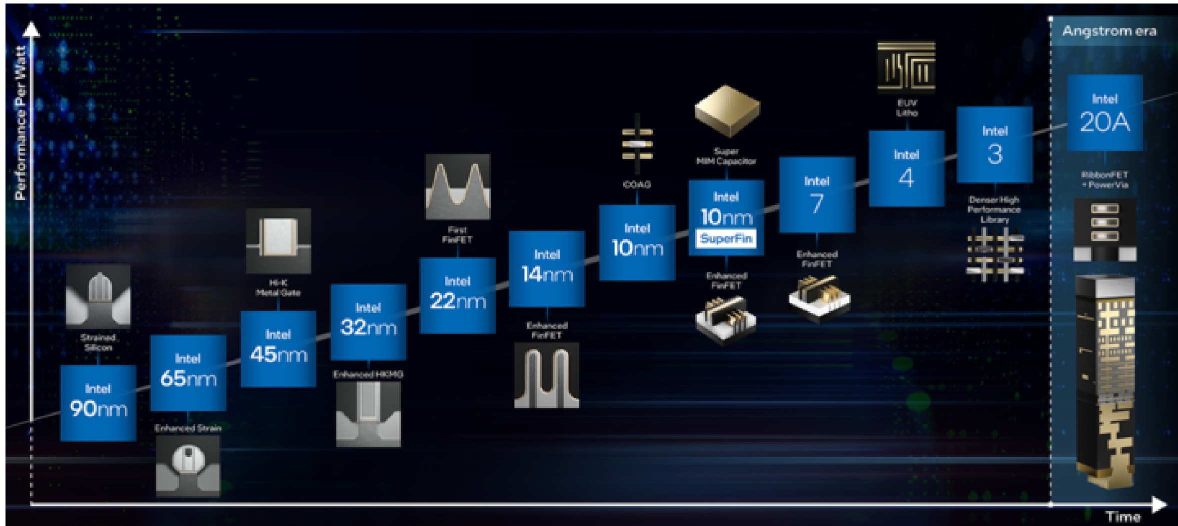


Figure 1.3: Miniaturization roadmap for the scaling of advanced transistors [16].

components. This relentless miniaturization has allowed the realization of devices with progressively improved switching speed, reduced power consumption, and lower production costs per individual transistor [5]. The miniaturization roadmap for the scaling of advanced transistors up to 2025 by Intel is presented in Figure 1.3.

Conventional doping techniques, diffusion and ion implantation, were perfectly suited for the planar architecture of early MOS field effect transistors (FETs), which dominated advanced semiconductor technology for decades. By 2011, planar MOSFET technology reached a fundamental physical limit which prevented further downscaling, primarily due to short-channel effects (SCE) [17]. These effects occur when the channel length becomes comparable to the depletion regions of the source (S) and drain (D), leading to degraded threshold voltage and gate control, drain-induced barrier lowering, and increased leakage currents. Electrostatic control of the channel by the gate became no longer sufficient in planar configuration.

At the 22 nm node, with the introduction of tri-gate transistors, the semiconductor industry transitioned to three-dimensional (3D) FinFETs architectures [18]. In this technological node, the channel is formed in a thin Si fin which is surrounded by the gate around three sides. This configuration provides improved electrostatic control over the channel, mitigates SCE, enables higher drive current, and reduces parasitic capacitances, thus enhancing both performance and energy efficiency.

The introduction of EUV lithography around 2019 [19] marked a major technological leap, allowing patterning of features with a wavelength of 13.5 nm and thereby extending *Moore's law* beyond the optical lithography limits. The use of ion implantation was progressively reduced until the 7 nm node, when it was almost entirely substituted by in-situ epitaxy for

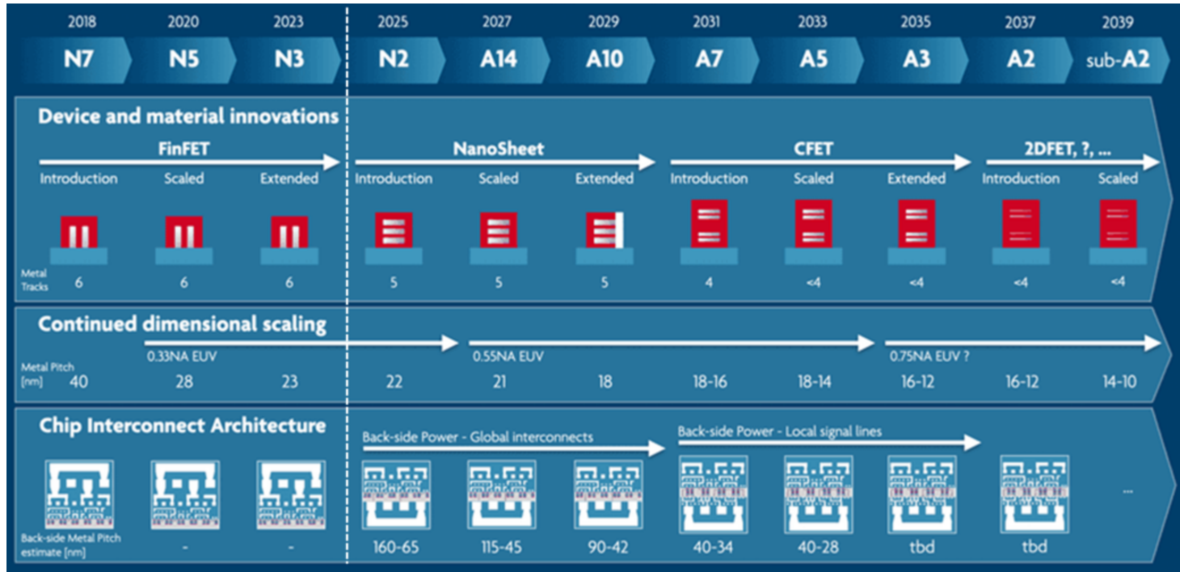


Figure 1.4: The 2025 imec logic technology roadmap [21].

the doping of S/D regions in order to minimize series resistance and strain the channel. In 2020, major semiconductor manufacturers started mass production of FinFET devices at the 5 nm technology node [20] and are currently producing, or preparing to introduce, nodes in the 3 nm and 2 nm range.

Naming conventions have diverged from actual physical dimensions and no longer corresponds directly to the gate length or half-pitch dimension, as it was for MOSFETs. Instead, it represents an "effective scaling factor" that combines density, performance, and power improvements.

As further downscaling continues, research and development efforts are already focusing on next-generation transistor architectures. Future predictions have already emerged to identify the options to extend the logic scaling roadmap (Figure 1.4). The next technological node will see the transition to a new 3D device architecture, the gate-all-around field-effect transistors (GAAFETs), also referred to as nanosheets or nanoribbon FETs, depending on the manufacturer. In this new architecture, the gate completely surrounds a Si nanosheet with a thickness of approximately ~ 5 nm, that is used as the channel, resulting in even stronger electrostatic control and superior subthreshold performance compared to FinFETs [22]. Moreover, the next generation transistors will introduce a back-side power delivery network (BSPDN) that completely moves the global power and ground interconnects from the front-side to the back-side of the wafer, freeing up crucial routing area. Despite the initial difficulties, GAAFETs are expected to enter high-volume manufacturing soon, with early production already being demonstrated by major foundries.

Further improvements will require the vertical stacking of nFET and pFET in a comple-

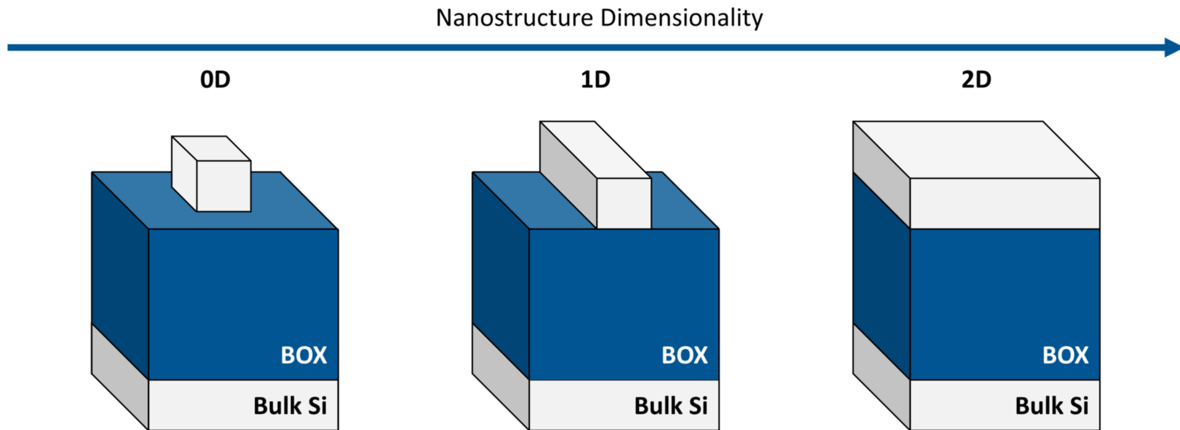


Figure 1.5: Schematic representation of confinement regimes in Si: 0D (Si Nanocrystals, SiNCs) , 1D (Si Nanowires, SiNWs), and 2D (ultrathin SOI nanofilms).

mentary FET (CFET) in order to significantly reduce the active area of each individual cell and improve the density on the chip. Just like in GAAFETs, the gate, common to n and p, fully wraps around and in between the Si channels, ensuring maximal electrostatic control. Imec foresees the introduction of CFETs at the A7 node onwards [21].

Doping of these 3D-devices introduced new technological and fundamental problems. The standard doping technique in mass production, diffusion and ion implantation, are already pushed to their fundamental limit. Damages caused by ions travelling through the Si lattice [7, 23] make ion implantation inefficient for nanometric electronic devices, even considering a high temperature thermal treatment to recover the crystal structure of the Si lattice after implantation. Moreover, this technique cannot be applied to complex 3D geometries because the highly directional nature of the ion-beam. Conversely, diffusion-based doping from solid and gas sources represents a milder alternative but faces limitations at controlling the dopant concentration and uniformity that are extraordinarily important in these ultra-scaled devices.

Doping at the nanoscale still remains a critical issue that requires systematical investigation. The small dimensions of the channel imply that even a few dopant atoms can drastically affect device behavior. In bulk materials, dopant distributions are effectively continuous, and device characteristics are determined by collective impurity behavior. However, as the characteristic device dimensions approach the average distance between ionized impurities, stochastic variations in dopant number and position introduce significant fluctuations in threshold voltage, mobility, and subthreshold slope.

The situation becomes more complex than in bulk when considering doping of Si in reduced dimensionality. Doping behavior can no longer be described by geometric scaling only, but must also account for the effects of confinement, which fundamentally modify both dopant states and carrier transport. Therefore, nanoscale doping requires also understanding

the transport mechanisms that govern how carriers move within these reduced dimensions. Depending on whether carriers are confined in one, two, or all three spatial directions, distinct regimes are identified (2D, 1D, and 0D, Figure 1.5), each imposing specific challenges for dopant incorporation, activation, and transport.

- **Zero-dimensional (0D) regime**. In the 0D limit, where carriers are confined in all three spatial directions, the discrete electronic density of states and large surface-to-volume ratio fundamentally alter dopant incorporation and activation [24].

  Si nanocrystals (Si NCs) represent one well-known example of this regime, showing size-dependent properties and significant challenges in achieving effective doping due to self-purification and dopant segregation effects. Incorporation of dopant impurities in 0D Si NCs with diameter below 10 nm is possible, even at concentrations well above the solubility limit [25, 26, 27]. However, the effective activation of these impurities and the availability of free charge carriers in the Si NCs is limited by quantum confinement and surface-related defects, which can significantly alter the electronic behavior. A comprehensive picture of the doping of these 0D systems is still missing [28, 29].

- **One-dimensional (1D) regime**. In the 1D limit, carriers are confined in two spatial directions but free along one. Under these conditions, surface and interface effects, as well as strain, drive dopant incorporation, activation, and charge transport. Doping in such reduced-dimensionality systems presents challenges different than those in bulk Si, including enhanced surface segregation, radial inhomogeneities, and dopant deactivation.

  Si nanowires (Si NWs) represent one of the most studied systems exhibiting 1D transport. The cylindrical geometry and strong dielectric mismatch with the surrounding media create a unique doping landscape. Through image-charge effects, this mismatch results in increased activation barriers and modified local band bending near the Si–dielectric interface [30, 31]. Doping strategies include in-situ axial or radial incorporation during growth, or post-growth implantation and annealing. However, the small diameters (often ~ 10 nm or less) hamper dopant activation and promote segregation at interfaces, surface trapping, and complex formation with defects. Diffusion becomes anisotropic and limited by the nanowire surface, enabling the engineering of graded or abrupt profiles via modulation or radial doping.

  The dielectric environment governs gate coupling, screening, and Coulomb scattering, making surface passivation and dielectric engineering (such as with high-k dielectrics) essential to maintain high mobility and control threshold voltages in Si NW-based devices [32, 33]. Bulk-like conductivities have been achieved down to the atomic scale by fabricating "interface-free" dopant wires embedded within single-crystalline Si [34], bridging atomic-scale dopant incorporation and positioning with macroscopic device performance.

- **Two-dimensional (2D) regime**. In the two-dimensional (2D) conduction regime, carriers are confined in one spatial direction but free to move in the other two. This regime is typically reached from bulk Si through progressive vertical confinement, leading to a continuous transition from 3D to 2D transport.

  The 2D conduction regime constitutes the physical transport mechanism of nanosheet FETs, which employ ultrathin Si channels. The reduced thickness of these films makes dopant profiles and activation highly sensitive to interface quality, dielectric environment, electrostatics, and strain. Moreover, the strict thermal budget imposed by ultrathin films constrains post-processing treatments such as annealing. Dopant distribution, activation efficiency, and interface quality are critical parameters that determine threshold voltage, mobility, and device variability.

  As a result, achieving controlled and uniform doping in 2D confined Si structures remains a key persistent challenge. Several doping strategies are employed, with ion implantation being historically widely used. It requires careful optimization of beam energy, dose, and post-implantation annealing to recover the damage in the reduced dimensionality. In-situ epitaxial incorporation is increasingly adopted for precise, ultra-shallow doping. Alternative approaches, such as laser annealing or solid-phase epitaxy, are used to activate dopants while minimizing diffusion [35, 36].

The 2D doping regime can be systematically explored using silicon-on-insulator (SOI) substrates, which provide a controlled and widely-employed platform for investigating both doping and transport in ultrathin Si films. In SOI, a thin crystalline Si layer, typically with a thickness $H_{SOI} \sim 10$ to 100 nm, is electrically isolated from the Si handle wafer by a buried oxide (BOX) layer. The BOX acts as a diffusion barrier, maintaining abrupt dopant profiles and preventing leakage into the handle wafer, but limits the thermal budget during processing. Excessive annealing can lead to defect formation, stress, or interfacial degradation at the Si/BOX boundary [37, 38].

Dopant activation and mobility in ultrathin SOI with $H_{SOI} < 30$ nm is severely influenced by the proximity and properties of the Si/BOX interface, as well as any residual strain, which can modify activation energies and dopant solubility[37, 39, 40]. Additionally, the intrinsic back-gate capability and potential for strain engineering in SOI enable novel advanced concepts such as fully-depleted SOI (FD-SOI) and back-gate tunable devices, where strain and bias can modulate activation and mobility [41, 42].

Surprisingly, despite the broad technological interest for this semiconductor platform, very few systematic studies addressed the problems and opportunities of doping of ultrathin SOI films [37, 39]. The tunable thickness, strain, and dielectric environment of SOI make it an ideal experimental platform to explore doping behavior in the 2D regime, bridging the gap between bulk Si and the ultrathin channels of next-generation devices.

1.3 Alternative doping strategies

To address the challenges associated with doping at the nanoscale, alternative compatible doping techniques, capable of controlling dopant placement and dose with high precision are required. In this section I briefly present a description of a range of doping strategies that are emerging as possible candidates to achieve controlled, or even atomically precise doping at the nanoscale.

Single ion implantation

A major limitation of conventional ion implantation is that implantation events follow a Poisson distribution. As a result, deterministic placement of very few atoms or a single dopant, is effectively not possible without additional control [43]. This statistical uncertainty motivated the development of single ion implantation, a direct extension of conventional ion implantation, which adapts the physical principles for single-ion detection and precise positioning control. It employs a focused ion beam combined with a single-ion detector system which measures the induced charge or the secondary electrons generated by the implantation event, enabling the controlled implantation of individual dopant atoms into a target region [44].

Shinada *et al*. demonstrated the performance increase of a $0.3 \times 3.2\ \mu m^2$ channel transistor with ordered doping distribution with a spacing of 100 nm between each dopant impurity, compared to disordered one [45].

Despite these advances, single-ion implantation faces several challenges. The spatial precision of dopant positioning is typically limited to ~ 10 nm. In addition, lattice damage and low throughput make the technique not practical for large-scale parallel industrial applications.

Hydrogen lithography

Hydrogen lithography represents a surface-based approach that overcomes some limitations of implantation-based techniques by producing a non-Poisson distribution of dopants [46].

It follows a simple scheme in principle which employs hydrogen-resist lithography [12]. Using a scanning probe microscope (STM), individual hydrogen atoms can be removed from a hydrogen-passivated Si surface, creating a hydrogen mask for the exposed reactive Si sites. A dopant precursor gas is then introduced, allowing the dopants to selectively attach only to the exposed Si sites. Subsequent thermal annealing or epitaxial growth incorporates the dopants into the crystal lattice.

This technique has enabled remarkable demonstrations, including the fabrication of single-dopant transistors and single-dopant-wide conductive wires exhibiting ohmic behavior even at the atomic scale [34, 47]. Such top-down surface-mediated approaches offer unparalleled placement precision down to the individual atoms. However, these

techniques require state-of-the art lithography patterning and are incredibly expensive, energy-consuming and with extremely low throughput.

Modulation doping

Modulation doping takes advantage of other concepts by moving completely the position of the dopants away from the channel itself. It represents a non-traditional form of doping that is primarily electronic in nature rather than structural. This results in high carrier mobility because scattering from ionized impurities is reduced [48].

In the context of Si, recent work demonstrated this technique by relocating the dopants outside the Si channel and into the surrounding dielectric. Al atoms embedded in the SiO_2 matrix create acceptor states below the Si valence band. Electrons tunnel from the Si to the acceptor states, thereby injecting holes into the adjacent Si layer without placing dopants inside the lattice itself [32]. This "outsourcing" of dopants to the dielectric avoids diffusion and random dopant fluctuation, reduces surface segregation, and quantum and dielectric confinement effects. Because the active Si remains nominally undoped, ionized impurity scattering is minimized, enabling enhanced carrier mobility even in ultra-scaled geometries.

However, the effective carrier concentration and mobility in the Si channel is intrinsically coupled to the Al dose in the SiO_2, meaning the concentration cannot be independently tuned without impacting mobility. Additionally, the technique requires precise control of the thicknesses of both the spacer and doping layers to maintain optimal charge separation. Finally, thermal processing during fabrication can significantly alter the doping profile, promoting dopant segregation and leading to interface roughness and charge instability.

Spin-on doping

The chemical analogue of conventional diffusion doping is Spin-on doping (SOD). This process involves the spin-coating of a dopant-containing solution onto the semiconductor surface, followed by a rapid-thermal processing (RTP) annealing to diffuse the dopants into the substrate. Often, a pre-diffusion annealing step is required to "glassify" the spin-on dopant layer [49].

SOD is a simple, low-cost, and essentially non-destructive technique, but can suffer from dose-control problems in addition to uniformity issues over large areas or 3D structures. Additionally, while pure SiO_2 and silicates are easily removed via wet etch, SOD often leaves residual organic components from the solvent that can be hard to remove.

Hoarfrost *et al*. improved control over dopant incorporation using a dopant-containing polymer [49]. Unlike traditional SOD, where the dopant-containing layers survive the annealing step, the dopant-containing polymer films employed are easily burned off during the drive-in of the dopants. Additionally, the amount of phosphorus introduced during the doping process was tuned by varying polymer film thickness. Thicker polymer films increased the total amount of P incorporated into the Si substrate.

Chemical-based doping techniques demonstrate the potential concept of surface-mediated dopant delivery, which is refined in monolayer-based approaches.

Monolayer doping

Bottom-up strategies like self-assembled monolayers (SAMs) offer an interesting path to controlled deterministic doping because of the limited cost and intrinsic simplicity of the self-assembing process involved. MLD requires two steps: functionalization of the semiconductor surface with a *p*- or *n*-type dopant-containing molecule, and subsequent diffusion of the chemisorbed dopant atoms into the substrate via RTP.

In 2007, Ho *et al*. proposed a technology based on SAMs of dopant-containing molecules and subsequent diffusion of dopants into the crystal lattice by high-temperature annealing [14]. This bottom-up, nondestructive technique guaranteed uniform and conformal coverage of semiconductor surfaces [50] and it was perfectly compatible with complex 3D structures [51, 52]. Ang *et al*. used MLD to conformally dope a 300 mm wafer by means of a P-based molecule [53]. In addition, they also investigated the application of their process to small feature sizes in 3D FinFET devices, maintaining a defect-free fin doping profile.

One of the major issues associated with these techniques is represented by the difficulty in modulating the amount of dopants deposited on top of the substrate. The surface density of dopants is determined by the steric encumbrance of the molecules carrying the impurities and the number of reactive sites available at the surface. In principle, changing the molecule, the dose of dopants per unit of surface can be properly tuned but requires fine tuning of the graft-to reaction for each different molecule. Moreover, surface preparations and the annealing step must be optimized and tailored to the particular process and material.

Ye *et al*. further evolved the concept of the MLD process through the use of a solution made of a blend of molecules containing the dopant and dopant-free molecules [54]. The control of the dose over more than one order of magnitude was demonstrated, even though the amount of deposited dopants was no more driven by the self-limiting nature of the graft-to reaction, but by the competition of the grafting kinetics of the two different molecules [54].

A common issue of all MLD techniques is the diffusion into the substrate of atoms from the molecules forming the SAM, mainly C, O and N. These contaminants can trap ionized electrons and form pairs with doping atoms which electrically deactivates them [55].

Polymeric precision doping

A step forward in MLD was proposed by Perego *et al*. in their work on polymers end-terminated with a P-containing moiety. These materials, made with a polymeric chain and a reactive terminal containing a P moiety, can be used to obtain a wider range of dopant doses deposited on the substrate compared to MLD following a protocol called polymeric precision doping (PPD) [56].

The graft-to reaction from melt of polymers is driven by the balance of negative free energy of the reaction and the loss of entropy of the system, leading to the creation of a

continuous film of grafted polymeric chains, called brush layer, with a thickness of about two times the gyration radius (R_g) of the polymer [57, 58, 59].

$$R_g = \left(\frac{Nb^2}{6}\right)^{1/2} \tag{1.3}$$

where N is the degree of polymerization, or M_n/M_0, the ratio between the molecular mass M_n and the mass of a single monomer M_0, and b is the statistical polymer segment lengths, the Kuhn length [60]. Grafted polymers can be assumed to have a steric encumbrance comparable to a sphere, with radius similar to the gyration radius. Thus, selecting a specific degree of polymerization N, it is possible to easily tune the steric encumbrance of the grafting polymers and the density of chains per unit of surface [60].

After the graft-to reaction, a mild oxygen plasma ashing allows the selective removal of the polymeric chains, without affecting the P grafted to the surface. Increase of the dose of dopants was demonstrated by repeated grafting/ashing cycles [61]. In principle, it is possible to reach the physical limit given by the number of reactive sites at the Si surface, typically between $10^{14} - 10^{15}$ sites/cm^2.

Finally, upon deposition of a 10 nm thick SiO_2 capping layer, P atoms are efficiently injected into the Si substrate by RTP without the C contaminants typically associated with MLD processes, which were removed by plasma ashing.

These alternative strategies collectively illustrate the evolution of doping from high-energy implantation toward surface-mediated, chemical, and even non-local approaches. Among them, polymeric precision doping offers a unique combination of control, scalability, and process compatibility, making it the focus of my research activity. Recent studies have investigated many aspects associated with this approach, from the nature of the grafting-to reaction to the electrical properties obtained. A more detailed description is presented in section 1.4.

Laser thermal annealing

Laser thermal annealing (LTA) complements the above doping strategies by achieving dopant activation with minimal diffusion. During the process, pulsed laser irradiation locally melts the Si surface, allowing dopant incorporation and activation on nanosecond timescales. Heating amorphous silicon (a-Si) with a laser pulse induces melting followed by epitaxial recrystallization, guided by the orientation of the underlying crystalline template [62]. The extremely short melt duration suppresses long-range diffusion. LTA yields uniform dopant profiles and sharp junctions within the treated region [63] and enhances dopant incorporation and electrical activation [64]. This aspects make LTA particularly suitable for post-implantation or MLD activation.

The maximum amount of dopants that can be incorporated into the crystalline Si lattice before precipitation or clustering is determined by the solid solubility of the element at a given temperature [65]. The segregation coefficient, defined as $k = C_L/C_S$, represents the

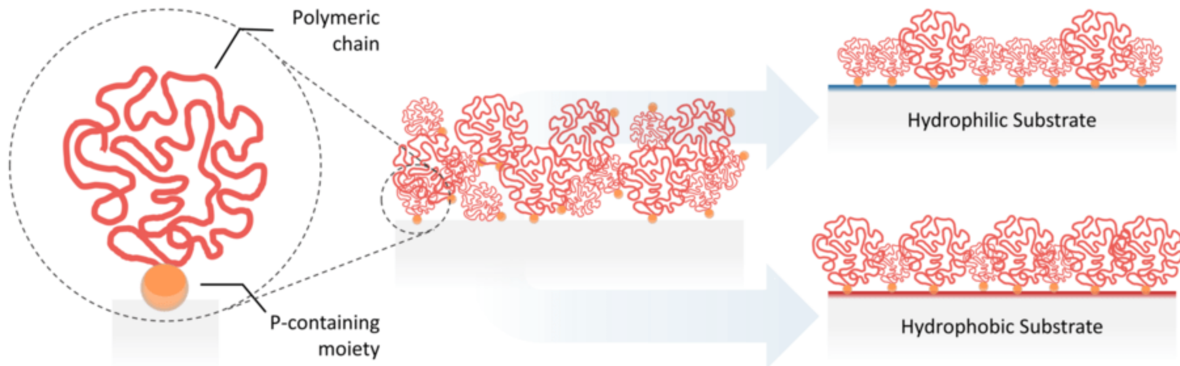


Figure 1.6: Schematic representation of the grafting-to reaction of polymer blends on both hydrophilic and hydrophobic substrates. Image adapted from [67].

ratio between the maximum dopant concentration in the liquid (l-Si) and in the solid (c-Si) phases. For most dopants in Si and Ge, $k > 1$, meaning that the melt can accommodate significantly higher impurity concentrations than the solid phase. Consequently, laser-induced melting transiently allows incorporation of dopants above the equilibrium solid solubility limit, making LTA particularly relevant for hyperdoping and superconductivity applications [66].

1.4 Advances in polymeric precision doping

As discussed in section 1.3, Perego *et al.* proposed P end-terminated polymers, or polymeric precision doping (PPD), as a tool to develop a mild, simple and scalable bottom-up approach for semiconductor doping [60]. The technique relies on the use of self-assembled layers by tailor-made P end-terminated polymers.

The central mechanism to achieve control of the dose is the self-limiting nature of the grafting-to reaction of the polymer chains. The concentration of dopant is finely tuned by adjusting the molecular mass M_n of the grafting polymers (eq. 1.3). This method successfully demonstrated precise control of the P dose on non-deglazed Si (i.e., with the 2 nm native SiO_2 layer on top) between 3×10^{13} and 8×10^{13} cm^{-2} by varying M_n from 2.3 to 25.4 kg/mol [60]. This significantly expands the accessible P dose range compared to classical MLD.

In general, it is difficult to obtain areal dopant concentrations higher than 10^{14} cm^{-2} due to the extremely low M_n required for the dopant polymers. However, it is possible to overcome this drawback by repeating the grafting/ashing cycles. This *multi-cycle approach* extended the dose range of the 2.3 kg/mol polymer to 3×10^{14} cm^{-2} after 5 repetitions [60]. The grafting and injection process of these polymers onto non-deglazed Si surfaces was investigated. It demonstrated the possibility to effectively control the amount of P atoms injected into a bulk Si substrate reaching electrical activation rate (η_a) values larger than

80 % [61, 68]. The η_a values obtained by PPD process are higher than the MLD ones (~ 70 %) [51], and comparable with the ones currently obtained through ion implantation technology.

Despite the success of PPD, the fundamental processes driving the graft-to reaction in the presence of highly polar dopant end-groups and polymer molecular weight dispersity are less understood than that of hydroxy-terminated systems and are subject of ongoing investigation [56, 59]. Current work is focused on understanding the complex surface-polymer interactions. Discrepancies between theoretical models and experimental observation, such as a decreasing P dose over increasing grafting time [69], suggest a dynamic exchange mechanism where short chains initially dominate the surface before being replaced by longer chains. Understanding and controlling this dynamic exchange could provide even greater control of the polymer brushes obtained by grafting to reactions.

Studies have shown that the polarity of the Si substrate surface (hydrophilic non-deglazed native SiO_2 versus hydrophobic deglazed Si) dramatically affects the resulting polymer brush composition and dopant dose [70, 67]. On hydrophilic surfaces, a preferential, rapid adsorption of shorter polymer chains leads to a thin brush with a high P dose. Conversely, on hydrophobic surfaces, this affinity is lost, favoring the grafting of longer chains and lower P dose (Figure 1.6).

Moreover, new techniques in polymer synthesis pave the way to the production of polymers with better control over molecular weight and structure, and the investigation of such complex systems [71].

Considering the current trend in ultra-scaled microelectronic devices, exploitation of PPD required the demonstration of the possibility to apply this technique to perform semiconductor doping of thin films, achieving a uniform doping concentration throughout the entire film and optimized electrical properties. Most of the data that follows were collected during my master thesis and published in the *Materials Science and Semiconductor Processing* journal [38].

Ex-situ doping of deglazed 30 nm thick silicon-on-insulator (SOI) substrates was performed by using poly(methylmetachrylate) polymers with a P containing moiety (PMMA-P), used to create a P δ-layer at the interface between the Si device layer and a 10 nm thick SiO_2 capping layer. Drive-in of the P atoms was performed by annealing the samples in a rapid thermal processing (RTP) system at temperatures (T_A) ranging from 900 to 1200 °C in N_2 atmosphere. Annealing time at each T_A was properly selected to inject into the SOI substrate a constant P dose, computed as the product of n_D and H_{SOI}, of $\sim 1.0 \times 10^{13} cm^{-2}$ and to achieve a uniform dopant concentration throughout the entire Si device layer. After drive-in, the SiO_2 capping layer was removed by a 2-minute bath in a diluted HF solution and circular Al contacts were deposited on the sample using a shadow mask by thermal evaporation. The metallic contacts were placed in a square van der Pauw (vdP) geometry, at the corners of each sample.

A uniform P concentration profile across the Si device layer can be achieved by exploiting P diffusion dynamics in the Si and SiO_2 matrix. Figure 1.7a illustrates the evolution of the

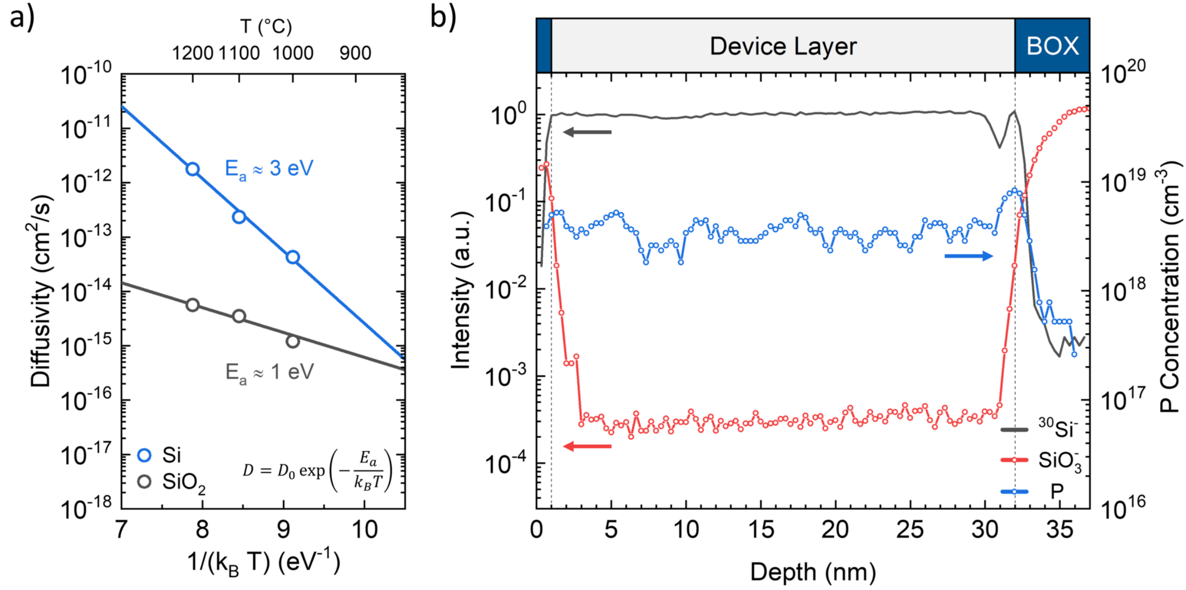


Figure 1.7: (a) Diffusivity values of P δ-layers embedded in a Si (blue) and a SiO_2 matrix (black) [72]. The Arrhenius fit of the data is reported. (b) ToF-SIMS depth profiles upon drive-in of a SOI sample with $H_{SOI} \sim 30$ nm upon drive-in at 1000 °C for 100 s. $^{30}Si^-$ and SiO^{3-} profiles are representative of the SOI structure.

extracted P diffusion coefficient as a function of the inverse of T_A. Crucially, the diffusivity values for P in Si are significantly larger than those available in the literature for P diffusion in SiO_2 considering a P δ-layer embedded into a SiO_2 matrix obtained by a similar protocol by Perego *et al*. [73]. This difference confirms that the SiO_2 layers, both the BOX and the top oxide (TOX) capping layer, effectively act as diffusion barriers. Consequently, P atoms injected into the device layer during annealing are efficiently trapped within the thin Si film. Prolonged thermal treatment contributes to flatten the P depth profile and achieve a uniform concentration throughout the entire device layer.

Figure 1.7b depicts a representative calibrated Time of Flight Secondary Ion Mass Spectrometry (ToF-SIMS) P depth profile of a SOI sample with $H_{SOI} \sim 30$ nm upon drive-in at 1000 °C for 100 s. The profiles of the SiO_3^- and $^{30}Si^-$ secondary ions are representatives of the SOI structure. ToF-SIMS profiles confirm that P atoms are trapped inside the Si device layer, with only a small fraction lost through the Si/SiO_2 BOX interface and that the P concentration is uniform throughout the entire H_{SOI} within the inherent experimental noise and uncertainty of the SIMS measurement.

The correct incorporation of electrically active impurities into the SOI substrate was studied via sheet resistance measurements in vdP configuration. Room temperature Hall measurements and ToF-SIMS were used to determine the free electron dose N_e and the total P dose N_D in the device layer after drive-in, under different annealing conditions, shown

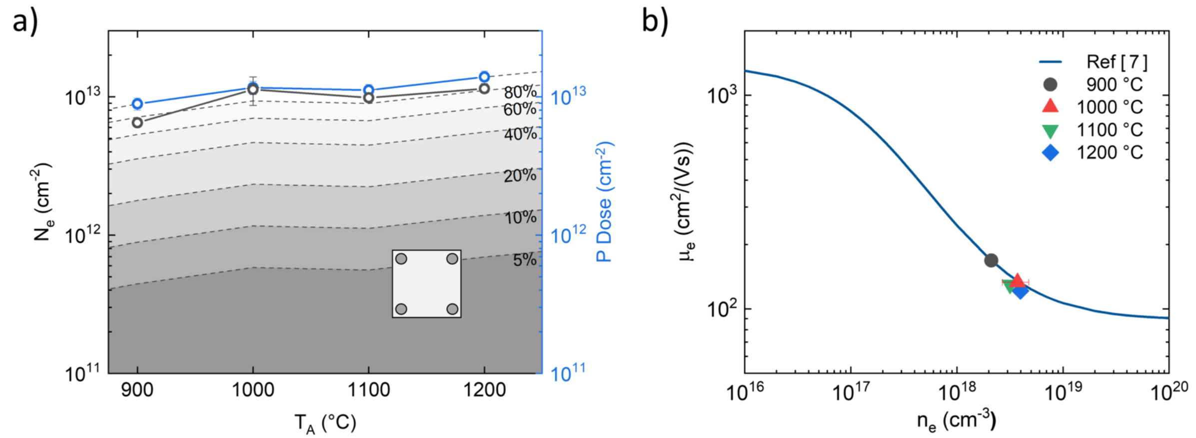


Figure 1.8: (a) The total P dose N_D (blue) and the dose of charge carriers N_e (black) for SOI samples with $H_{SOI} \sim 30$ nm as a function of the temperature of the drive-in process. Dashed lines correspond to η_a values reported. (b) Carrier mobility μ_e as a function of n_e compared to the electron mobility in bulk Si [7].

in Figure 1.8a. η_a was determined from the comparison of electrical and compositional measurements. The highest activation ($\sim$ 100 %) was achieved for samples annealed at 1000 °C for 100 s [38]. At higher temperatures (1100 °C and 1200 °C), η_a decreased to 88.0 % and 83 %, respectively. This deactivation correlated to thermal instability of the BOX at $T_A > 1000$ °C [38]. Oxygen atoms released from the BOX into the device layer can form electrically inactive complexes with the P dopants [68]. Conversely, the lower activation ($\sim$ 72.5 %) at 900 °C was ascribed to the reduced thermal budget of the annealing process, insufficient to fully activate all P atoms.

The calculated carrier mobility (μ_e) (Figure 1.8b) was almost constant through the temperature range of the analysis and is perfectly compatible with mobility values reported in the literature for bulk Si [7]. The low-temperature electrical characterization of a sample annealed at 1000 °C, further demonstrated that the evolution with temperature of ρ, n_e, and μ_e was consistent with that of bulk Si with the same P concentration [38]. High mobility, combined with an average activation rate of $\sim$ 100 % achieved at 1000 °C, demostrated optimal electrical properties of the film and confirmed the efficient and precise incorporation of substitutional P atoms in Si. PPD provides a mild and low-cost alternative to conventional top-down doping approaches and represents a viable solution for the doping of ultrathin film, paving the way to fundamental studies on the electrical properties of these 2D Si nanostructures.

In this work, we combine sheet resistance, Hall and capacitance-voltage (CV) measurements at room temperature to quantify the complex interplay between dopant dose, device layer thickness and processing conditions and the device-relevant characteristics of the SOI substrate, as carrier concentration and mobility. Correlation of these data with dopant

concentration profiles obtained by ToF-SIMS analysis is used to achieve information about effective dopant activation and ionization. Low temperature sheet resistance and Hall measurements are performed to determine activation energy of the dopants as a function of their concentration and device layer thickness and investigate additional quantum related phenomena. By connecting atomistic behavior of dopants with macroscopic characteristics of the semiconductor material, this work aims to lay the foundation of an empirical model for doping of ultrathin Si films in a wide range of concentrations and to inform robust fabrication strategies for next-generation Si technologies.

Chapter 2

Processing and characterization

In this chapter, the experimental methods and tools employed in this work are presented in detail. The chapter is organized into two main sections: one dedicated to the equipment used for *sample preparation* (2.1) and the other focused on the *characterization techniques* (2.2) employed to investigate the properties of the SOI samples.

For each piece of equipment and characterization method, a brief description of its operating principle is provided, highlighting the underlying physics and the type of information extracted. The goal is to provide the reader with a clear understanding of both the methodology and the rationale behind the choice of techniques for this work.

All research activities and instrument characterization, unless otherwise specified, were conducted at the National Resource Council - Institute for Microelectronics and Microsystems (CNR-IMM), laboratories in Agrate Brianza, Italy.

Some parts of this work were carried out during two research periods abroad at the Institute of Applied Physics (IAP) and the Institute of Experimental Physics (IEP) laboratories of the Technische Universität Bergakademie Freiberg, Germany and the Research Institute of Electronics (RIoE) laboratories of the Shizuoka University in Hamamatsu, Japan. The specific equipment used at each institution is detailed within the subsequent sections.

2.1 Sample preparation equipment

This section introduces the tools used to fabricate and prepare the samples for subsequent characterization. The protocol itself will be presented in details in sections 3.1 and 3.2. Each technique is discussed in terms of its principle of operation, key parameters, and how it affects the final properties of the samples. The methods presented include spin coating, rapid thermal processing, plasma etching, vapor deposition, photolithography, contact bonding, and reactive ion etching.

Figure 2.1: SAWATEC SM-150 machine, the spincoater used during this work.

2.1.1 Spin coating

Spin coating is a widely employed technique for the deposition of thin films with uniform thickness onto planar substrates. The process relies on the combined action of radial acceleration (centrifugal force) and hydrodynamic (viscous) forces.

A small, filtered volume of solution is first dispensed onto the center of the substrate, which is held in place by a mild vacuum. Upon high-speed rotation, the centrifugal force causes the liquid to spread uniformly across the surface. As spinning continues, solvent evaporation and outward flow progressively reduce the film thickness until a steady-state is reached. The final film thickness is controlled by the rotational speed, duration, and properties of the solution, specifically its concentration. In general, higher rotational speeds or lower solute concentration yield thinner layers. The solvent used is typically volatile to ensure evaporation during the process [74].

In this work, the deposition parameters were optimized for two sets of materials. For the PMMA-P and PS-P PGMEA solutions, a rotational speed of 2000 rpm for **30** s was employed, producing films approximately $30 - 40$ nm thick. A speed of 6000 rpm for 30 s was used to deposit both hexamethyldisilazane (HMDS) and the AZ5214 photoresist. The spin coating operations were carried out using a SAWATEC SM-150 system (Figure 2.1).

2.1.2 Rapid thermal processing

Thermal processes are widely employed in the semiconductor industry for annealing treatments, dopant diffusion, oxidation, contact formation, defect recovery and related materials

Figure 2.2: Annealsys As-One150 RTP system used in this work (left) and zoom of 4" substrate used as support for diffusion and oxidation on small samples (right).

processing steps. A typical thermal process consists of a temperature ramp-up to the target process temperature (T_A), a soak period at the set point, and a final cool-down. The conventional tube furnace operates under thermal equilibrium, however, its slow heating ramps (a few °C/min) result in a large energy transferred to the sample during the ramp-up and ramp-down stages of the process. Therefore, the thermal budget, defined as the total thermal energy transferred to the sample could be significantly affected. To mitigate this and make ramp times negligible, rapid thermal processing (RTP) systems are employed. RTP operates out of thermal equilibrium, keeping the heating elements, usually an array of infrared halogen lamps, at temperatures much higher than the sample, thereby achieving extremely fast heating ramps.

In this work, all high-temperature thermal treatments were performed using the Annealsys As-One150 RTP system (Figure 2.2a). The chamber was equipped with gas inlets for O_2, N_2, Ar, and forming gas (FG) (5 % H_2 in N_2). Different ramp-up rates were set for each specific process: a rate of 150 °C/s was used for short drive-in treatments to minimize

Figure 2.3: Technics Plasma 300 machine, used for plasma cleaning processes.

ramp-up effects; 50 °C/s for longer rapid thermal oxidation (RTO) treatments; 20 °C/s for the grafting of the polymers and 10 °C/s for FG anneals.

Control of the temperature was achieved using the two infrared optical pyrometers installed in the RTP system, which measure the thermal radiation emitted from the backside of a handle substrate (Figure 2.2b). The low temperature pyrometer, positioned at the edge of the chamber, operates from 100 to 1000 °C while the high temperature pyrometer, positioned at the center of the chamber, operates from 400 to 1300 °C. Each pyrometer operates in a non-contact configuration providing real-time feedback for closed-loop control of the temperature. A fixed emissivity value for Si was used. Each pyrometer was accurately calibrated against a reference thermocouple to ensure measurement consistency and reproducibility.

2.1.3 Plasma etching

Plasma etching is primarily employed to remove carbon contaminants and polymeric residues from the surface of a sample. When used specifically for the removal of organic impurities and carbon-based compounds, the process is referred to as *plasma ashing*. In this technique, an energetic plasma, typically generated from O_2 or Ar gas, is produced by ionizing the low-pressure gas through high-frequency radio waves in the low-pressure chamber (< 1 mbar).

Oxygen plasma ashing is a chemically-driven cleaning process. It effectively and completely removes organic matter, including water vapor and volatile carbon oxides, as the oxygen species selectively attack only organic bonds (as $C-H$, $C-C$). The activated plasma

species, including vacuum-ultraviolet (VUV) photons, are highly effective at breaking these bonds, degrading high molecular weight contaminants. A secondary cleaning action occurs as oxygen species react with organic contaminants to form volatile compounds such as H_2O, CO, and CO_2. These byproducts are evacuated from the chamber, resulting in an ultra-clean surface.

Crucially, oxygen plasma is highly selective and does not affect inorganic contaminants, making it possible to fully remove the polymer layer without significantly affecting the underlying layer and dopant atoms grafted to the Si surface. In contrast, Argon plasma operates as a non-selective, purely physical cleaning method, where energetic Ar^+ ions sputter the surface without inducing chemical reactions.

In this work, plasma cleaning was performed using a 300 Plasma System by Technics Plasma Gmbh, shown in Figure 2.3. The system supports both O_2 and Ar plasma and operates at pressures between 0.2 mbar and 0.8 mbar. All cleaning steps in this study employed O_2 plasma ashing at a fixed power of 40 W, with process durations ranging from 2 to 15 min, tailored to each specific application.

2.1.4 Physical vapor deposition system

Physical vapor deposition (PVD) refers to a class of well-established industrial and research techniques widely employed for the deposition of metallic and dielectric thin films and coatings. In general, a solid source material is vaporized in a high-vacuum environment and subsequently condensed on the substrate surface to form a thin layer. The vacuum conditions ensure a sufficiently long mean free path for the evaporated atoms to travel in straight trajectories toward the substrate without being scattered by the gas molecules. Evaporation of the source material can be achieved through various heating mechanisms, such as resistive heating, radio-frequency induction, or focused electron-beam. Deposition rate is accurately monitored during the process by a quartz microbalance positioned in the proximity of the sample, which can monitor rates on the order of nm/s. Because the quartz microbalance and the sample are at slightly different distances from the source, correct calibration is verified by measuring the final film thickness on test substrates using spectroscopic ellipsometry (Section 2.2.1) or surface profilometry (Section 2.2.2).

Aluminum (Al) and materials with relatively low melting points are efficiently deposited using thermal heating. This simple and cost-effective technique relies on a filament or boat heated by a high current through the Joule effect. Materials with high melting points or prone to thermal or chemical degradation are deposited using electron-beam (e-beam) evaporation. First, a tungsten filament emits electrons via thermo-ionic emission when heated by a high voltage. These electrons are accelerated, focused, and magnetically deflected toward the target material in the crucible, where their kinetic energy is converted into thermal energy, melting and vaporizing the source material.

In this work, Al contacts were thermally deposited using the Auto 306 TURBO PVD system by Edwards (Figure 2.4, left). E-beam evaporation was used to deposit the SiO_2

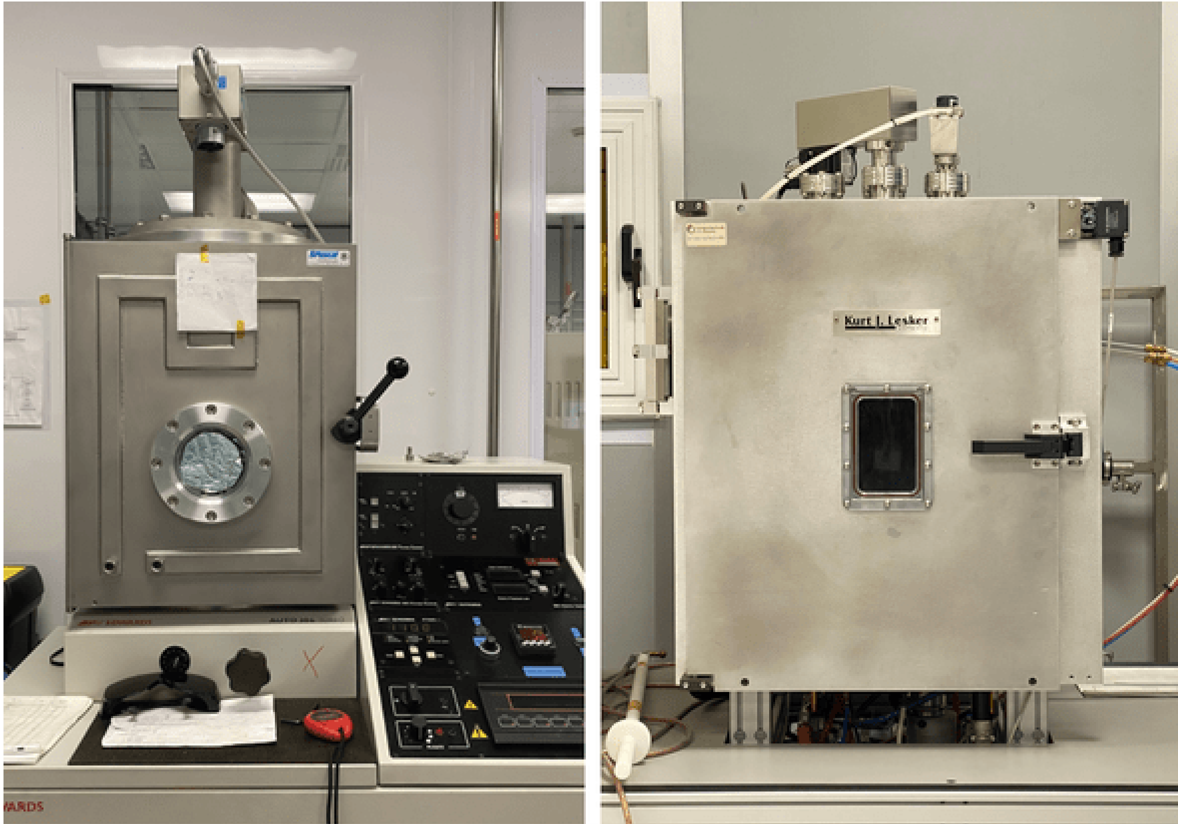


Figure 2.4: (left) Auto 306 TURBO PVD system by Edwards used for Al thermal evaporation. (right) The e-beam evaporator from Kurt J. Lesker used to deposit the SiO_2 capping layer.

capping layer and hard mask on the sample surface and was carried out using a system supplied by Kurt J. Lesker (Figure 2.4, right).

2.1.5 Lithography

Lithography is a patterning technique that enables the transfer of a designed geometry onto a sample by selectively exposing a photosensitive polymer, the resist, to photons (photolithography) or electrons (e-beam lithography, EBL). The exposure modifies the chemical structure of the resist, altering its solubility in a developer solution with respect to the unexposed part. Depending on the resist formulation, exposure can either increase or decrease solubility. In a positive resist, the exposed regions dissolve during development, whereas in a negative resist, the exposed regions become insoluble. After development, a patterned resist mask is obtained, which can be used to define areas for subsequent etching or material deposition. Finally, the remaining resist is removed, leaving the desired pattern

Figure 2.5: Tabletop Maskless Aligner µMLA used for photolithography.

on the substrate.

In this work, optical lithography was performed using the Tabletop Maskless Aligner (µMLA) by Heidelberg Instruments Mikrotechnik GmbH, shown in Figure 2.5. The system employs a 390 nm LED light source and a two-dimensional spatial light modulator (SLM) to project the pattern directly onto the sample surface. During exposure, the substrate is moved by a precision motion stage under the optical unit, which dynamically reproduces the designed pattern without the need for a physical photomask. This maskless configuration eliminates the alignment and fabrication constraints associated with conventional chrome-on-glass photomasks. The design of the mask was carryed out using the KLayout software.

The resist employed was the commercial AZ5214, a reversal photoresist that can be processed in either positive or negative tone, depending on the exposure and baking conditions. Every process is achieved using the positive tone. The process is shown in Figure 2.6 and detailed as follows.

- **Cleaning:** at the beginning of the process, the surface of the sample was prepared by cleaning in acetone and isopropanol. The samples were then dehydrated on a hotplate at 120 °C for 4 min to improve resist adhesion.

- **Spin-coating:** the sample surface was covered with the resist, spincoating the AZ5214 photoresist on the sample at 6000 rpm for 30 s to obtain a 1 µm thick uniform layer.

- **Baking:** the sample was baked on the hotplate at 90 °C for 1 min in order to completely dry the resist layer.

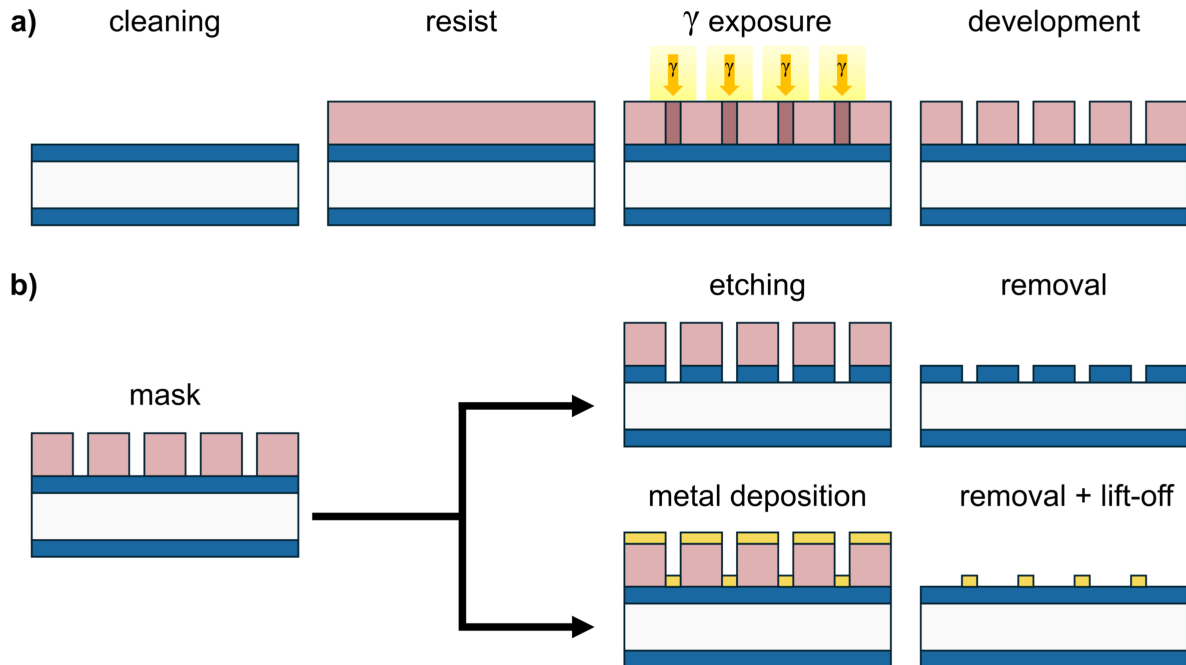


Figure 2.6: (a) Schematic description of the photolithographic process and (b) the typical two possible next steps, etching or metal deposition.

- **Exposure:** the desired pattern was printed on the sample surface by means of maskless photolithography.

- **Development:** The exposed regions were removed by immersing the sample in a specific buffered alkaline solution, the AZ400K developer, for a duration of 40 s to 1 min.

- **Processing step:** (Figure 2.6b) at this point, the two steps following the lithographic process were chemical etching of the material or metal deposition. In the case of wet chemical etching in hydrogen peroxide (KOH), a hard bake at 120 °C for 3 min was applied to improve the mechanical stability of the resist.

- **Resist removal:** at the end, the resist left on the surface of the sample is dissolved by soaking in acetone. In the case of metal deposition, removal of the resist in acetone causes the metal deposited on top to be lifted-off together with the resist. The lift-off process was assisted by gentle heating or solvent agitation using a syringe.

- **Cleaning:** Finally, the samples were rinsed with isopropanol (IPA) and dried under N_2 flow.

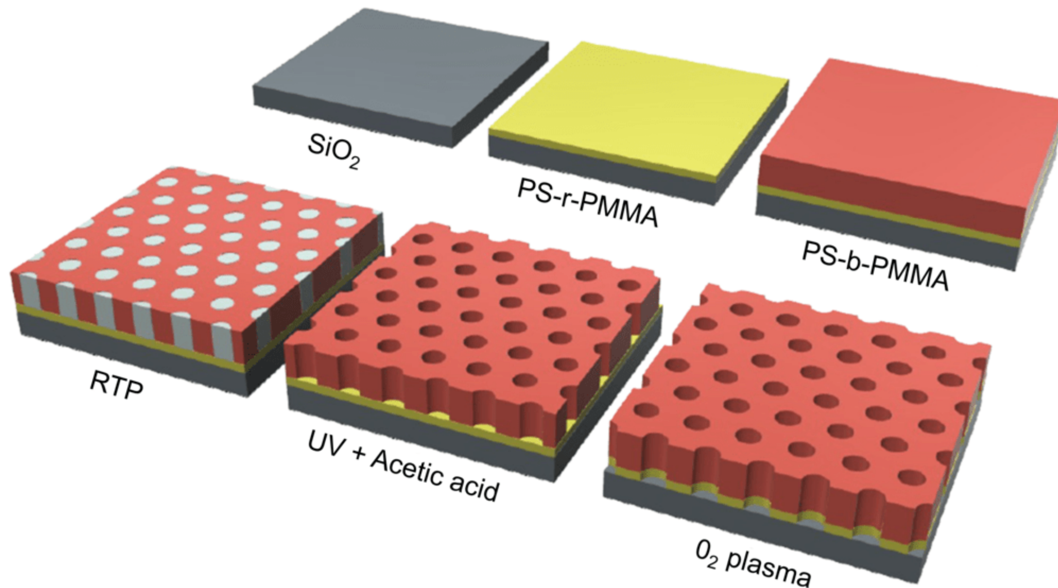


Figure 2.7: (a) Schematic representation of the process flow for the deposition of the PS-b-PMMA mask.

Block copolymer lithography

Whenever periodic patterning at the nanoscale over large areas is required, block copolymer (BCP) lithography provides an extremely attractive alternative to conventional top-down techniques. BCPs offer a lower-cost alternative to optical lithography and higher-throughput than serial processes, as EBL, route to generate sub-20 nm features over wafer-scale surfaces.

A linear di-block copolymer consists of two chemically distinct linear homopolymer chains covalently bonded at one end. When annealed above the glass transition temperature they spontaneously microphase separate generating a variety of periodic nanostructures with a characteristic domain spacing (L_0) typically between 10–100 nm. The phase separation and the resulting morphology, cylindrical, lamellar, or spherical, is determined by the interaction between the two different polymers [75]. It depends on the volume fraction of each block (f_A) and the product χN, where χ stands for the Flory–Huggins interaction parameter and N is the degree of polymerization of the BCP. By appropriately tuning these parameters, ordered nanostructures suitable for lithographic patterning can be achieved [76, 77].

Among BCP systems, polystyrene-block-poly(methylmethacrylate) (PS-b-PMMA) is one of the most widely used due to its well-established processing and the ability to form vertically oriented PMMA cylinders within a PS matrix through simple thermal annealing. The similar interfacial energies of the two blocks with air ($\gamma_{PS-air} \sim \gamma_{PMMA-air}$) result in a neutral interface which prevents film dewetting during the self-assembly process. However, due to the preferential affinity of PMMA with SiO_2, the neutralization of the substrate is

necessary to obtain the right alignment of the domains. This is achieved by functionalizing the substrate with a brush layer of a random copolymer (PS-r-PMMA) -OH terminated, prior to BCP deposition [78].

The complete process flow for the preparation of the PS-b-PMMA lithographic mask is illustrated in Figure 2.7. First, a thin PS-r-PMMA film is spin-coated onto the SiO_2 surface. Grafting and formation of the brush layer is achieved by annealing at 210 °C for 900 s in N_2, followed by sonication in PGMEA to remove unbound chains. A PS-b-PMMA film is then spin-coated on top and thermally annealed at 190−250 °C for 600 s to induce the self-assembly process. During this step, PMMA domains organize into a hexagonal array of vertically aligned cylinders within the PS matrix. Selective removal of PMMA is performed by ultraviolet (UV) exposure in air, which preferentially degrades the PMMA phase. Immersion in acetic acid subsequently dissolves the degraded PMMA, yielding a nanoporous PS film. A mild O_2 plasma treatment (3 min, 40 W) removes the residual random copolymer and fully opens the pores to the underlying SiO_2 layer. The resulting PS mask provides a highly uniform, hexagonally ordered pattern suitable for transfer by reactive ion etching (RIE) into the underlying Si film.

BCP lithography enables large-area patterning with periodicity down to ∼ 10 nm, compatible with standard Si processing, as integrated with ultra-low energy ion implantation [79]. Its combination of scalability, precise control over nanoscale morphology, and low cost makes it a powerful approach for creating honeycomb lattices in ultrathin Si films.

2.1.6 Contact bonding

Because of the small size of the devices and Al contacts patterned with the resist mask, it was necessary to bond the sample onto a chip carrier or puck to perform electrical measurements and investigate the transport characteristics. The introduction of wire bonding ensures high reliability and minimizes the contribution of contact resistance.

In general, to interconnect the metal contacts deposited on the sample surface to external leads, two common wire bonding techniques are used: Al *wedge bonding* and gold (Au) *ball bonding*. In Al wedge bonding, the 25 µm thick Al wire is pressed and ultrasonically vibrated onto the electrode surface, creating a cold-welded joint. In Au ball bonding, the Au wire is heated and melted at the end of a small capillary tip to form a small ball, which is then both thermally and ultrasonically bonded onto the contact pad. A second wedge bond completes the interconnection to the leads. Typically, Au ball bonding is more compatible in the case of gold contacts.

In this work, Al wedge bonding was employed to connect the Al electrodes to the sample holder. Two different instruments were employed. A 5332 Ball-Deep Access (DBA) bonder by F&K Devoltec Semiconductor GmbH installed at the CNR-IMM laboratories (Figure 2.8) and a TPT HB05 manual wire bonder installed at the IAP laboratories.

Three types of chip carriers were employed to connect the samples to the relative measurement setups. A schematic of the device structure and bonding configurations of the

Figure 2.8: F&K 5332 BDA bonder installed at the CNR-IMM labratories.

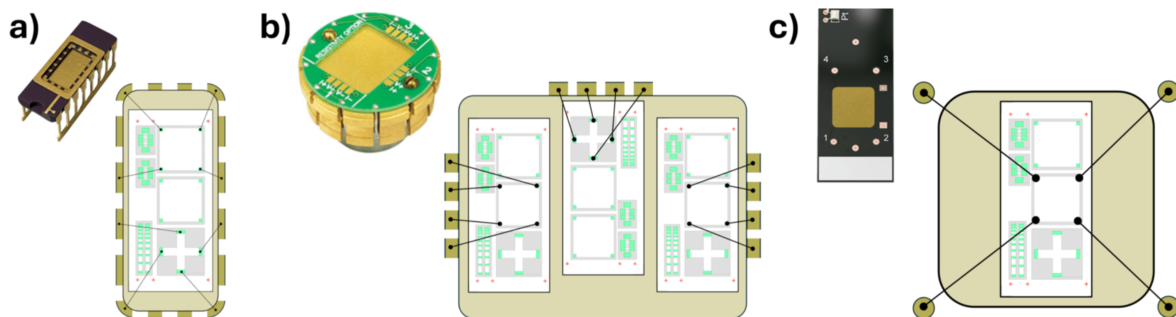


Figure 2.9: Schematic of the device structure and bonding configurations of the chip carrier used at the CNR-IAP laboratories (a), IEP laboratories (b) and IAP laboratories (c).

Al contacts (green) to the Au leads (gold) of each chip carrier is shown in Figure 2.9.

Figure 2.9a is used for measurements at the CNR-IMM laboratories. Figure 2.9b is used for the measurements performed at the Physical Properties Measurement system (PPMS) installed at the IEP laboratories. Figure 2.9c for the measureready FastHall setup at the IAP laboratories. More details about each measurement setup are presented in section 2.2.

2.1.7 Reactive ion etching

Reactive Ion Etching (RIE) is a plasma-based dry etching technique which enables the selective removal of material from the surface of a substrate. Low-pressure gas is introduced

Figure 2.10: RIE instrument installed at the INRIM laboratories.

in a vacuum chamber and ionized by an RF electromagnetic field. Two competing mechanisms provide etching of the substrate. First, the resulting plasma contains reactive ions and radicals, which chemically react with the surface to form volatile products. Second, accelerated ions bombard the substrate and physically sputter and directionally etch the surface. The combination of chemical and physical etching enables high selectivity and highly anisotropic trenches. The processing parameters, as the chemical composition of the gas, chamber pressure, RF power, and substrate bias control the etching rate, depth profile, and selectivity.

The versatility of the chemistry makes RIE suitable for a wide range of materials, from semiconductors to dielectrics and polymers. In combination with a lithographic mask, RIE allows precise and controlled pattern transfer to the underlying substrate, making it a key step in micro- and nanofabrication.

In this work, the pattern transfer of the BCP mask pattern onto the substrate surface was performed in a PlasmaPro 100 Cobra 300 ICP by Oxford Instruments Plasma Technology, shown in Figure 2.10 installed at the National Metrology Institute of Italy (INRIM) laboratories in Turin, Italy. Two chemistries were used depending on the material to be etched. SiO_2 etching was achieved by CHF_3/Ar RIE with a power of 35 W. Si etching was achieved following a pseudo-Bosch protocol by $CHF_3/SF_6/C_4F_8$ RIE with an ICP plasma power of 750 W and an RF table power of 35 W. The RIE processes were carried out with the help of Dr. Irdi Murataj.

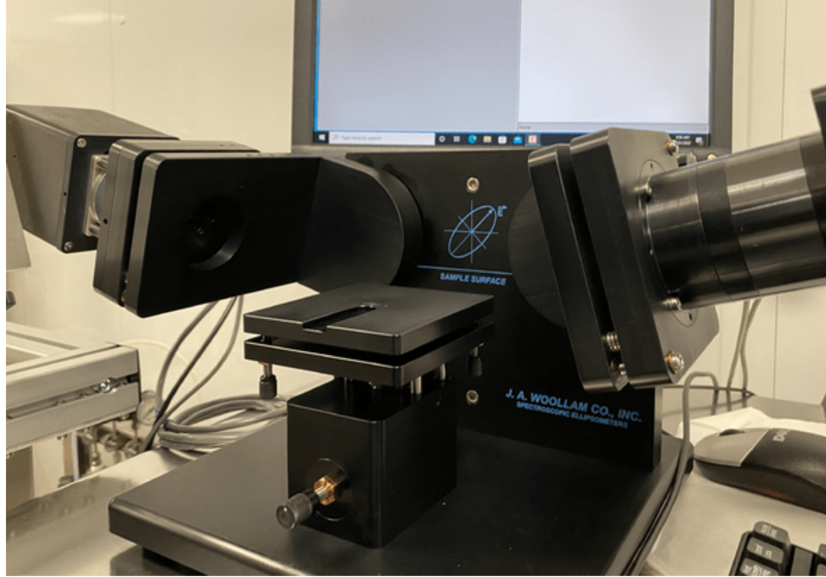


Figure 2.11: M-2000F spectroscopy ellipsometer apparatus used in this work.

2.2 Characterization techniques

This section presents the characterization methods used to analyze and quantify the properties of the fabricated SOI samples. For each technique, the main operating principle and the type of information obtained are outlined. The techniques discussed include spectroscopic ellipsometry (SE), surface profilometry, scanning electron microscopy (SEM), time-of-flight secondary ion mass spectrometry (ToF-SIMS), electron paramagnetic resonance (EPR), charge transport measurements, capacitance-voltage and current-voltage characterization.

2.2.1 Spectroscopic ellipsometry

Ellipsometry is a non-destructive optical technique employed to characterize the optical properties, film thickness and dielectric constants of a various range of materials. Ellipsometry is particularly sensitive for reflective materials as it quantifies changes in the polarization state of light upon its reflection from the material. Typically, the incident light passes through a linear polarizer, undergoes a change in polarization and is reflected from the sample at a specific angle elliptically polarized, hence the name of the technique. The change in the polarization is measured by an analyzer, coupled with a detector.

The difference of polarization of the reflected light is described in terms of the phase difference Δ, and the ratio between the amplitude of the incident and reflected wave Ψ.

$$\rho = \tan(\Psi) e^{i\Delta} \tag{2.1}$$

This difference in polarization is given by the boundary conditions of Maxwell's equations at each interface and at the surface of the sample.

In monochromatic ellipsometry, a single pair of Ψ and Δ values can be determined for a single wavelength of the light at a single angle of incidence, allowing at maximum two parameters to be determined from the measurement, for example, the film thickness H and the refractive index n. Spectroscopic ellipsometry (SE), on the other hand, yields a pair of Ψ and Δ for each employed wavelength, significantly expanding the number of complex properties that can be independently determined.

The Ψ and Δ curves typically do not provide quantitative information about the properties of the sample. Film thickness and optical constants are determined through regression analysis, adjusting the model calculations to fit the experimental data by refining any unknown properties of the sample. SE is widely used for the characterization of thin transparent films, provided that an appropriate optical model is used, especially for very thin or multi layer films. The quality of the fit is measured by means of root mean square error (MSE) between the model-generated and measured Ψ and Δ data values. For thicker and multi layer films typically MSE values fall within the range of 10–20. In the case of polymeric materials, being simple and transparent dielectrics, a Cauchy layer is added on top of the SOI stack. The reflective index is described using the Cauchy formula [80].

$$n(\lambda) = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^4} \tag{2.2}$$

where A, B, and C are fitting parameters.

In this work, a M-2000F rotating compensator ellipsometer by J. A. Woollam Co. Inc. is used (Figure 2.11). The probing light is a spectroscopic light from an Xe arc lamp. A Si detector is used. Acquisition is performed at fixed 75° incidence angle. The analysis and fitting is performed using the EASE software package, by J.A. Woollam Co. Inc.. The SOI was modelled as four layer: cristalline Si from the handle wafer, SiO_2 from the BOX, cristlline Si from the device layer, and SiO_2 from the capping TOX, all fitted using the default models of the software. Precise details about these models can be found in literature [81].

2.2.2 Surface profilometry

Profilometry is a technique used to extract topographical information from the surface of the samples to investigate surface morphology, step heights, and surface roughness. Two main types of surface profilometers are commonly used, differing for the type of detector, mainly a stylus or optical, which uses light instead of a physical probe.

In this work, a stylus alpha-step 500 surface profilometer by Tencor Instruments (Figure 2.12) was used to perform line scans across the surface of the SOI samples after etching and metal deposition. Stylus profilometers acquire step height information of features by physically moving a probe tip along the surface of the sample. A mechanical feedback loop monitors the force from the sample pushing up against the probe as it scans along. The changes in the Z position of the arm holder are used to reconstruct the surface.

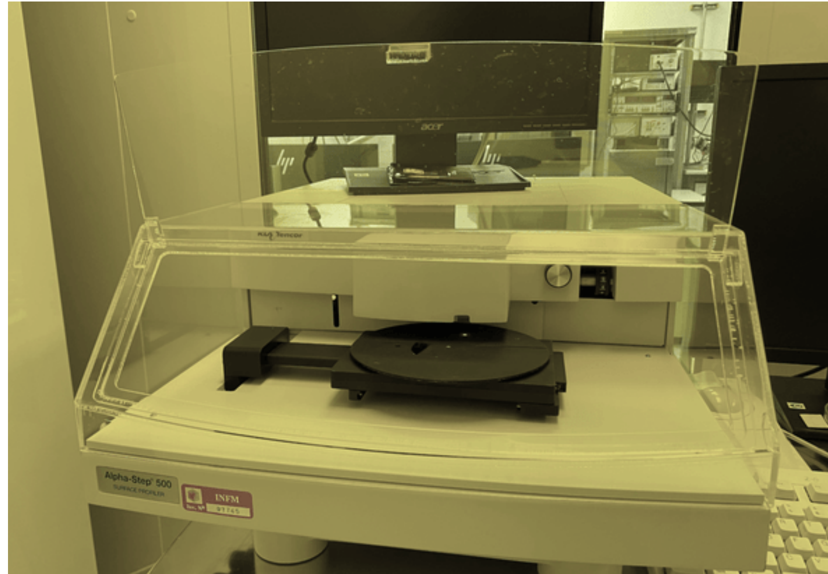


Figure 2.12: Alpha-step 500 surface profilometer used in this work.

Stylus profilometry provides high Z resolution and accurate measurements. However, the stylus tip size and shape can influence the lateral resolution of the measurement. Necessary contact makes it sensitive to contamination and soft surfaces and can be destructive. Because substrate curvature can affect the apparent step height extracted, a baseline correction was applied to each measurement to account for substrate bow and improve the accuracy.

2.2.3 Scanning electron microscopy

Scanning electron microscopy (SEM) is an advanced imaging technique employed for the high-resolution analysis of the surface of materials. SEM utilizes a focused electron ion beam for imaging. The electrons are produced via thermal emission from a heated source or extracted from a sharp tip under high electric fields in the case of field-emission SEM (FE-SEM). The electron beam is focused and scanned across the surface of the sample, line by line. As the incident electron beam interacts with the specimen, it induces the emission of electrons through elastic and inelastic scattering events occurring at and near the surface. The emitted electrons at each specific position are then collected by a detector.

Inelastic scattering arises from interactions between the incident electrons and the electrons within the specimen, leading to ionization and excitation. The relaxation of these excited states results in the emission of low-energy secondary electrons. Secondary electrons originate from only a few nanometers beneath the surface and provide excellent topographical contrast and high spatial resolution. Elastic scattering occurs when incident electrons are deflected by atomic nuclei or outer-shell electrons without significant energy loss. The

Figure 2.13: SEM-FEG Zeiss Supra 40 used in this work.

electrons are backscattered out of the specimen and retain most of their initial energy. Their intensity depends on the mass of the nucleus they interact with, making them useful to represent the mass contrast of the specimen surface [82].

In this work, a SUPRA 40 FE-SEM by Zeiss (Figure 2.13) was used to characterize the quality of the pattern transfer of the BCP polymeric mask to the Si device layer and verify the quality of the fabricated devices. Imaging was performed using an in-lens detector, a tungsten source and an acceleration voltage of 15 kV. Multiple SEM images from various areas of each sample were acquired and analyzed.

2.2.4 Time of flight-secondary ion mass spectrometry

Time-of-flight secondary ion mass spectrometry (ToF-SIMS) is a surface-sensitive mass spectrometry technique. A primary ion beam sputters the surface. Secondary ions are ejected during the interaction between the beam and the sample, and they are collected and analyzed using a time-of-flight analyzer. From the mass/charge ratio of secondary ions, it is possible to determine the elemental, isotopic, or molecular composition of the surface to a depth of ~ 1 nm. ToF-SIMS is one of the most surface-sensitive techniques, granting an elemental detection limit ranging from parts per million to parts per billion. To obtain a compositional depth profile of the sample, each analysis cycle is preceded by the emission of a focused ion beam that sputters the surface, removing part of the material. Using this procedure, each sputtering/analysis cycle collects information at different depths, making it possible to study the composition of the specimen as a function of the depth from the

Figure 2.14: M6 IONTOF apparatus used for ToF-SIMS analysis.

surface, with a resolution close to ~ 2 nm.

Due to the inherent SOI structure, measurements performed on the samples required charge neutralization which was achieved using a flood gun. This electron source provides a steady flow of low-energy electrons to the target. The process is calibrated to balance the charge by ensuring each impinging flood gun electron knocks out a secondary electron from the target, preventing surface charging and maintaining a steady potential during measurement.

Secondary ion intensity is highly sensitive to the local chemical environment, a phenomenon known as the matrix effect. This effect causes significant variations in the ionization probability of elements, particularly at abrupt interfaces, leading to an out-of-equilibrium emission of secondary ions. For this reason, quantitative measurements can be obtained only in a homogeneous matrix. To obtain quantitative P concentrations it is mandatory to compare the signals with reference samples. The ToF-SIMS counts were converted into atom concentrations (in atoms/cm^3 or simply cm^{-3}) following a calibration protocol described in the literature [83]. Specifically, the P^- secondary ion signal was normalized to the $^{30}Si^-$

secondary ion signal, in order to eliminate the dependency of the measured counts on the analysis gun current. The normalized P signal was then calibrated using a relative sensitivity factor (RSF) determined from a set of samples implanted with P at the same energy but different doses, verifying linearity of the calibration over a broad concentration range. Therefore, the P concentration is directly measured from calibrated depth profiles as the average value in the Si matrix, excluding the peaks at the TOX and BOX SiO_2 interfaces. The total P dose (in atoms/cm^2 or simply cm^{-2}) can be readily obtained by integrating the calibrated signal.

In this work, ToF-SIMS measurements were carried out using dual-beam ION-TOF M6 system operating in negative polarity with cesium Cs^+ ions for sputtering and bismuth Bi^+ ions for analysis. The sputtering was performed over a 500 × 500 μm^2 area using Cs^+ ions, while Bi^+ ion beam was used for analysis. Depth scale calibration was performed by individually measuring the sputter rate for each SOI sample. The Si/SiO_2 interfaces were identified by the intensity spikes in the ^{30}Si signal, while H_{SOI} was accurately determined by SE. The error on each measurement was assumed to be around ∼ 10% of the concentration measured from calibrated depth profiles. The minimum P concentration that could be discriminated from the background of the instrument, $n_{D,min} \sim 1 \times 10^{17}$ cm^{-3}, was directly measured in a lowly doped bulk Si substrate.

2.2.5 Electron paramagnetic resonance

Electron paramagnetic resonance (EPR), or electron spin resonance (ESR), is a spectroscopy technique to address the paramagnetic spin states in materials. In semiconductors, it provides insight into dopants, both shallow and deep, defect centers, and localized electronic states.

When a static magnetic field B_0 is applied, the electron levels of the spin states $\pm 1/2$ split due to the Zeeman effect. The energy separation ΔE is proportional to B_0.

$$h\nu_{\mu w} = \Delta E = g\mu_B B_0, \tag{2.3}$$

where h is the Planck constant, $\nu_{\mu w}$ is the microwave frequency, g is the Landé g-factor, and μ_B the Bohr magneton. Continuous wave EPR (cw-EPR) experiments are performed using a fixed microwave source at a given frequency $\nu_{\mu w}$ and sweeping the magnetic field. Resonance occurs when the microwave energy matches ΔE [84]

In this work, cw-EPR measurements were performed using a Varian E15 EPR spectrometer operating in the X-band ($\nu_{\mu w} \approx 9.4$ GHz). For $g \approx 2$, the resonance field B_0 is around 335 mT. The sample was placed in a EF4122sHQ Bruker super high-Q cylindrical cavity, positioned between electromagnets generating static fields up to 1 T, with a minimum step of 0.01 mT. For low-temperature measurements, the cavity was housed in an ESR900 flow cryostat by Oxford Instruments, allowing measurements down to 4.2 K using liquid helium (Figure 2.15).

The reflected microwave, modified by the absorption under resonance, is detected and converted into current by a Schottky diode detector. The output is amplified and processed through a SR830 DSP dual-phase lock-in amplifier by Stanford Research for phase-sensitive

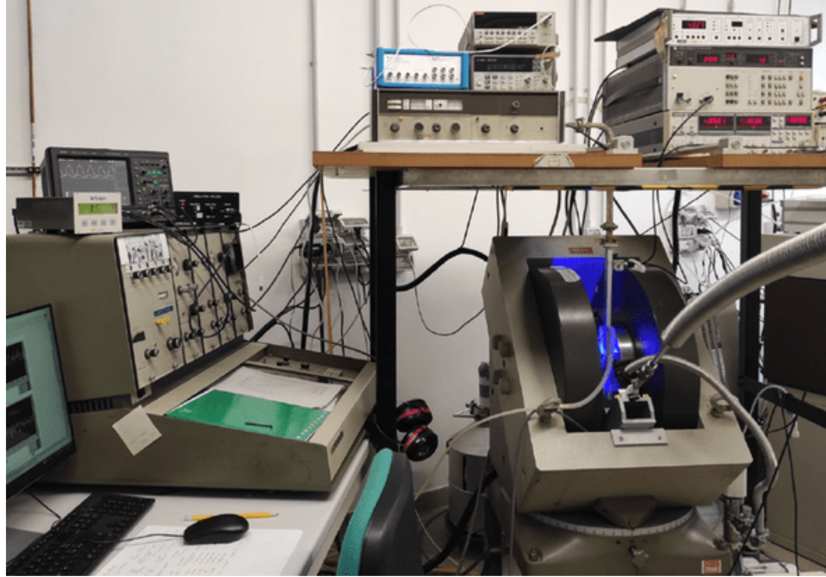


Figure 2.15: EPR setup used in this work, installed in the UNIMIB laboratories.

detection. A small AC magnetic field modulation B_{mod} of ~ 100 kHz, was superimposed on B_0, enhancing sensitivity by filtering out of other signals coming from noise and background. The resulting spectrum corresponds to the first derivative of the absorption line [85]. Power saturation curves were recorded for representative samples by varying the microwave power between 1 and 60 mW to ensure all measurements were performed in the linear regime. A microwave power of 1 mW was selected for the characterization of the samples. g-factors were calibrated using the standard $\alpha, \alpha' - \text{diphenyl} - \beta - \text{picryl hydrazyl}$ DPPH signal with $g = 2.0036$.

EPR spectra were analyzed and fitted with the MATLAB toolbox EasySpin, using the `pepper` function, in order to extract the g-factors and linewidths of the detected paramagnetic species [86]. EPR signals were fitted considering a normalized Lorentzian absorption lineshape centered at B_0:

$$f_L(B) = \frac{2\pi\sqrt{3}\,\Gamma}{1 + 4\left(\frac{B - B_0}{\Gamma}\right)^2} \tag{2.4}$$

where Γ represents the peak-to-peak distance and it is related to the full width at half maximum (FWHM) via $\Gamma = \text{FWHM}/\sqrt{3}$. The g-factors were extracted from B_0 according to eq. 2.3. The fitted signal intensity, intended as the absolute amplitude, were extracted by the fitting procedure. Finally, the quality of the fit was valued in terms of MSE, describing the deviation of the experimental from the simulated spectrum. EPR measurements as well as the fitting of the extracted parameter were all performed by Dr. Fabiana Taglietti of the University of Milan-Bicocca (UNIMIB).

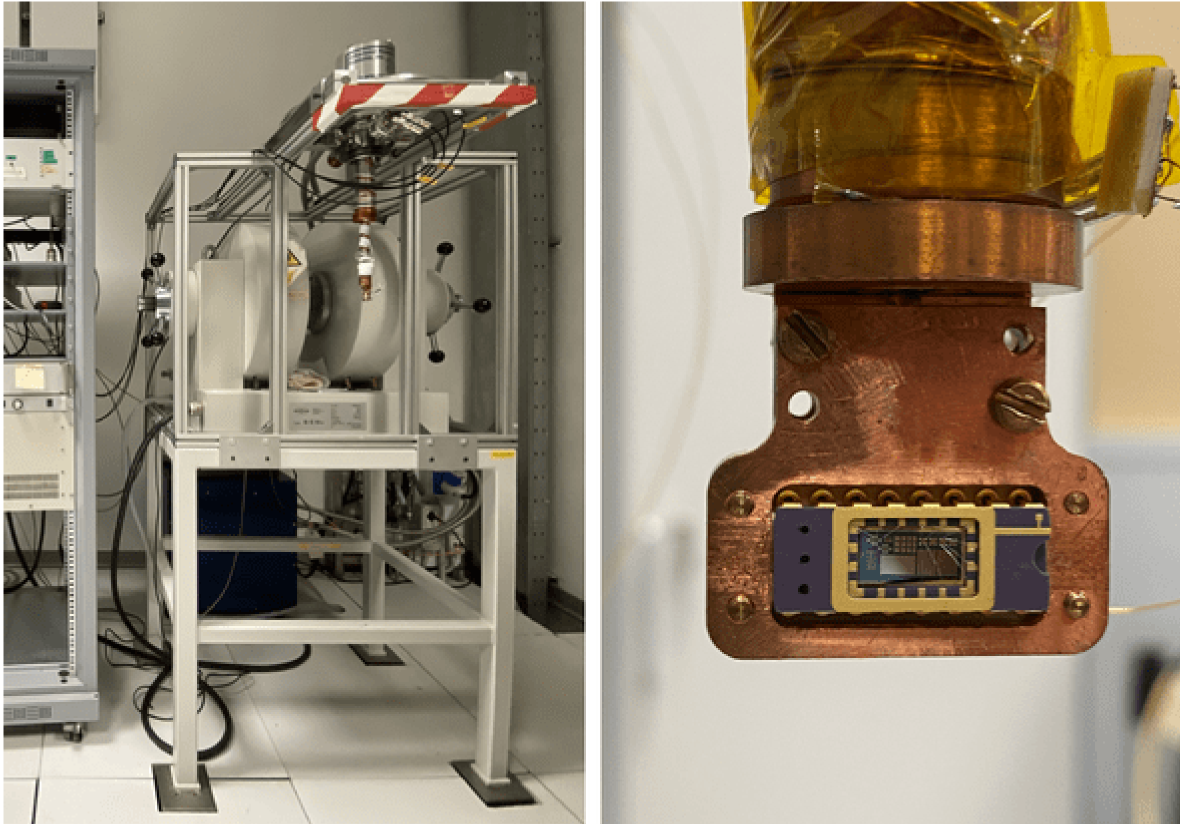


Figure 2.16: (left) Electrical measurements setup. (right) Zoom of a sample bonded to the chip carrier and mounted on the electrical apparatus.

2.2.6 Charge transport measurements

In this section, I provide a brief description of the physical phenomena involved in charge transport and magnetotransport measurements. The electrical measurements involve the extraction of sheet resistance, free carrier concentration, and mobility as well as their evolution with temperature and magnetic field.

The electrical setup used in this work (Figure 2.16), is equipped with a Keithley 6221 current generator, a Keithley 2182 voltmeter, a Bruker BE15 magnet, and a homemade matrix used to invert the current polarizations and its injection contacts. The magnetic setup is also equipped with a cryostat to perform temperature-dependent Hall measurements from 5 to 300 K.

The resistivity ρ of a semiconductor depends on the free electron and hole densities (n_e and n_h), and the electron and hole mobilities (μ_e and μ_h). In an n-type semiconductor, there is only one type of majority carrier responsible for the charge transport, the electrons since

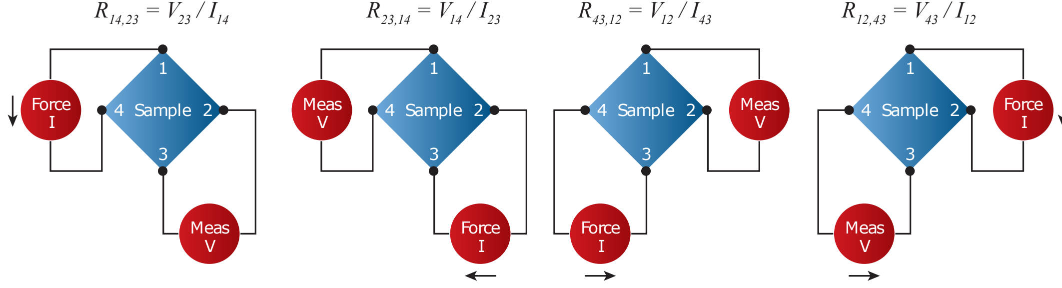


Figure 2.17: Probe configurations for sheet resistance measurements in 4PP vdP configuration [87].

$n_e \gg n_h$ [7].

$$\rho = \frac{1}{q(\mu_e n_e + \mu_h n_h)} \approx \frac{1}{q\mu_e n_e}, \tag{2.5}$$

where $q = 1.602 \times 10^{-19}$ C is the elementary charge.

Resistivity is not directly measurable. However, if a sample is uniform and of constant thickness as in the case of the device layer of SOI, the resistivity can be derived from the sheet resistance R_s and H_{SOI}.

$$\rho = R_s H_{SOI}, \tag{2.6}$$

R_s, in $\Omega/\square$ (ohms per square), is the measured two-dimensional resistance of a thin film, nominally uniform in thickness. For non-uniformly doped samples, the sheet resistance depends on resistivity and mobility at different depths [7]. The most common method for measuring sheet resistance of a thin sample is the four-point probe (4PP) van der Pauw (vdP) method [88]. In this method, four ohmic contacts are placed on the sample boundary. For a square sample, the probes are typically placed at the four corners (Figure 2.17). Current is injected between two adjacent contacts (I_{ij}) and the voltage across the opposite contacts (V_{kl}) is measured to extract the relative resistance ($R_{ij,kl} = \frac{V_{kl}}{I_{ij}}$).

Van der Pauw showed that R_s can be determined from two resistances measured along perpendicular edges, vertical (R_v) and horizontal (R_h). Repeating the measurements in the reciprocal and reverse polarity greatly improve accuracy:

$$e^{-\pi R_v/R_s} + e^{-\pi R_h/R_s} = 1 \tag{2.7}$$

$$R_v = \frac{R_{12,34} + R_{34,12} + R_{21,43} + R_{43,21}}{4}, \qquad R_h = \frac{R_{23,41} + R_{41,23} + R_{32,14} + R_{14,32}}{4}$$

The vdP equation is generally solved numerically. In this work, the Newton-Raphson method was used, repeated until $|R_s^+ - R_s|/R_s^+ < 10^{-6}$ [89].

$$R_s^+ = R_s + \frac{R_s^2(1 - e^{-\pi/R_s}R_v - e^{-\pi/R_s}R_h)}{\pi(R_v e^{-\pi/R_s}R_v + R_h e^{-\pi/R_s}R_h)}. \tag{2.8}$$

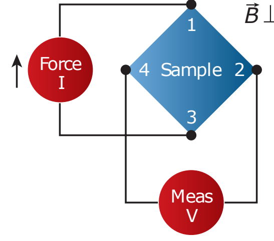


Figure 2.18: Probe configurations for Hall effect measurements in 4PP vdP configuration [87].

R_S (and ρ) does not provide a direct measurement of carrier concentration and mobility individually (eq. 2.5). To obtain information of these quantities, Hall effect measurements are performed. The Hall voltage V_H arises from the Lorentz force when the sample is introduced in a perpendicular magnetic field.

$$V_H = \frac{R_H B I}{H_{SOI}}, \tag{2.9}$$

where R_H is the Hall coefficient. In the case of *n*-type samples:

$$R_H = -\frac{r_H}{q n_e} = -\frac{1}{q n_e}, \tag{2.10}$$

where r_H is the Hall scattering factor and is usually assumed to be equal to 1 [90]. For uniform carrier mobility and uniformly doped SOI samples:

$$R_H = \frac{H_{SOI}}{q \int_0^t n(x) dx} = \frac{H_{SOI}}{q N_e}. \tag{2.11}$$

In our measurements, the magnetic field was scanned from −0.8 T to +0.8 T. At each field, four measurements were performed by switching the current direction and the measurement terminals to improve the accuracy. The slope m of V_H versus B gives the total carrier density N_e (in cm^{-2}):

$$m = \frac{V_H}{B} = -\frac{I}{q N_e} \tag{2.12}$$

Once N_e is known, mobility is obtained:

$$\mu_e = \frac{1}{e N_e R_s}. \tag{2.13}$$

Assuming a uniform conductive layer with a thickness H_{SOI}, the average carrier concentration n_e is determined:

$$n_e = \frac{N_e}{H_{SOI}} \tag{2.14}$$

In this work, two other setups were used to perform electrical characterization at the IAP and IEP laboratories in Freiberg, Germany. Room temperature measurements were

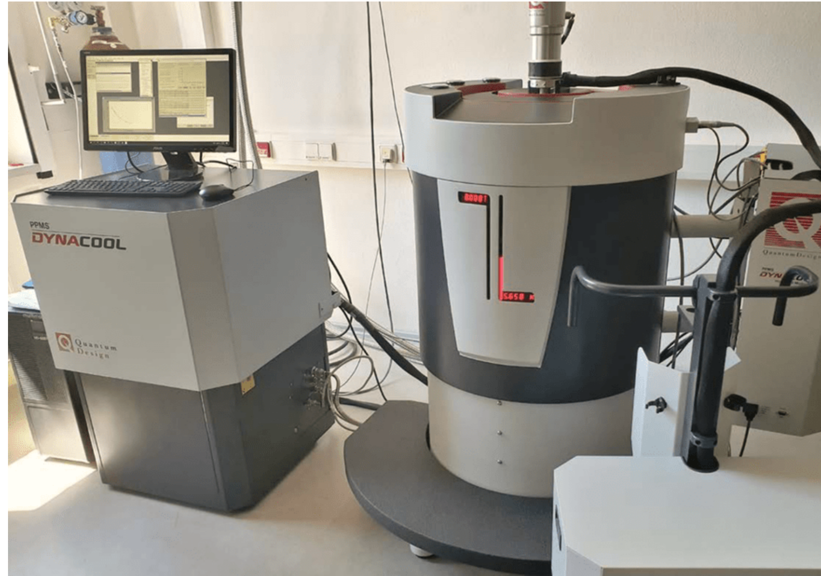


Figure 2.19: PPMS station installed at the IEP laboratories.

performed via the Measureready FastHall station by Lake Shore Cryotronics equipped with a M91 measurement controller and a 1 T permanent magnet. Low temperature sheet resistance and Hall measurements were carried out with the vdP option of DynaCool-12 physical property measurement system (PPMS) by Quantum Design (Figure 2.19). The magnetic field applied was varied from 3 to 8 T, and measurements were conducted over a temperature range from 1.8 to 300 K. Repeated measurements on the same SOI samples revealed perfect compatibility across the three setup used.

Magnetoresistance measurements at low temperature were performed to investigate the variation of the sheet resistance as a function of the applied magnetic field from 0 to 10 T in the PPMS. Measurements performed in the PPMS system were conducted with the help of Prof. Roman Gumeniuk from the IEP of the Technische Universität Bergakademie Freiberg, Germany.

2.2.7 Capacitance-Voltage

Capacitance-Voltage (CV) measurements provide key characteristics of the dielectric interface of MOS capacitors. The probe station used in this work (Figure 2.20) is composed of a metal chuck that support the sample and can act as the electrical back contact, tungsten tips mounted on a manipulator to contact the top pads, an Agilent E4980A Precision LCR Meter with GPIB interface for measurement and a LABVIEW software for the collection and analysis.

In a typical configuration, the top electrode is biased while the bottom is grounded. The

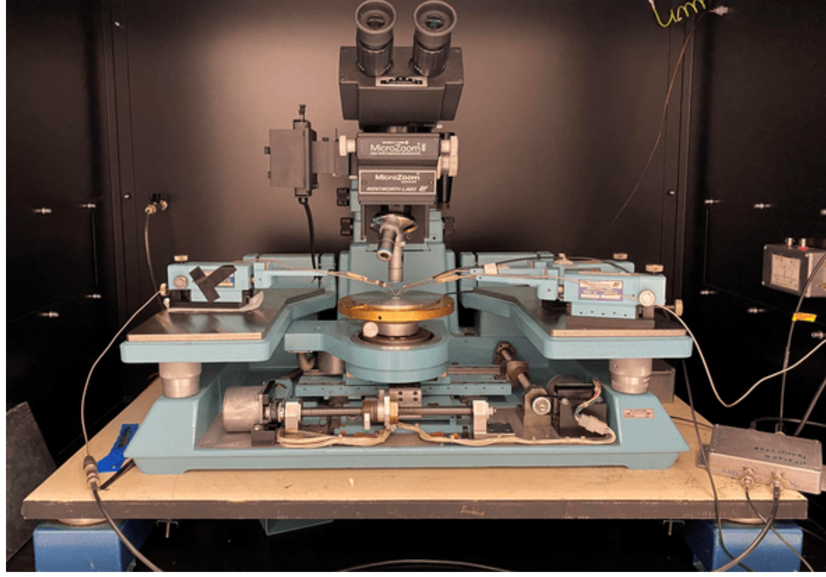


Figure 2.20: Probe Station installed at CNR-IMM laboratories.

handle wafer is left floating. The capacitance of a MOS capacitor in the accumulation zone is related to the geometrical dimensions of the gate and the dielectric using a parallel plate model [91]:

$$C_{ACC} = C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox} A}{H_{ox}}, \tag{2.15}$$

where C_{ACC} is the measured capacitance in the accumulation condition, A the gate electrode area, H_{ox} the dielectric thickness, and ε_0 and ε_{ox} the vacuum and dielectric permittivity. In the inversion or depletion zone, the capacitance of the system is modified considering the depleted region created in the inversion layer. The total capacitance is the series capacitance of the oxide C_{ox} and the semiconductor C_s [91]:

$$\frac{1}{C_{INV}} = \frac{1}{C_{ox}} + \frac{1}{C_s} = \frac{1}{\frac{\varepsilon_0 \varepsilon_{ox} A}{H_{ox}}} + \frac{1}{\frac{\varepsilon_0 \varepsilon_s A}{W_{dep}}}, \tag{2.16}$$

where C_{INV} is the measured capacitance in the inversion condition, W_{dep} the depleted region thickness, ε_s the semiconductor permittivity. The depth of the depleted region is related to the active dopant concentration n_a, i.e., the amount of active dopant that can be ionized and contribute to carrier conduction in a substitution position of the Si lattice.

$$W_{dep} = \sqrt{\frac{2\varepsilon_s \Phi_s}{q n_a}}, \tag{2.17}$$

where Φ_s is the surface potential. By comparing eq. 2.16 and 2.17 it is possible to extract the

n_a value:

$$n_a = \frac{2\Phi_S}{q\varepsilon_S A^2}\left(\frac{C_{INV}C_{ACC}}{C_{ACC}-C_{INV}}\right)^2, \tag{2.18}$$

The density of interface states D_{IT} is extracted using the formula derived from the conduction method by Nicollian-Brews [91]:

$$D_{IT} = \frac{2}{qA}\frac{G_p/\omega}{\left(\frac{G_p}{\omega C_{ACC}}\right)^2 + \left(1-\frac{C_m}{C_{ACC}}\right)^2}, \tag{2.19}$$

where G_p is the peak parallel conductance measured, $\omega = 2\pi f$ is the angular frequency and C_m the capacitance measured at the conductance peak.

CV characteristics were measured over a frequency range from 500 Hz to 1 MHz and the results are averaged between the ones collected. In ideal capacitors, capacitance is independent of applied voltage and frequency. A double voltage sweep with 50 mV steps was performed to evaluate hysteresis, which was not observed in any of the sample. All the results were corrected to account for the presence of a series resistance.

Validation of the characterization methods on Bulk Si

To validate the electrical and compositional characterization methodologies used for the SOI samples, we performed a controlled experiment on bulk Si substrates.

Two identical sets of bulk Si substrates were prepared. After 2% HF bath to remove the native SiO_2 oxide, each sample was capped with 2 nm SC2-SiO_2 capping layer chemically grown in SC2 ($H_2O : H_2O_2 : HCl$, 5.5 : 1 : 1) at 75 °C for 20 min. The samples underwent a hight temperature oxidation process in RTP (RTO) at 900 °C for 5 min to grow a 15 nm thick RTO-SiO_2/Si capping layer. This sample preparation precisely replicated the RTO process applied to the SOI samples. The pristine bulk substrates were already doped with P (Si : P) in a broad concentration range, from 1×10^{15} cm^{-3} to 6×10^{19} cm^{-3}.

- Sample Set 1: Dedicated to transport measurements (R_S, and Hall effect) and ToF-SIMS analysis.
- Sample Set 2: Dedicated to CV characterization.
- The P Dopant concentration (n_D) was directly measured via ToF-SIMS analysis for samples above the instrument sensitivity limit.
- The active dopant concentration (n_a) was extracted from the CV analysis (eq. 2.18).
- The electron concentration (n_e) was computed from Hall measurements (eq. 2.14), considering the thickness of the entire wafer. The carrier concentration is assumed to be an indicator of the total ionized P concetration.

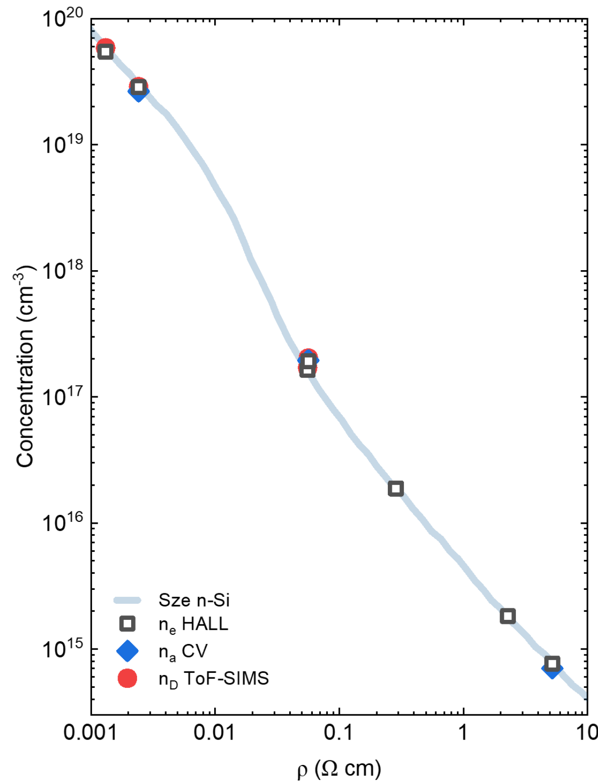


Figure 2.21: Carrier concentration (n_e) computed from Hall measurements vs dopant concentration (n_D) measured by ToF-SIMS depth profiles vs active dopant concentration (n_a) measured by CV analysis for bulk Si substrates.

The results obtained for these bulk Si substrates are presented in Figure 2.21 as a function of the ρ of each sample, which was determined by eq. 2.6. This comparative analysis revealed that our extracted values are perfectly compatible with established literature across the entire range of P concentration [7, 92], thereby validating the entire experimental method. Furthermore, the close agreement between the donor concentrations (n_D) measured by ToF-SIMS and the electron concentrations (n_e) derived from electrical measurements on these bulk samples strongly supports the $r_H = 1$ approximation used for the Hall scattering factor in eq.2.10 [92].

2.2.8 Current-Voltage

Current-Voltage (IV) measurements provide key information about the characteristics and the conduction mechanisms of devices. The probe station follows the same scheme described for CV measurements. In this work, a high-vacuum variable temperature prober by Nagase Co. equipped using a high precision parameter analyzer by Agilent/Keysight with resolution in

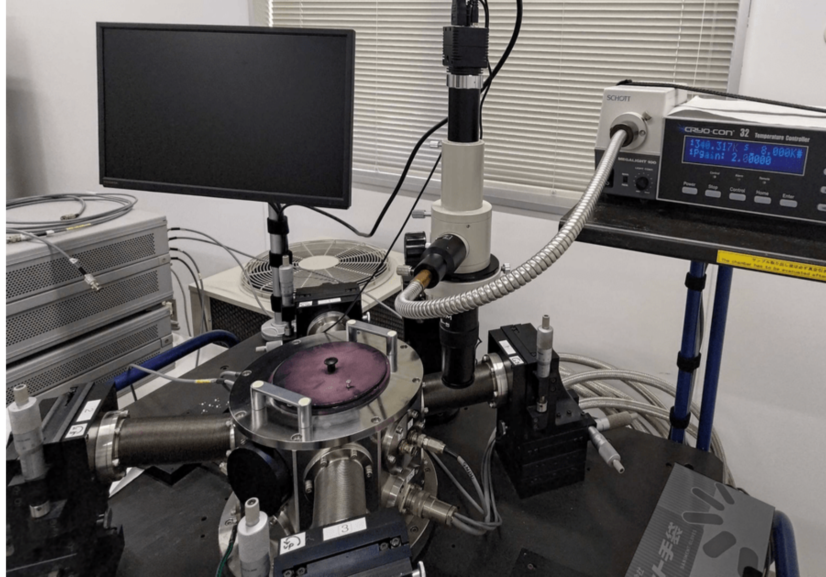


Figure 2.22: Probe Station installed at the RIoE laboratories.

the ~ 10 femtoampere (fA) range for IV measurement at the RIoE laboratories during the research period abroad in Hamamatsu, Japan.

IV Measurements were performed at temperatures ranging from 300 to 8 K in vacuum in a dark ambient. In a typical configuration, three electrodes were used to contact the source, drain and the gate contact. The back contact to the handle wafer was always left floating. The left 60×60 μm^2 Al electrode was defined as the source and grounded and the right electrode was biased as the drain (V_D). Gate voltage (V_G) is applied to the top 5 μm Al electrode. The gate only significantly affects the potential in the effective channel length between the source and drain leads.

Another type of IV measurement aims for the characterization of the contact resistance. Al pads are deposited in a linear configuration with distances between each contacts (d) varying from 25 μm to 200 μm. This arrangement constitutes the linear Transfer Length Method (TLM). By measuring the total resistance between adjacent pad pairs for each varying d, it is possible to separate the specific contact resistance (ρ_c) from the sheet resistance of the semiconductor (R_s). The total resistance at each pair is the sum of the bulk resistance of the channel and the resistance contributed by the two Al-Si contacts ($2R_c$). When the data is plotted as a function of the separation distance, the result is a straight line. The slope directly relates to R_s and the dimensions of the channel, while the intercept at $d = 0$ provides the total contact resistance ($2R_c$).

Chapter 3

Doping at the nanoscale

In this chapter, I present the investigation of the physical and electrical properties of doped ultrathin Si films, experimentally realized on a SOI platform. The study focuses on understanding how the thickness of the film (H_{SOI}) and doping concentration (n_D) influence charge transport.

First, I detail the processing parameters and testing methodologies that enable the precise control of the doping profile and fabrication of test devices within these semiconductor nanofilms. The discussion of the experimental results demonstrates how the fundamental transport properties are changed by the reduction of H_{SOI}.

I show how the transport mechanism is significantly influenced by the surrounding SiO_2/Si interfaces particularly through the effect of non-passivated interface states and dielectric mismatch. Furthermore, I detail the identification of quantum phenomena that emerge at high n_D. Finally, I present the initial development and optimization of a periodic patterning procedure used to successfully transfer a topology onto the crystalline Si device layer to tune the electrical properties of the semiconductor.

3.1 Sample preparation

In this work, poly(methylmethacrylate) (PMMA) and polystyrene (PS) polymers terminated with phosphorus-containing groups (PMMA-P and PS–P) were employed for the doping of the Si device layer. The polymers were synthesized in collaboration with the research group of Prof. Michele Laus from the University of Eastern Piedmont (UPO).

PMMA-P and PS–P polymers were produced via activators regenerated by electron transfer atom transfer radical polymerization (ARGET–ATRP) of poly(methylmethacrylate) and polystyrene, followed by attachment of a diethylphosphate (DPP) terminal group to the polymer chain. After purification, gel permeation chromatography (GPC) was used to determine the molar mass (M_n) and polydispersity index (Đ), while Nuclear Magnetic Resonance (NMR) spectroscopy was performed to evaluate the yield of the phosphorylation

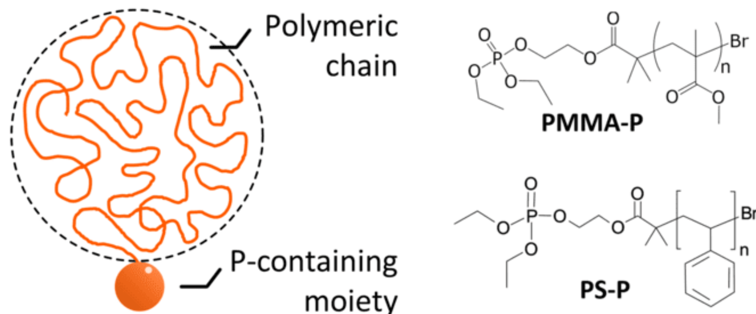


Figure 3.1: Schematic representation of the polymer P-terminated and the chemical composition of the PMMA-P and PS-P used in this work.

reaction. A detailed description of the synthesis and characterization of P end-terminated polymers is available in a previous publication [69].

The PMMA-P used in this work was characterized by an average molar mass M_n = 7.5 kg/mol and a polydispersity index Đ = 1.14. The PS–P was characterized by an average molar mass of M_n = 2.4 kg/mol and a polydispersity index Đ = 1.15. A schematic representation of the polymer structure as well as the chemical composition of the PMMA-P and PS-P used in this work is shown in figure 3.1.

Figure 3.2 presents a schematic representation of the procedure used to create a P δ-layer source of dopants after 1 grafting-ashing cycle at the surface of the Si device layer. The doping process followed the PPD alternative bottom-up approach introduced in Section 1.4.

1×1 cm^2 SOI dies were cleaved from lightly doped SOI wafers. Three pristine SOI substrates from different suppliers were employed to minimize substrate-dependent contributions. The thickness of the buried oxide (BOX) layer was 200 nm, 160 nm and 210 nm, while the Si device layer (H_{SOI}) was 75 nm, 50 nm and 70 nm, respectively. The device layer was further thinned to the desired H_{SOI} by oxidation at T = 1000 °C. This process was already optimized to achieve nanometric control on the thickness of ultrathin SOI films with no evidence of sample degradation associated with the high temperature oxidation [38, 39]. Before polymer deposition and grafting, each die underwent a bath in HF solution to remove the thermal oxide layer grown on the Si surface. The HF-deglazed Si samples were then rinsed in deionized (DI) water and dried under N_2 flow.

Samples were cleaned to remove contaminants through sequential treatments in acetone (5 min) and ultrasonic isopropanol (IPA) bath (5 min), followed by N_2 drying. The SiO_2 layer was etched in a 2% HF solution, followed by a 2 min deionized (DI) water rinse to expose H-terminated reactive sites on the Si device layer surface. Polymer films were deposited on the deglazed Si device layer by spin coating from 1.5 wt% solutions in propylene glycol monomethyl ether acetate (PGMEA). Spin coating was performed at 2000 rpm for 30 s, aiming for $30-40$ nm thick uniform films of P-terminated polymer. The thickness of the film and the optical properties were verified by SE.

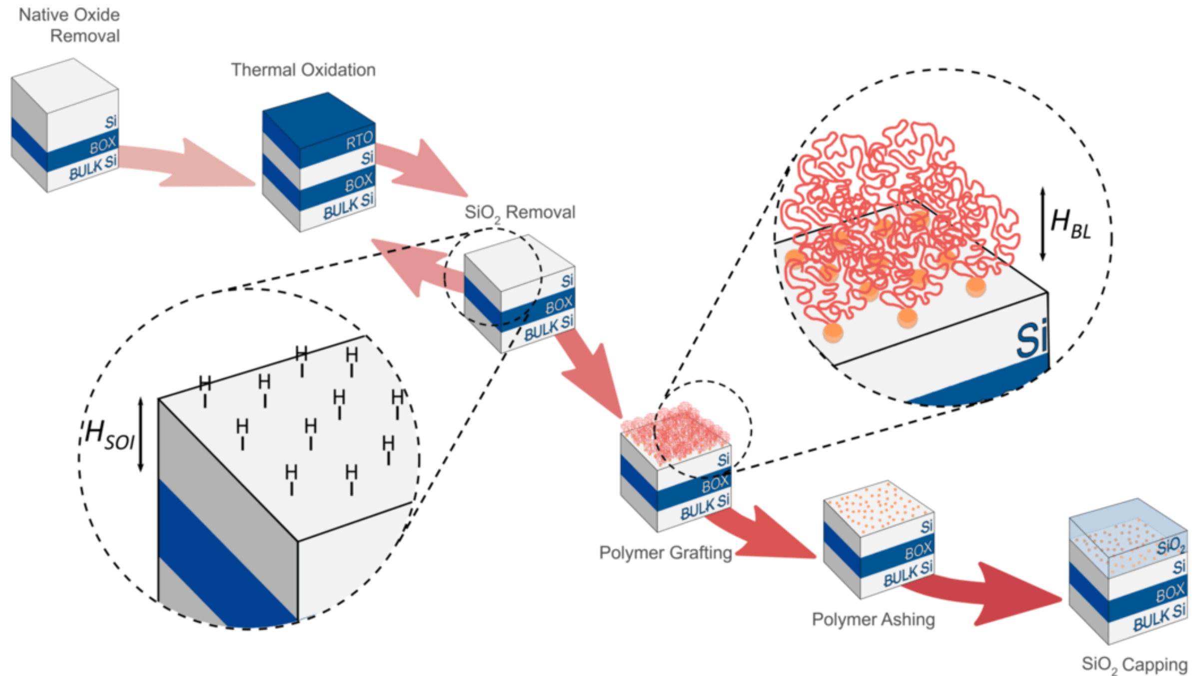


Figure 3.2: Schematic flow for the preparation of a P δ-layer source on a HF-deglazed SOI substrate.

The samples were then annealed at 210 °C for 600 s in N_2 using a rapid thermal processing (RTP) system to promote the grafting-to reaction via the P-containing moiety. Non-grafted chains were removed in an ultrasonic PGMEA bath for 5 min, leaving a thin brush layer whose thickness was measured by SE.

The residual polymeric chain was removed via oxygen plasma at 40 W, leaving only the P dopants attached to the surface. The etching rate of PS was about 0.03 nm/s, allowing complete removal within a few minutes. An over-etch of 10–20% was applied to minimize carbon contamination without affecting phosphorus atoms covalently bonded to the substrate. Samples were immediately loaded into the vacuum chamber of the evaporator in order to minimize exposure to air and prevent reoxidation of the surface. A 10 nm SiO_2 capping layer was then deposited by e-beam evaporation to create the P δ-layer source at the SiO_2/Si interface, preventing dopant desorption and contamination.

The dopants are injected and activated via high temperature annealing via RTP system. After removal of the ebeam SiO_2 capping layer, all the doped SOI samples were capped with a 2 nm SiO_2 layer chemically grown in standard clean 2 (SC2) solution (H_2O:H_2O_2:HCl, 5:1:1) at 75 °C for 20 min in order to guarantee a consistent SiO_2/Si top oxide (TOX) interface.

Finally, after mesa patterning of the samples in KOH solution (22 % wt.) at room temperature, aluminum metal contacts were deposited by thermal evaporation at the corners

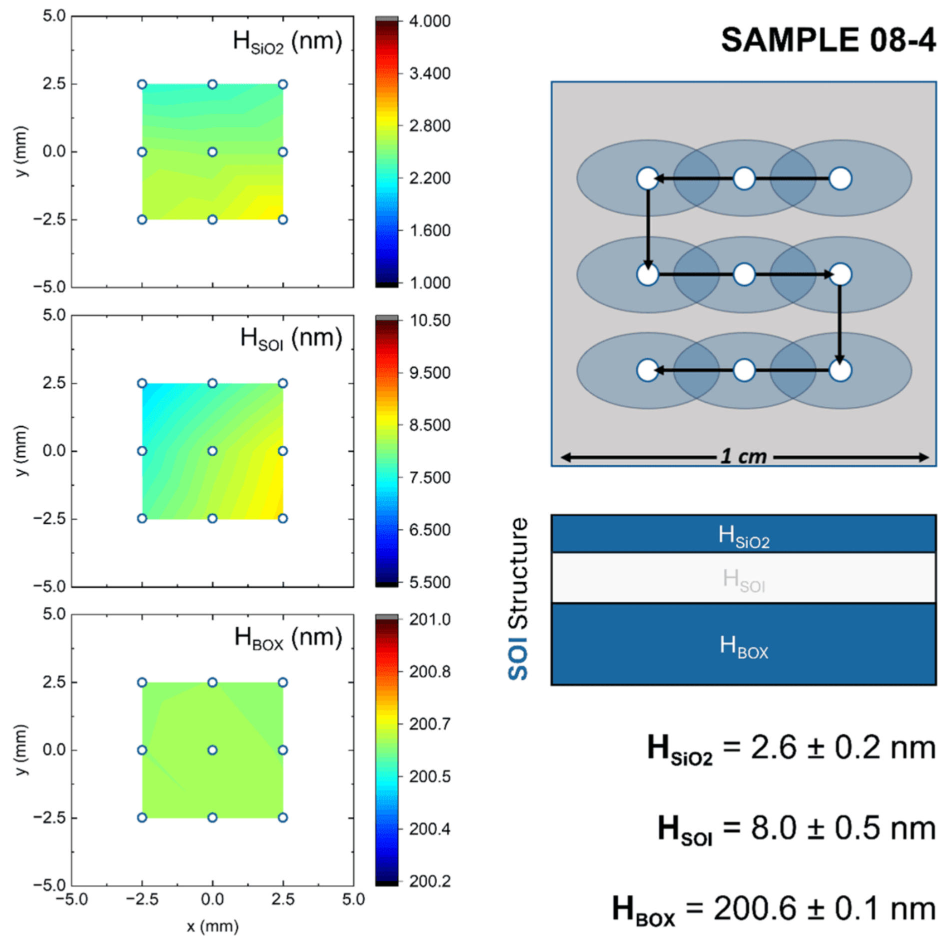


Figure 3.3: Spectroscopic ellipsometry (SE) measurements scheme of an example sample. Data are fitted using a three-layer SOI model as presented in the SOI structure.

of each structure following two subsequent photolithography exposures. More detailed description of the mesa patterning and photolithography steps, as well as the design of the mask used is presented in section 3.3.

SE was used to accurately monitor H_{SOI} after each step of the process. Sample preparation was optimized to produce SOI films with H_{SOI} ranging from 6 to 70 nm after SC2 capping. Since H_{SOI} is critical in correlating the electrical properties of the samples, at the end of the process, the thickness of the device layer of each SOI sample is measured at five or nine evenly spaced points across the center of the sample at a fixed incidence angle of 75°. Repeated measurements of the same spot produced the same thickness value. An uncertainty of 0.1 nm was assigned to each measurement spot. The measurement scheme of an example sample is presented in Figure 3.3.

Experimental data are fitted using a three-layer model comprising the BOX, the device layer, and the top SiO_2. Mean values and errors are computed as the average and standard deviation of the nine points collected across the sample. H_{SOI} values reported are the average ones obtained at the end of the process, after SC2 cleaning, just before mesa patterning and electrical characterization of the samples.

3.2 Doping control

Previously, control of the dopant dose in the δ-layer source relied mainly on the accurate control of the self-limiting process based on M_n [60], which requires process optimization tailored to the specific characteristics of each polymer batch. Moreover, the degree of polymerization ($N = M_n/M_0$ in eq. 1.3) of the dopant polymers, cannot be easily tuned over a wide range.

Synthesizing very short (low-N) chains is difficult due to the intrinsic statistical nature of polymerization reaction, making it challenging to obtain narrowly distributed low-M_n polymers. On the other hand, synthesizing very long (high-N) polymers introduces solubility and processability issues, as long chains tend to entangle and increase solution viscosity, complicating uniform deposition. Furthermore, long chains are characterized by reduced molecular mobility and slower grafting kinetics.

To overcome this limitations, additional strategies were developed in this thesis work to enhance the reproducibility and tunability of the doping concentration. This part of the work aimed to achieve accurate modulation of the doping profile by varying the processing parameters rather than altering the dopant polymer itself. This methodology enables fine process tuning while also improving the full compatibility with large-scale integration technologies.

Accurate control of the dopant dose (atoms/cm^2) introduced into the Si device layer was realized through two distinct approaches: a modified version of the *Multicycle* approach (3.2.1), originally developed on SiO_2 and adapted for HF-deglazed Si and the *Double Annealing* process (3.2.2).

3.2.1 Multicycle approach

The first approach follows a methodology already described in our previous publications [60, 61, 72]. Repeated grafting/ashing cycles of the polymer lead to a stepwise linear increase in the number of P atoms grafted to the Si surface. Increased P dose in the δ-layer source already demonstrated increased N_D injected in the substrate by the same injection treatment. However, the methodology was applied to repeated grafting-ashing cycles on SiO_2 capped Si substrates with OH termination and not HF-deglazed Si samples with H termination, making the oxygen plasma ashing step particularly critical to reoxidation. In the present work, to increase the amount of P in the dopant source, the number of grafting/ashing cycles was varied between 1, 3, 5, and up to 10, whereas previous studies were limited to

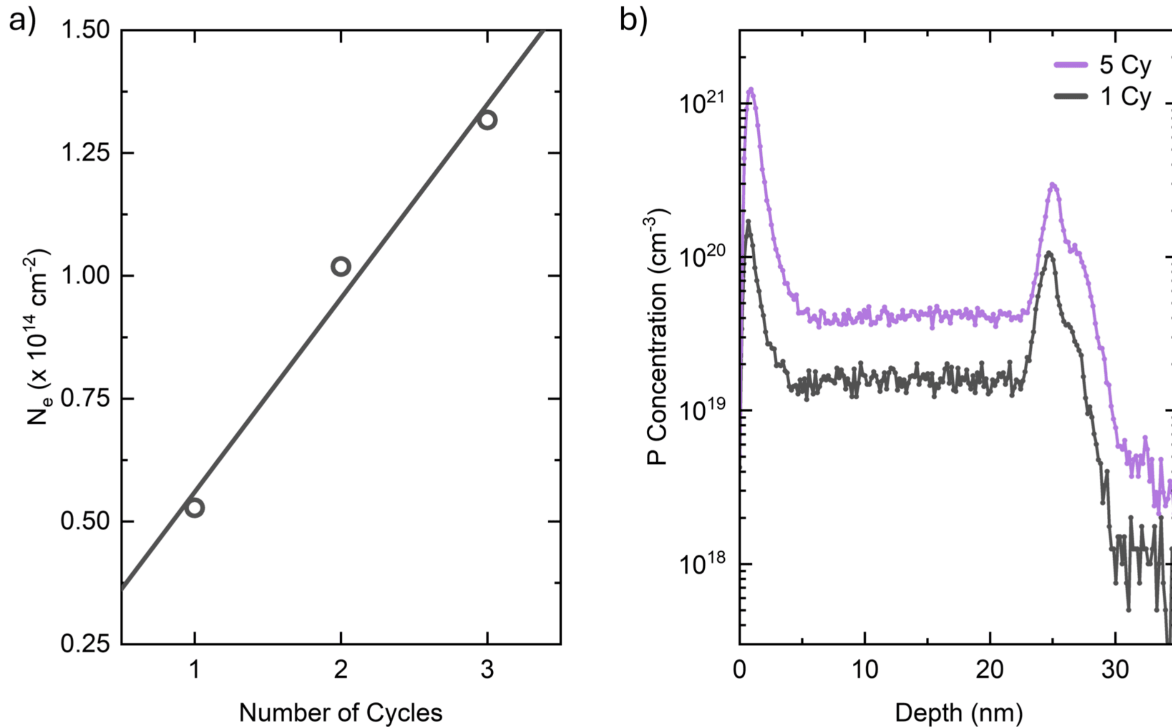


Figure 3.4: (a) N_e as a function of the number of grafting-ashing cycles. (b) ToF-SIMS P depth profiles of SOI samples with $H_{SOI} = 24 \pm 1$ nm doped following 1 and 5 cycles.

a maximum of 5 cycles. After deposition of a 10 nm thick SiO_2 capping layer, the samples underwent a single high-temperature treatment in an RTP system at $T = 1000$ °C in N_2 atmosphere to promote drive-in and redistribution of P atoms into the Si device layer.

A test 340 nm thick SOI was used to investigate the process and demonstrate the correct transfer of the process to HF-deglazed Si. The carrier dose N_e measured via Hall effect in the samples as a function of the number of grafting-ashing cycles is reported in Figure 3.4a. Clear linear stepwise increase is demonstrated even in the case of HF-deglazed Si. Each subsequent grafting-ashing cycle achieves an average 75 % increase in N_e.

Increase of the P dopant dose was demonstrated by the calibrated ToF-SIMS depth profiles in Figure 3.4b, for SOI samples with $H_{SOI} = 24 \pm 1$ nm. ToF-SIMS profiles were calibrated in the Si matrix according to the protocol detailed in Section 2.2.4. By increasing the number of grafting cycles to 5, the P concentration (n_D) is greatly increased compared to the sample doped with 1 doping cycle. A small increase in the P signal at the Si device layer/BOX interface was observed at higher n_D. While this feature suggests the presence of P near the interface, the change in SIMS ionization probability between the Si and SiO_2, limits our interpretation to a qualitative observation, as discussed in Section 2.2.4. These features at the interface are therefore treated as a combination of partial P segregation at the

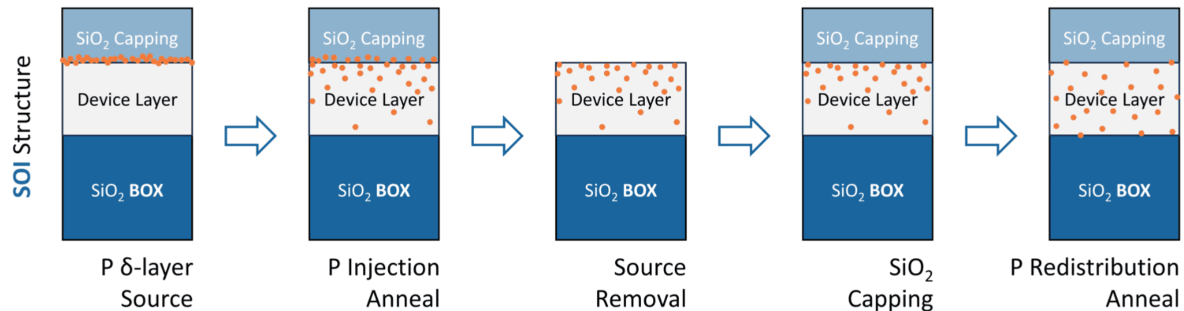


Figure 3.5: Schematic representation of the *Double Annealing* doping approach. The first annealing selects the P dose injected into the device layer while the second uniformly redistributes and activates the dopants.

Si/BOX interface and possible partial diffusion into the BOX [39] and known SIMS matrix artifacts at the interface.

3.2.2 Double annealing approach

The second approach employs an alternative protocol aimed at reducing the P concentration in the Si device layer by decoupling the injection and redistribution processes, which are performed in two separate thermal treatments. A schematic of this *Double Annealing* approach is shown in Figure 3.5. A P δ-layer source is created at the surface of the Si device layer using a single grafting/ashing cycle. The first annealing is performed at T = 900 or 1000° C in N_2 atmosphere. By adjusting the annealing time, the effective P dose in the Si device layer can be precisely controlled [38]. A calibrated P concentration profile for a SOI sample with $H_{SOI} \sim 23$ nm, after drive-in at 1000 ° C for 1 s, is reported in Figure 3.6a (black line). The short injection treatment results in a P concentration gradient throughout the device layer, consistent with Fick's law of diffusion for thick SOI films [8].

After injection, the 10 nm thick SiO_2 capping layer and the P δ-layer source are removed via 2 % HF bath and 2 min DI water rinse. A new 10 nm thick SiO_2 capping layer is immediately deposited by e-beam evaporation to prevent P out-diffusion during the subsequent thermal treatment. A second high-temperature treatment is then performed at T = 1000 °C for 100 s in N_2 atmosphere to redistribute the dopants throughout the Si device layer. Thermal treatment at 1000 °C for 100 s has been shown to fully activate the dopants and achieve uniform P concentration for 30 nm thick SOI samples and optimal electrical properties (Section 1.4) [38]. Figure 3.6a also shows a representative calibrated P profile after the double annealing process. ToF-SIMS depth profiles demonstrate uniform dopant concentration throughout the device layer and a clear reduction in the P dose confined within the layer. The inset of Figure 3.6a shows the total P dose (N_D) in the device layer, computed as the integral of the P concentration depth profile obtained by ToF-SIMS. The first injection treatment was varied between 1, 10, and 100 s. Comparison of N_D before and

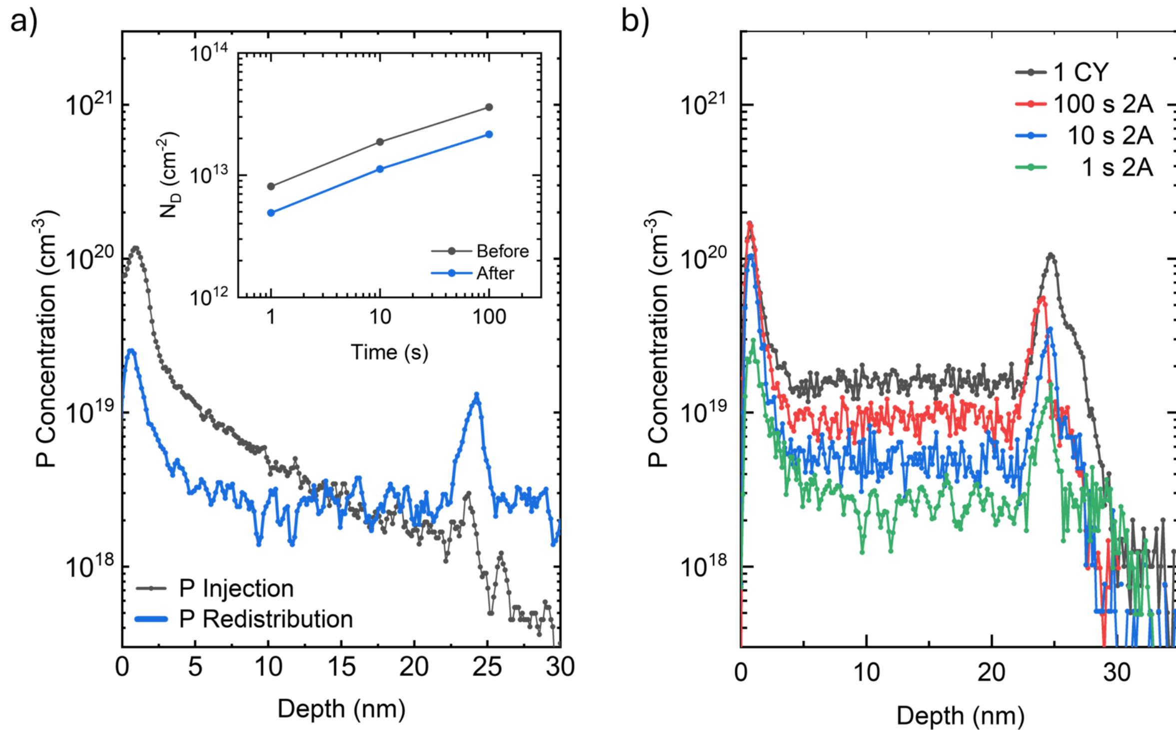


Figure 3.6: (a) ToF-SIMS P depth profiles of a SOI sample with $H_{SOI} \sim 23$ nm obtained before (black) and after (blue) the redistribution anneal. In the inset, N_D values before and after the redistribution annealing as a function of the duration of the injection treatment. (b) ToF-SIMS P depth profiles of SOI samples with $H_{SOI} = 24 \pm 1$ nm doped following different sample preparation procedures.

after the second redistribution step indicates a ~40 % reduction of the P dose due to possible segregation and out-diffusion through both the TOX and BOX interfaces [39].

Reduction of the P dopant dose injected was demonstrated by the calibrated ToF-SIMS depth profiles in Figure 3.6b, in the case of SOI samples with $H_{SOI} = 24 \pm 1$ nm. By varying the duration of the first injection treatment between 1, 10 and 100 s, P atoms are uniformly redistributed throughout the Si device layer, while the P concentration (n_D) is greatly reduced compared to the sample doped with 1 doping cycle.

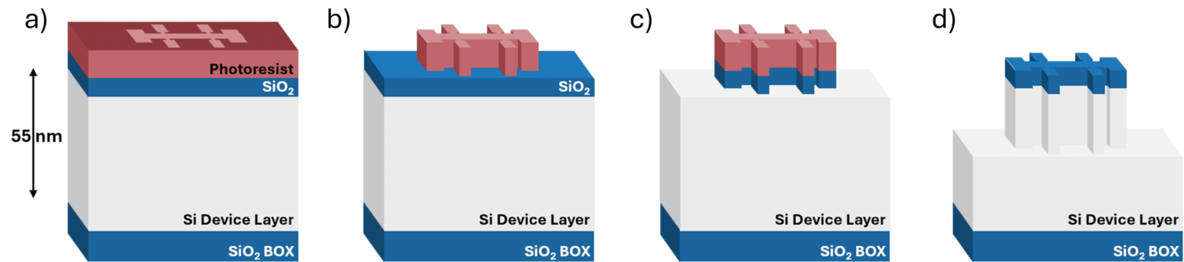


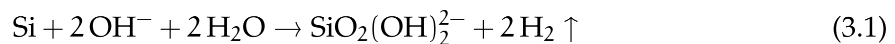
Figure 3.7: Schematic representation of the KOH mesa patterning. (a) Resist exposure, (b) Resist developement and opening, (c) BOE SiO_2 etching, (d) KOH Si etching.

3.3 Patterning and test device fabrication

At the end of the sample preparation process, each sample was capped with a 2 nm SC2-grown SiO_2 capping layer before device fabrication and subsequent electrical measurements. Mesa patterning was employed to define the device geometry, followed by photolithography and precise alignment steps for the deposition of aluminum (Al) ohmic contacts. These fabrication steps were introduced to replace the shadow mask approach previously used in the laboratory, significantly improving the measurement accuracy and ensuring a more reliable and reproducible characterization of test devices.

A schematic illustration of the mesa definition is shown in Figure 3.7. The fabrication process began with cleaning of the susbstrates in acetone (5 min) and isopropanol (5 min) baths, followed by N_2 drying. A photoresist layer was then spin-coated after Hexamethyldisilazane (HMDS) treatment of the surface in order to improve adhesion to the substrate. The positive photoresist was exposed and developed to define the desired etched areas of the mesa pattern. A post-bake annealing step is performed to harden the resist mask, improving mechanical stability during the subsequent two-step wet etching.

The exposed regions of the 2 nm SiO_2 film were opened using Buffered Oxide Etchant (30:1 BOE). After etching, samples were rinsed in DI water for 2 min, dried in N_2, and immediately immersed in a 22 wt% electronic-grade KOH solution at room temperature to etch the Si layer and define both the mesa geometry and alignment marks. The etching process follows the anisotropic reaction between Si and KOH:



$$\mathrm{Si} + 2\,\mathrm{OH}^- + 2\,\mathrm{H_2O} \rightarrow \mathrm{SiO_2(OH)_2^{2-}} + 2\,\mathrm{H_2} \uparrow \tag{3.1}$$

The KOH solution was continuously stirred to maintain uniformity, ensuring homogeneous etching and consistent etch rates across the sample surface. The anisotropy of the KOH etch arises from the lower etch rate of the (111) Si plane compared to the (100) and (110) planes, enabling the formation of well-defined trenches.

To calibrate the KOH etching rate and evaluate the quality of the etched regions, preliminary tests were conducted on 55 nm-thick SOI test substrates. Figure 3.8 presents the

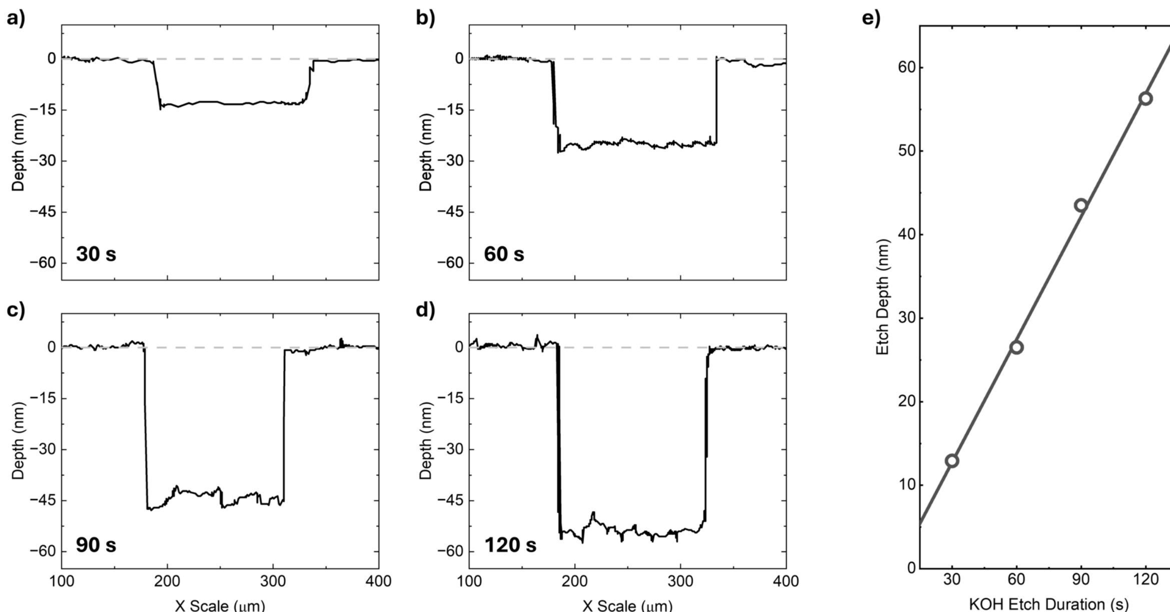


Figure 3.8: Profilometer trench profiles after KOH etching for 30 s (a), 60 s (b), 90 s (c), and 120 s (d). Panel (e) shows etched depth versus KOH process duration at room temperature.

profilometer height profiles of four samples etched for 30, 60, 90, and 120 s (a to d, respectively). Height data are normalized to the non-etched Si surface, which is set as zero. The dips in the profiles confirm effective Si removal, with etch depth increasing proportionally to the KOH exposure time. Regardless of the etch depth, the resulting features exhibit clean and well-defined edges, demonstrating the anisotropic nature of the KOH etching. For samples a to c, the full etch condition was not reached, as the depth remained below the Si device layer thickness ($H_{SOI} \sim 55$ nm). The complete removal of the Si device layer was verified during the wet etching by observing changes in the color of the etched regions and further confirmed by profilometer analysis for sample d.

Figure 3.8e shows the etch depth as a function of the KOH bath time, revealing a clear linear dependence. A linear fit of the data yielded an etching rate of approximately 0.5 nm/s. This value, combined with visual observation of color changes in the etched regions, was used to confirm complete removal of the Si device layer and to ensure accurate mesa definition for all SOI samples prepared in this work.

Following mesa patterning, a second photolithography step was carried out to define and align the Al ohmic contacts. The schematic representation of the process is shown in Figure 3.9. The samples are first cleaned in acetone and subsequent isopropanol bath. After spincoating, the photoresist film is exposed and developed to open contact windows located at the corners of each structure. No post-bake is introduced in order to avoid hardening of the resist and to facilitate the subsequent lift-off process after metal deposition.

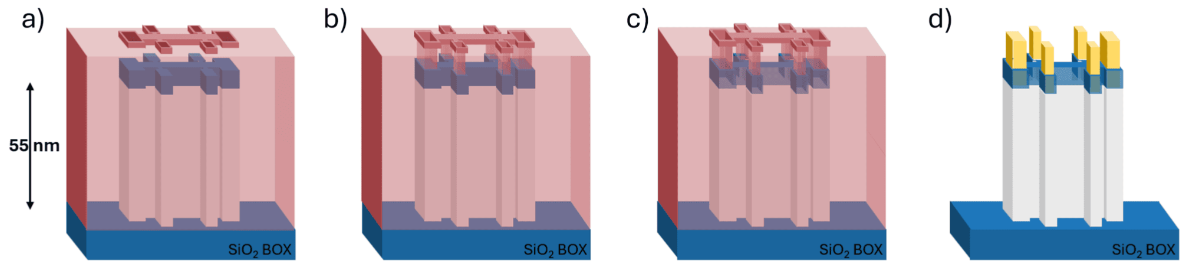


Figure 3.9: Schematic representation of the Al contact deposition process: (a) resist exposure, (b) resist development and window opening, (c) BOE SiO_2 etching, (d) Al deposition and resist lift-off.

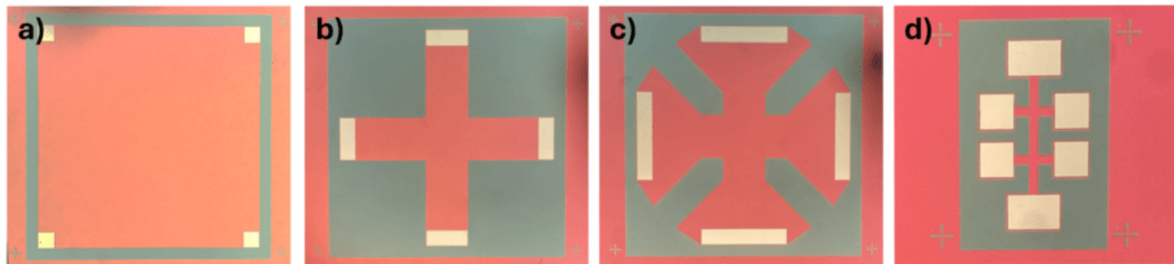


Figure 3.10: Close-up view of vdP geometries (a to c) and Hall bar (d) for electrical measurements.

The 2 nm SiO_2 capping layer is removed using a short 30:1 BOE etch to eliminate the interfacial oxide between Si and Al and minimize the Schottky barrier height between the metal and the semiconductor, thereby promoting the formation of low-resistance ohmic contacts [7]. After rinsing in DI water, the samples are immediately transferred to the chamber of an evaporator to prevent re-oxidation of the exposed Si surface. 150 nm thick Al is then deposited by thermal evaporation. Lift-off is performed in a 50 °C acetone bath to leave only the patterned contacts.

Figure 3.10 presents a close-up image of fabricated structures with alignment marks on the 55 nm-thick SOI substrate. The red regions correspond to the protected Si device layer that remained unetched during processing, the gray/green regions indicate the exposed buried SiO_2 following KOH etching, and the white areas represent the Al metal contacts precisely aligned at the edges of each device.

Accurate patterning of the substrates is crucial to minimize measurement errors arising from contact misalignment [93]. To further assess this effect, different van der Pauw (vdP) geometries were implemented, including square (Sample A), cross (Sample B), and clover (Sample C) configurations, each measuring 1.75×1.75 mm^2. These geometries were patterned at the center of three 1×1 cm^2 doped test SOI samples to investigate the systematic errors in the measured sheet resistance and Hall coefficients introduced by the

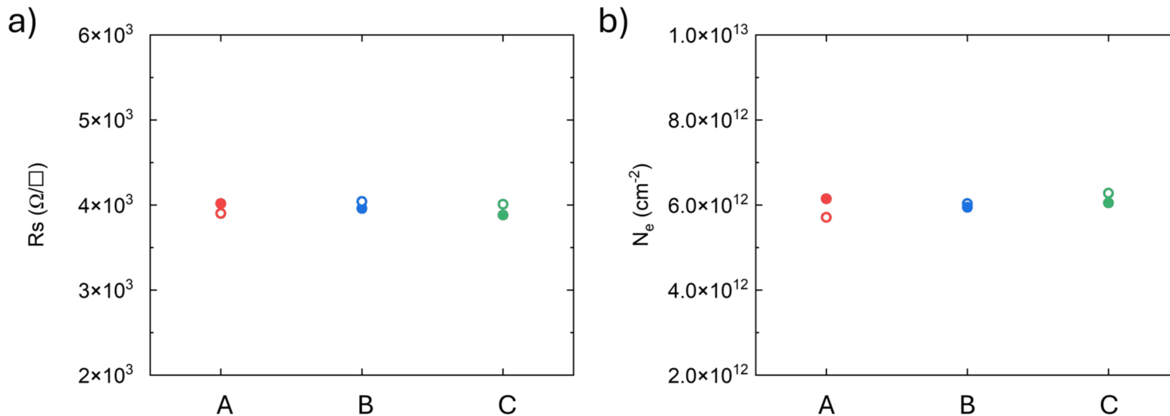


Figure 3.11: Sheet Resistance R_s (a) and carrier dose N_e (b) obtained at room temperature for different vdP geometries: square (A), cross (B), and clover (C).

finite contact size and imperfect alignment [94, 95]. The position and size of the Al contacts were also optimized. By comparing multiple vdP geometries, the influence of geometric deviations on the extracted electrical parameters can be evaluated, allowing selection of the configuration that provides the highest accuracy and reproducibility [95]. Larger contacts are expected to further reduce contact resistance. Representative examples of the different geometries are shown in Figures 3.10a to 3.10c.

Room-temperature sheet resistance and Hall measurements were performed on the three vdP geometries after bonding the Al contacts to the chip carriers. The results, shown in Figure 3.11, demonstrate consistent transport properties across all geometries, confirming that the precise alignment and small size of the Al contacts ensure reliable measurements.

A variation in carrier concentration (N_e) of less than 5 % was observed for the square geometry, while the cross and clover geometries exhibited even smaller variations. The sheet resistance (R_s) varied by less than 2.5 % across all geometries, indicating that R_s extraction is less sensitive to contact and mesa geometry. No significant influence of geometry was observed on the measured parameters. Based on these results, the square and cross geometries were selected for subsequent device fabrication and used to obtain accurate measurements of the SOI conductive properties.

TLM measurements were performed to evaluate the quality of the Al/Si ohmic contacts. Figure 3.12 reports the total resistance measured as a function of the distance (d) between two adjacent contacts for a doped SOI sample with $H_{SOI} \sim 24$ nm. Two independent test structures were measured to verify the uniformity across the sample. As expected, the resistance increases linearly with L across the entire range of the analysis, from 25µm to 200µm, consistent with the TLM model. The small variation observed between the two data sets confirms the high quality and spatial uniformity of both the contacts and the underlying highly doped device layer.

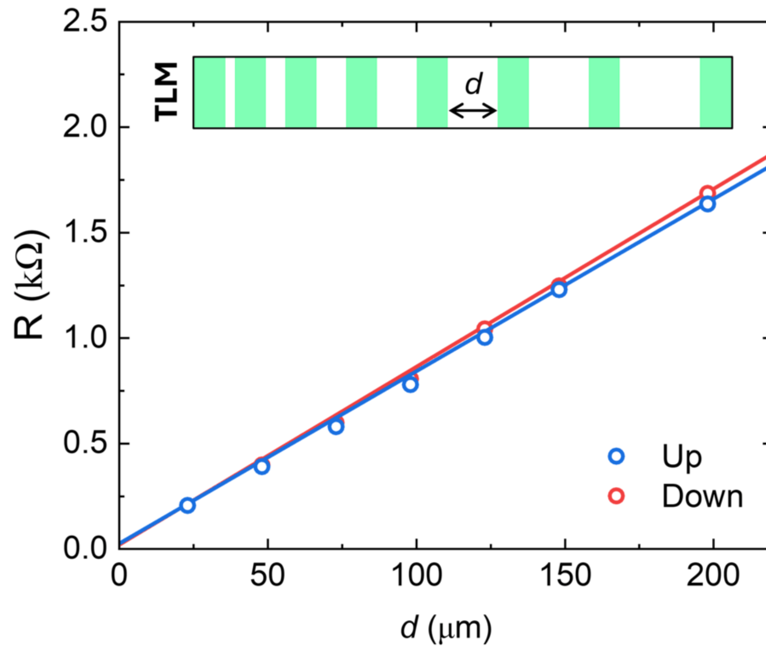


Figure 3.12: TLM resistance versus distance between contacts (d) for a doped SOI sample with H_{SOI} ~ 24 nm.

Linear fit of the experimental data is carried out to extract key electrical parameters (as described in Section 2.2.8). The average total contact resistance, R_c, was $12 \pm 2\ \Omega$, while the sheet resistance, R_s, was $1.45 \pm 0.03\ k\Omega/\square$. Similar R_S value vas obtained by measuring the sample in vdP configuration. The extracted small transfer length, L_T ~ 2μm, significantly smaller than the spacing used in the array, guarantees the correct one-dimensional current assumption of the TLM model.

Finally, the normalized contact resistivity, ρ_c, was calculated based on the Al contact dimensions and the measured R_s. The resulting $\rho_c \approx (3 \pm 1) \times 10^{-5}\ \Omega cm^2$ represents a competitive value, especially considering that the entire fabrication was performed manually in a standard cleanroom environment. This low contact resistivity confirms the formation of high-quality ohmic contacts. Therefore, contact resistance introduces only negligible errors in subsequent electrical measurements, including those performed on large-area structures in vdP configuration. Prior to all electrical measurements, the ohmic behavior of each pair of contacts in vdP configuration was verified through Current-Voltage (IV) measurements.

Two distinct vdP photolithography masks were employed for the characterization of the SOI samples, depending on whether Capacitance–Voltage (CV) measurements were performed. The mask layouts, designed using the KLayout software, are presented in Figure 3.13. In the schematic, the grey regions indicate the areas etched by KOH during the first photolithography step, while the green regions correspond to the Al ohmic contacts

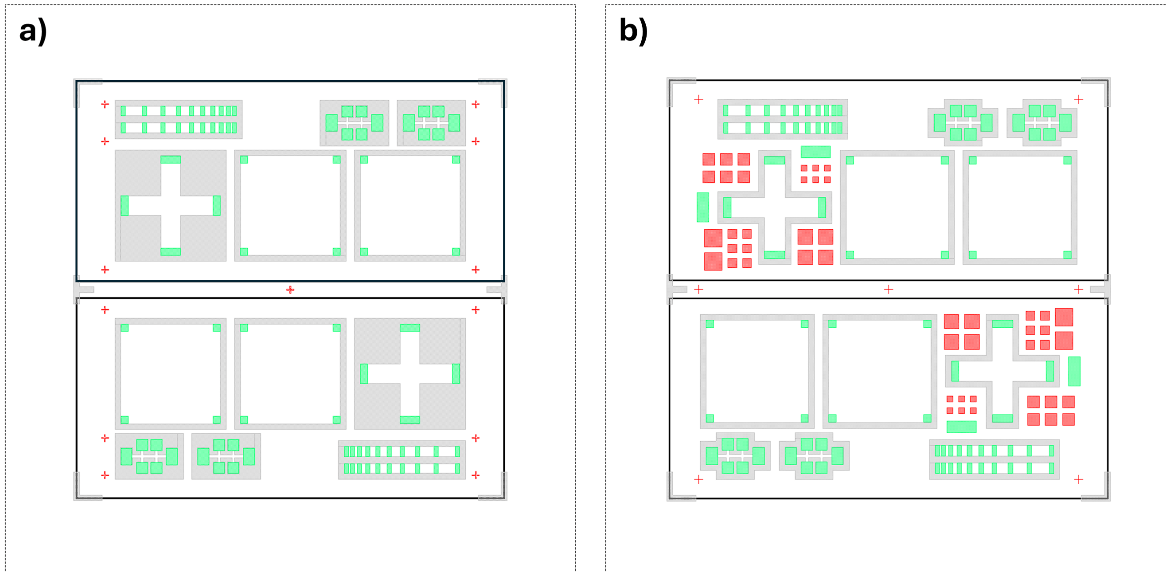


Figure 3.13: vdP mask designs for samples without (left) and with (right) capacitors for CV measurements.

deposited in the subsequent step. For samples intended for CV characterization, an additional photolithography step was implemented to define Al gate electrodes on top of the SiO_2 layer. The position and geometry of these Al gates are highlighted in red in Figure 3.13b.

The big alignment marks on the masks were employed to define sample areas of 3.5×7.5 mm^2, which were later cleaved either manually or using a 300 µm diamond cutting saw (installed at the IAP laboratories) at the end of the process. These dimensions were selected to ensure compatibility with the chip carrier used in the CNR-IMM laboratories and to allow simultaneous mounting of up to three samples on the PPMS puck used in the IAP laboratories.

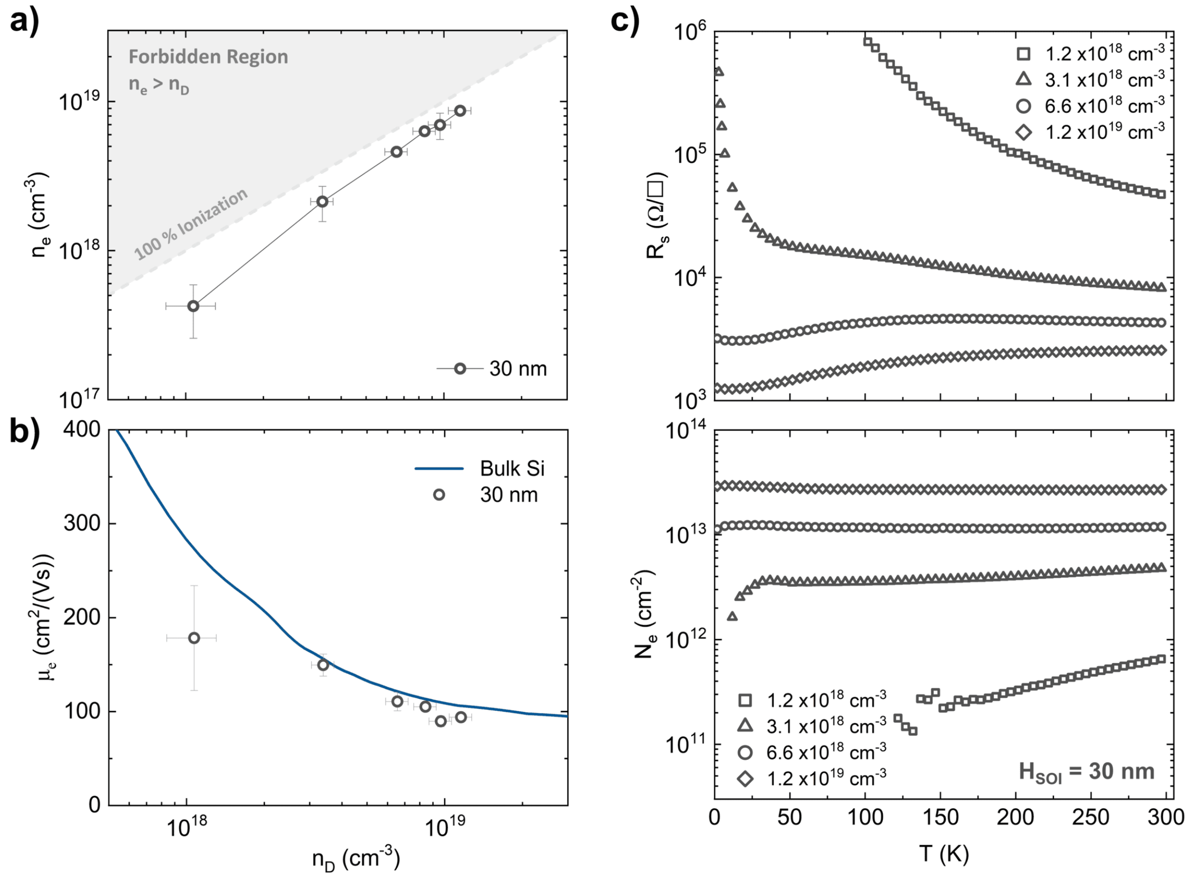


Figure 3.14: (a) The concentration of charge carriers (n_e) vs the total dopant concentration (n_D) for SOI with $H_{SOI} = 30 \pm 1$ nm. (b) mobility (μ_e) values as a function of n_D for the same SOI samples. Electron mobility in bulk Si (line) is shown for comparison [7]. (c) Example low temperature sheet resistance R_s (top) and total carrier dose N_e (bottom) obtained on SOI samples with $H_{SOI} \sim 30$ nm for different n_D values below and above the metal-insulator transition.

3.4 Methodology validation

To demonstrate the effectiveness of the proposed doping technique on ultrathin SOI substrates, 1×1 cm^2 SOI samples were fabricated with a target $H_{SOI} \sim 30$ nm. By controlling the concentration of dopants injected and activated into the Si device layer, it is possible to tune the electrical conductivity and validate this alternative doping approach in a wide range on P concentrations.

Figure 3.14a shows the carrier concentration (n_e), extracted from Hall measurements, plotted against the average P concentration (n_D) obtained from ToF-SIMS analysis for all

SOI samples with $H_{SOI} = 30 \pm 1$ nm. The n_e values are calculated as the ratio between the total carrier dose N_e, directly measured from vdP Hall measurements, and the device layer thickness H_{SOI}, measured by SE. As already discussed in Section 3.2, variations in the sample preparation protocol produced a broad range of doping concentrations, with n_D spanning from 10^{18} to 10^{19} cm^{-3} for the 30 nm SOI devices. In Figure 3.14a, the increase in n_D is clearly correlated with the increase in n_e, confirming effective and controllable dopant incorporation within the device layer.

The activation rate (η_a) is computed as $\eta_a = n_e/n_D$, assuming that n_e reflects the ionized P at room temperature [38]. Almost full activation is observed when $n_D > 1 \times 10^{18}$ cm^{-3}, with η_a values consistently above 80%. The theoretical model of incomplete ionization proposed by Altermatt *et al.* [92] predicts that in bulk Si, the fraction of ionized P atoms at room temperature varies with n_D. Specifically, the occupation probability of dopant states is directly related to the relative position of the dopant energy level (E_d) with respect to the Fermi level (chemical potential, E_F). A minimum at $n_D \sim 2 \times 10^{18}$ atoms/cm^3 is expected because E_F is close to E_d, resulting in up to 25% of donors remaining non-ionized, causing significant incomplete ionization even at room temperature [92]. In this n_D range, experimental data for $H_{SOI} \sim 30$ nm agree with the model, suggesting full activation at room temperature [39]. Interestingly, η_a slightly decreases when n_D is reduced to 1×10^{18} cm^{-3}. Further investigation of this apparent incomplete ionization effect is presented in Section 3.6.

Assuming a uniform P distribution through the Si device layer, the majority carrier mobility (μ_e) can be computed from the combination of sheet resistance and Hall measurements using eq. 2.13. Figure 3.14b reports the computed μ_e values versus n_D, compared to literature data for similarly doped bulk Si (solid blue line) [7]. Experimental results show that SOI samples with $H_{SOI} \sim 30$ nm match the electrical properties of uniformly doped bulk Si with similar n_D. Interestingly, the sample with the lowest n_D, which showed reduced η_a, also exhibits lower mobility.

The electrical properties of selected SOI samples were measured via sheet resistance and Hall effect in vdP configuration at low temperature, for T ranging from 1.8 to 300 K. The four selected samples span one order of magnitude in n_D (1.2×10^{18} to 1.2×10^{19} cm^{-3}), allowing investigation of the metal-insulator transition (MIT), which in bulk Si occurs at $n_D \sim 3 \times 10^{18}$ cm^{-3} [92, 96]. Figure 3.14c shows the evolution of R_s (top) and N_e (bottom) versus temperature for these samples. Two contrasting trends are observed: the two lightly doped samples show increasing R_s with decreasing temperature, while the highly doped samples show the opposite trend.

For the lowest n_D, the strong increase of R_s at low temperature correlates with the decrease of N_e, consistent with semiconductor-like behavior controlled by thermally activated dopant ionization. Below 100 K, the resistance exceeds the instrument detection limit, as a result of carrier freeze-out. In the more resistive samples, R_s and N_e change only slightly at higher temperatures but vary significantly below 20 K. As n_D increases toward the critical metal-insulator transition value, dopant wavefunctions overlap, forming a dopant band within the Si bandgap, reducing the energy gap between the dopant level and the conduction

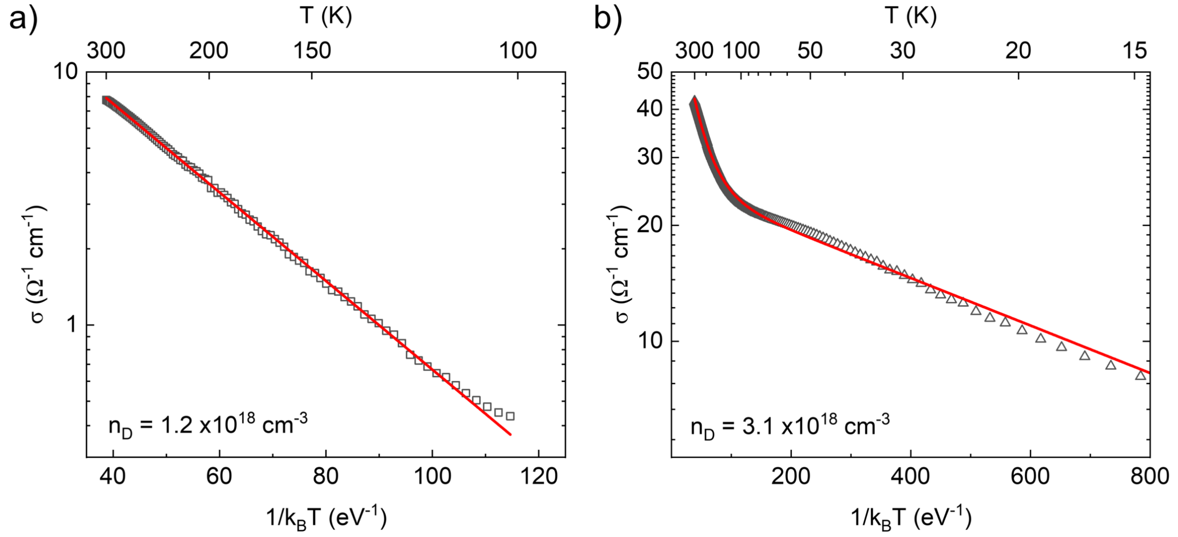


Figure 3.15: The conductivity as a function of the inverse of the temperature for the 30 nm thick SOI samples with $n_D = 1.2 \times 10^{18}$cm−3 (a) and $n_D = 3.1 \times 10^{18}$cm−3 (b). The red line corresponds to the fitting of the data using eq. 3.2 in the temperature range 15–300 K.

band [92]. The smaller energy gap requires less thermal energy for dopants to be ionized, and freeze-out occurs at lower temperatures. In the highly doped samples, conduction persists even at $T = 1.8$ K, suggesting full overlap between the dopant and conduction bands. N_e remains constant over the entire temperature range and correlates with the decrease of R_s. Reduced phonon scattering at low T increases mobility, lowering the sheet resistance, consistent with a metallic Fermi gas [7, 96].

The thermally activated behavior of the semiconductor-like samples was analyzed using a twofold activation energy model:

$$\sigma = \frac{1}{\rho} = A \exp\left(-\frac{E_1}{k_B T}\right) + B \exp\left(-\frac{E_2}{k_B T}\right), \tag{3.2}$$

where E_1 corresponds to the P donor energy level (E_d) and E_2 to the impurity band arising from high n_D [92, 97]. The evolution of the conductivities for two selected SOI samples are reported in Figures 3.15a and 3.15b. The fitting curves in the temperature range from 15 to 300 K are also reported for reference, showing almost perfect compatibility in both of the samples analyzed. Furthermore, the analysis of the low temperature conductivity using a general hopping expression $\sigma \propto \exp[-(T_0/T)^p]$ yielded an exponent $p \approx 0.92$. This value, being close to unity, validates the use of Eq. 3.2 and suggests that even at low temperatures, the system remained in a regime where transport occurs via excitation to extended states or nearest-neighbor hopping, rather than variable-range tunneling. This behavior is likely due to the relatively high n_D causing the presence of extended states in the ultrathin films.

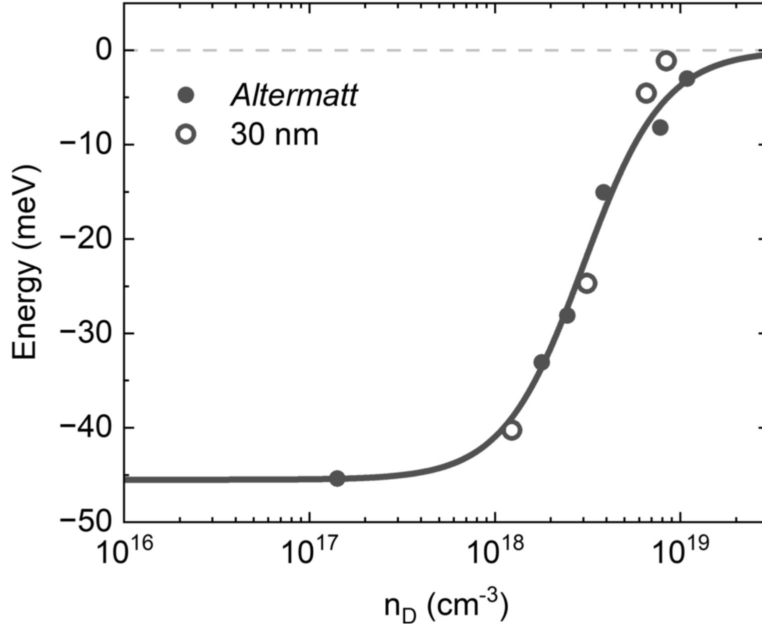


Figure 3.16: Activation energy obtained on SOI samples with $H_{SOI} = 30 \pm 1$ nm by eq. 3.2 versus n_D. The black line corresponds to the fitting function as eq. 3.3 Data obtained by Altermatt *et al.* are reported in the graph for comparison [92].

The computed E_d for all low-temperature, thermally activated SOI samples with $H_{SOI} \sim$ 30 nm are reported in Figure 3.16 as a function of n_D and compared to literature data for similarly P-doped bulk Si [92]. Clear reduction of Ed is observed in Figure 3.16 by increasing n_D. The experimental data were fitted using the model for activation energy reduction at high dopant concentration (black solid line) [92]:

$$E_d = \frac{E_{d,0}}{1 + (n_D/n_{ref})^c}, \tag{3.3}$$

where $E_{d,0} = 45.5$ meV [98], $c = 2$, and $n_{ref} = 3.0 \pm 0.4 \times 10^{18}$ cm^{-3}. These values are consistent with the model for P-doped bulk Si developed by Altermatt [92].

For $H_{SOI} \sim 30$ nm, the experimental results demonstrate the perfect compatibility of this alternative doping strategy, which achieved full activation of the dopants in a wide range of n_D and optimal transport properties which follow the bulk Si model, indicating that the system behaves almost bulk-like in this H_{SOI} and n_D range [38, 39].

3.5 2D confinement

A first set of samples was prepared to investigate the effect of 2D confinement by progressively reducing H_{SOI}. The results presented here are reported in the publication in the *Journal of Materials Chemistry C* journal [39]. The injection of P impurity atoms was investigated by confining the same P dose in progressively thinner device layers, with H_{SOI} ranging from 6 to 70 nm. The P δ-layer source was formed following a single grafting-ashing cycle of the PMMA-P polymer. To promote the drive-in of P atoms into the Si device layer, the samples underwent high-temperature drive-in treatment in the RTP system at T ranging from 900 to 1100 °C in N_2 atmosphere.

Upon drive-in, this first set of samples underwent a different preparation protocol for contact deposition and electrical characterization. The e-beam SiO_2 capping layer was etched in 2% HF bath, and the samples were quickly loaded for Al deposition. Al was deposited through shadow masks at the corners of each sample. After evaporation, the samples were immediately characterized at room temperature using 4PP vdP configuration. The short time between the samples were unloaded from the vacuum chamber and measurement result in good hydrogen passivation of the Si surface, while a thin native oxide layer begins to regrow slowly on the surface.

The P concentration profiles of the SOI samples upon drive-in at 1000 °C for 100 s are reported in Figure 3.17. The ToF-SIMS depth profiles of the 50 and 70 nm thick SOI samples show a P concentration gradient throughout the device layer. The observed concentration profile is correctly predicted by Fick's law of diffusion for thick SOI films [8]. Conversely, when $H_{SOI} \sim 30$ nm, P atoms quickly reach the Si/SiO_2 BOX interface during diffusion. As the BOX acts as a diffusion barrier (Figure 1.7a), the dopants are confined within the thin Si layer; continued thermal treatment leads to the flattening of the concentration gradient as the finite volume of the device layer becomes uniformly occupied. For this specific drive-in thermal treatment, uniform P concentration throughout the entire device layer is achieved only in the case of the samples with $H_{SOI} \leq 30$ nm.

Figure 3.18a shows the total P dose (N_D, blue line) injected in the device layer, computed as the integral of the P concentration depth profile obtained by ToF-SIMS analysis. Data were obtained by averaging the P doses obtained across several samples annealed in the same RTP conditions with the same nominal H_{SOI}. In the SOI samples with $H_{SOI} > 6$ nm, N_D is found to be constant within experimental error. The average P dose was determined to be $N_D \sim (1.0 \pm 0.2) \times 10^{13}$ cm^{-2}.

Figure 3.17 shows an apparent increasingly higher P signal at the device layer/BOX interface when reducing H_{SOI}. As discussed in Section 3.2.1, this feature is treated qualitatively due to SIMS matrix effects, although it suggests a possible P segregation at the interface. The N_D reduction that is observed in the 6 nm thick sample, is therefore attributed to a fraction of P atoms lost due to P diffusion in the BOX, in agreement with the previous discussion about P diffusivity in Si and SiO_2 under similar annealing conditions [38].

Figure 3.18a shows the N_e values (black line), obtained by Hall measurements at room

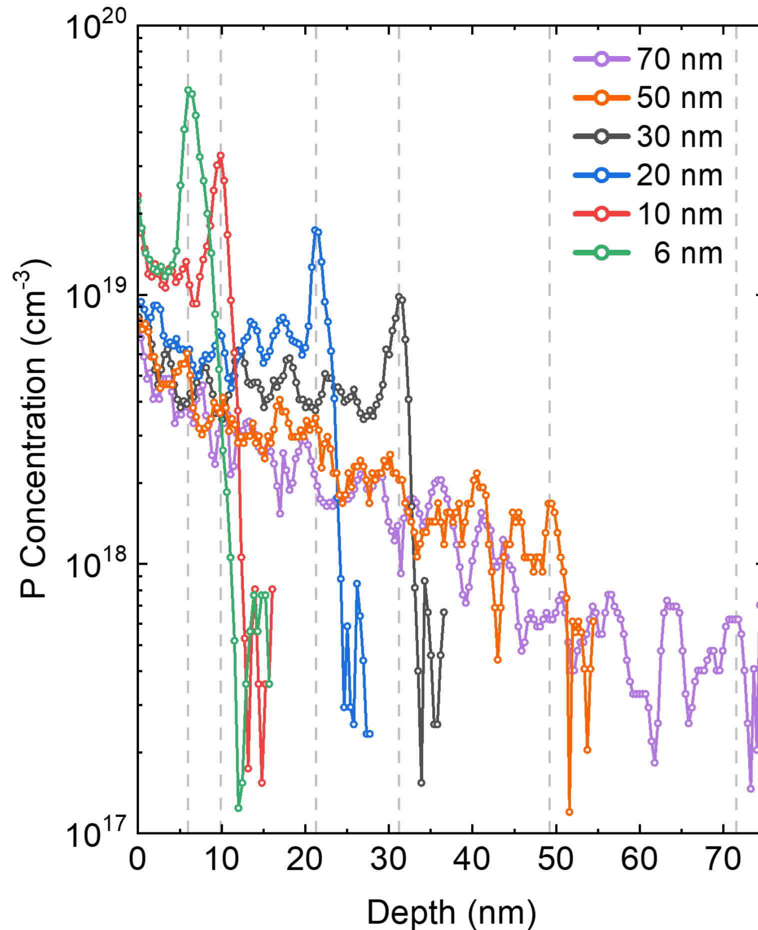


Figure 3.17: ToF-SIMS P depth profiles of SOI samples with H_{SOI} ranging from 6 to 70 nm upon drive-in at 1000 °C. Grey dashed lines indicates the position of the BOX interface.

temperature, as a function of H_{SOI}. Almost complete activation and full ionization is achieved when $H_{SOI} \geq 30$ nm, consistent with previous results [38]. Since the doping procedure and annealing temperature is the same, the full activation condition should be independent on H_{SOI} and be achieved in all samples. However, apparent incomplete ionization is observed by the significant reduction of N_e/N_D ratio. This effect significantly increases when decreasing $H_{SOI} < 20$ nm, achieving a minimum ~ 5% when $H_{SOI} \sim 6$ nm.

Figure 3.18b and Figure 3.18c reports the R_s and μ_e values as a function of H_{SOI}, respectively. μ_e is computed by combining R_s and N_e according to the equation 2.13. The R_s value progressively increases when reducing H_{SOI}. The large error bars associated with N_e and R_s values obtained in the samples with $H_{SOI} \sim 10$ nm are attributed to the high sensitivity of these ultrathin SOI films to the surface termination at the time of characterization. Specifi-

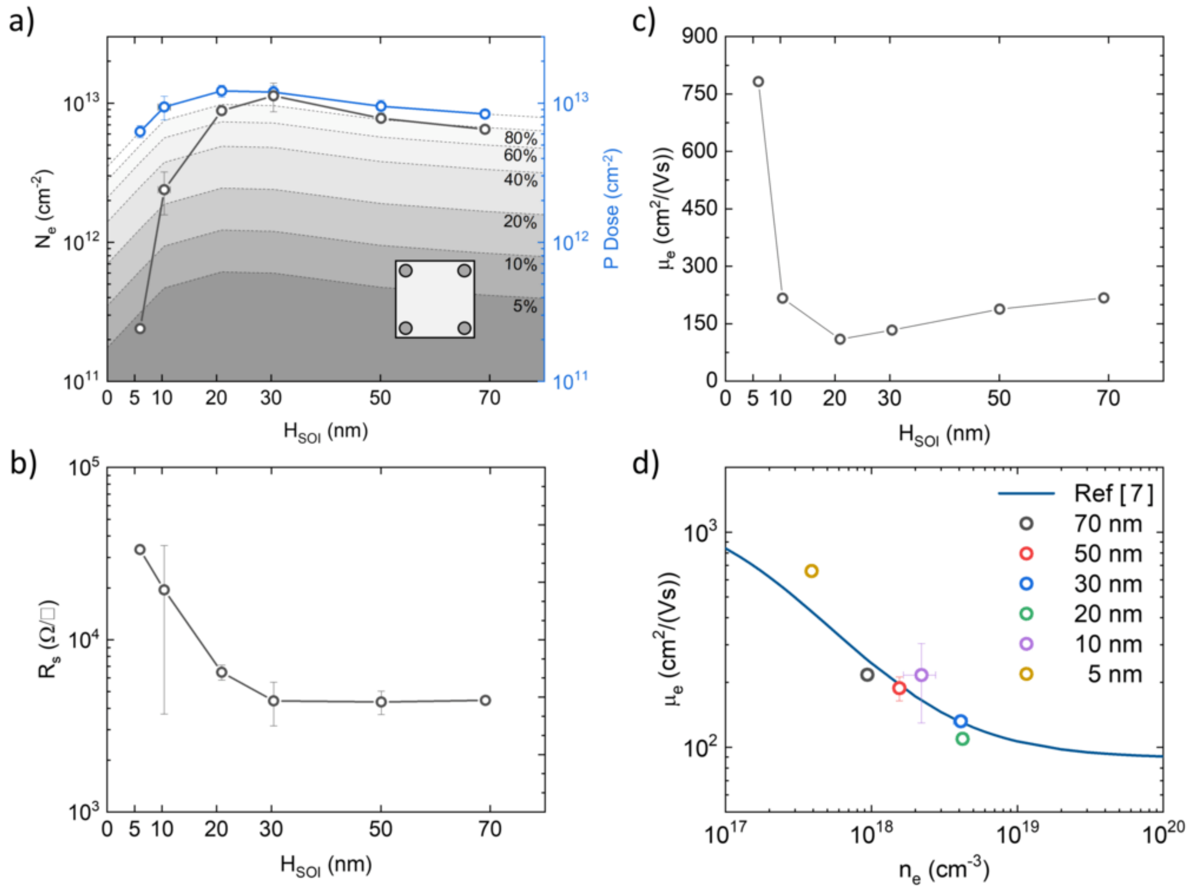


Figure 3.18: (a) The total P dose computed from analysis of ToF-SIMS depth profiles (blue) and the dose of charge carriers (N_e) obtained by Hall measurements (black) for the SOI samples upon drive-in at 1000 °C. Dashed lines correspond to different dopant activation rates. (b) Sheet resistance R_s and (c) carrier mobility μ_e versus H_{SOI} for the same set of samples. (d) μ_e versus the average carrier concentration n_e. Blue solid line indicates electron mobility in bulk Si [7].

cally, variations in the transfer time between vacuum removal and characterization resulted in different degrees of hydrogen passivation. A more detailed description of the physical mechanisms responsible for this phenomenon is provided later in this Section and in Section 3.6.1.

The mobility progressively decreases until $H_{SOI} \sim 20$ nm, consistent with the idea of increased Coulomb scattering that correlates with the progressive increase in n_e observed in Figure 3.18a as H_{SOI} is reduced. These mobility values are perfectly compatible with those reported for bulk Si [7] as shown in Figure 3.18d. Interestingly, a strong increase in electron mobility is observed when $H_{SOI} < 20$ nm, with values even higher than those reported for

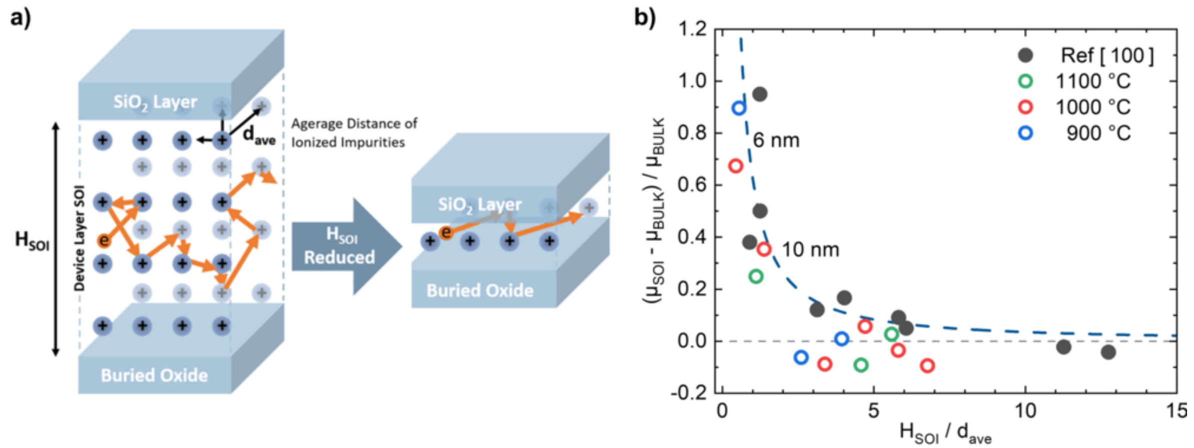


Figure 3.19: (a) Schematic representation of ionized impurities and the effect of Coulomb scattering on an electron in a thick or ultra-thin SOI. (b) Relative mobility versus H_{SOI}/d_{AVE}, for SOI samples upon drive-in at different temperatures. Experimental data (open circles) are compared to those reported in the literature (black) [99].

bulk Si. This trend is consistent with data in the literature for highly doped SOI samples and can be explained assuming that the H_{SOI} reduction causes a transition from 3D to quasi-2D Coulomb scattering [99].

Figure 3.19a depicts a schematic representation of ionized impurities and the effect of Coulomb scattering on an electron moving in a thick or ultra-thin doped SOI. When H_{SOI} is similar to the average distance between ionized impurities ($d_{ave} = n_e^{-1/3}$), the number of Coulomb scattering ions surrounding an electron decreases because no ions exist outside the Si device layer plane. The reduced number of neighboring ionized dopants results in reduced Coulomb scattering and leads to enhanced mobility [99].

To effectively describe this effect, it is necessary to consider both H_{SOI} and the concentration of ionized scattering centers. Following the procedure described by Kadotani *et al.* [99], the variable defined as H_{SOI}/d_{ave} should lead to a universal relative mobility increase. Interestingly, the relative mobility, defined as the mobility increase with respect to the expected bulk mobility, is found to increase when decreasing H_{SOI}/d_{ave} (Figure 3.19b). When $H_{SOI}/d_{ave} \sim 1$, a significant rise of the relative mobility is observed, with values even double those expected for bulk Si.

Figure 3.19b reports the electron mobility values of the SOI films annealed at 1000 °C for 100 s (red open circles). The results obtained from two other sets of samples are also shown in Figure 3.19b. These SOI samples were prepared and characterized following the same sample preparation protocol but varying the temperature of the drive-in process of the dopants from 900 °C (blue open circles) to 1100 °C (green open circles). The duration of each annealing was properly adjusted to inject into the device layer the same $N_D \sim 1.0 \times 10^{13}$ cm^{-2}.

As shown in Figure 3.19b, the experimental data follow the same universal curve irrespec-

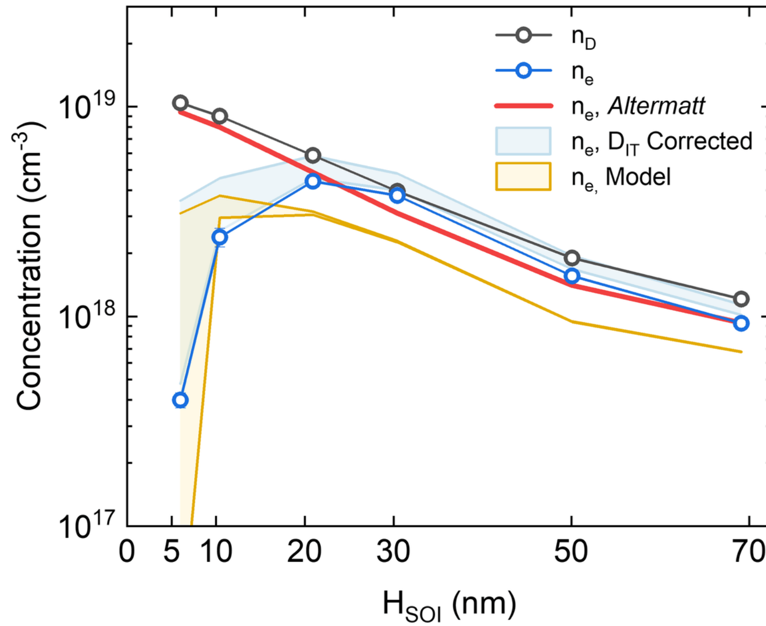


Figure 3.20: The average P concentration obtained by ToF-SIMS analysis (black) and the carrier concentration computed by Hall measurements (blue) versus H_{SOI} upon drive-in at 1000 °C. The measured electron concentration corrected considering the effect of the D_{IT}, the electron concentration predicted by the incomplete ionization model of Altermatt *et al.* [92] and the range predicted by the 1D dielectric mismatch model of Bjork *et al.* [30] corrected considering the reduction of E_I, are shown for comparison.

tive of the annealing temperature and are fully compatible with those reported by Kadotani *et al.* (black closed symbols), indicating that the model provides a consistent picture of the system, particularly for the ultra-thin SOI samples, where the increased electron mobility is observed [99].

Data in Figure 3.18a demonstrate a significant apparent incomplete ionization for $H_{SOI} <$ 20 nm. In principle, this reduction of N_e could be ascribed to incomplete ionization associated with the variation of P concentration in the conductive channel. Figure 3.20 shows the average P concentration in the device layer as obtained by ToF-SIMS analysis. P concentration progressively increases as H_{SOI} is reduced. The average electron carrier concentration n_e, reported in Figure 3.20, is derived as the ratio between the N_e value obtained by Hall measurements and H_{SOI}.

The model of incomplete ionization proposed by Altermatt *et al.* [92] predicts that more than 80 % of the dopants is expected to be ionized and, considering the n_D range, the percentage of ionized impurities is actually expected to increase as the P concentration increases, i.e., reducing H_{SOI}. The $n_{e,Altermatt}$ expected to be ionized at room temperature, computed using the parametrization of Abenante [100] of the model proposed by Altermatt

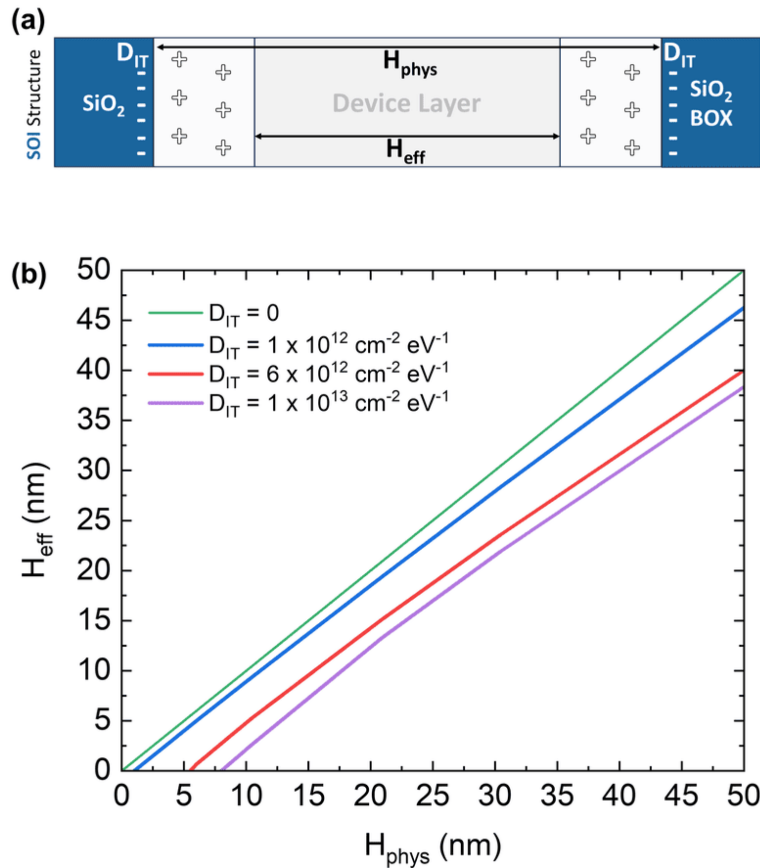


Figure 3.21: (a) Schematic representation of the effect of trapped charge carriers at the interfaces, reducing the effective thickness of the conductive channel (H_{EFF}). (b) H_{EFF} versus H_{SOI} calculated solving the Poisson equation considering the average P concentration obtained by ToF-SIMS analysis.

et al. [92], is shown (red solid line) in Figure 3.20. The model correctly predicts, within the experimental error, the values recorded for the SOI samples with $H_{SOI} \geq 20$ nm but does not account for the strong decrease of N_e observed in the ultra-thin SOI. When $H_{SOI} < 20$ nm, the model developed for bulk Si cannot be directly applied and needs to be corrected because interface and confinement effects are expected to occur due to the increased surface-to-volume ratio.

The first interface effect to be considered is the presence of non-passivated interface traps between the Si and the surrounding. Since the samples were measured immediately after removal from the vacuum following the HF treatment, the density of these traps could be be substantially reduced. Nevertheless, a very thin SiO_2 layer is still assumed to form, which gradually grows over time.

Figure 3.21a shows a schematic representation of the effect of interface states in a n-type SOI. A more detailed investigation of this phenomena will be presented in Section 3.6. Interface states trap negative charges at the SiO_2/Si interface, resulting in a depletion of mobile charges near the interface [101]. As a result, the effective thickness of the conductive channel (H_{eff}) is lower than the physical thickness of the device layer (H_{SOI}).

The dimensions of the depleted region can be computed by solving the 1D Poisson equation, assuming both interfaces are identical, considering the full depletion approximation, and imposing the charge neutrality condition. Figure 3.21b shows H_{eff} plotted against H_{SOI} for various density of interface states (D_{IT}) values. As D_{IT} increases, H_{eff} is reduced considerably. The graph was computed considering the average dopant concentration in the device layer obtained by ToF-SIMS analysis, which increases as H_{SOI} is reduced. Higher n_D leads to smaller depletion regions created by interface states, ultimately resulting in a small difference between H_{SOI} and H_{eff}.

Figure 3.21b suggests a maximum D_{IT} value of $\sim 6 \times 10^{12}$ cm^{-2} eV^{-1}. Above this threshold value, the model predicts that the 6 nm thick SOI should be fully depleted, resulting in no conduction during the electrical characterization. The correct D_{IT} value could vary when H_{SOI} is reduced. In particular, we expect a higher D_{IT} value as n_D is increased due to the enhanced segregation of the P dopants at the interfaces, potentially causing additional traps and doping-induced defects [102]. Additionally, according to the literature, D_{IT} values between 1 and 6×10^{12} cm^{-2} eV^{-1} are appropriate for non-passivated Si/SiO_2 interfaces [103, 104].

Accordingly, to correctly compute the average carrier concentration in the conductive layer, we must divide the N_e values by H_{eff} and not H_{SOI}. The corrected carrier concentration value in the conductive channel varies in the blue range shown in Figure 3.20, which was computed considering the reduction of H_{eff} for D_{IT} values ranging between 1 and 6×10^{12} cm^{-2} eV^{-1}.

Figure 3.20 clearly indicates that there is no significant difference when comparing the lower limit to the one without any effect of interface states. However, increasing the D_{IT} to 6×10^{12} cm^{-2} eV^{-1} results in a significant increase in the average carrier concentration in the conductive channel. The reduced dimensions of the conductive channel could contribute to the significant N_e reduction observed in Figure 3.18a.

However, the correct D_{IT} value may differ from the proposed upper limit, and even after considering the effects of interface states, the experimental data for these ultra-thin SOI differ from the values predicted by the model proposed by Altermatt *et al.* [92]. It is important to note that these samples were measured soon after removal from vacuum, resulting in improved H-passivation. The apparent incomplete ionization could arise from other significant effects.

The second interface effect to be considered is the dielectric mismatch between Si and SiO_2. This effect was highlighted in Si nanowires by Bjork *et al.* [30]. Nanostructures usually exhibit sharp dielectric interfaces with their surroundings. These dielectric mismatches are responsible for significant self-energy corrections to the band structure [105].

When an electron is injected into a solid, it repels nearby valence electrons [106]. In nanostructures, this charge accumulates around the dielectric interfaces in the vicinity of the impurity, leading to an extra term in the Coulomb potential [105]. The interaction between the electron and these image charges is responsible for the additional self-energy correction to the band structure. The total charge seen far from the impurity as well as the potential is asymptotically unscreened [31]. Diarra *et al*. theoretically studied dopant deionization due to dielectric mismatch between a nanowire and its surroundings. This additional contribution to the tight-band Hamiltonian leads to a strong increase in the ionization energy of the dopants [31]. Using their model, an expression for the change in impurity ionization energy (E_I) with respect to the ionization energy in bulk Si (E_I^{BULK}) is obtained:

$$E_I - E_I^{BULK} \approx \frac{2e^2}{\varepsilon_{in}} \frac{\varepsilon_{in} - \varepsilon_{out}}{\varepsilon_{in} + \varepsilon_{out}} \frac{1}{R} F\left(\frac{\varepsilon_{in}}{\varepsilon_{out}}\right), \tag{3.4}$$

where R is the effective radius of the nanowire, ε_{in} and ε_{out} are the dielectric permittivities of Si and the surrounding medium, respectively, and F is a function of the dielectric ratio of the wire to the surroundings [105]. Due to the presence of a very thin SiO_2 layer in this set of SOI samples, which gradually grows over time, the dielectric mismatch effect, and consequently the correction to E_I, could be significant, as the Si is effectively surrounded by air on one side rather than SiO_2 ($\varepsilon_{air} < \varepsilon_{SiO_2}$).

The geometry of our system is planar rather than cylindrical. However, following the 1D radial parametrization given by eq. 3.4, we believe it accounts for the maximum contribution of the dielectric mismatch between Si and the surrounding. To our knowledge, this represents a necessary approximation, as a theoretical model specifically accounting for 2D dielectric mismatch in planar SOI films is still missing in the literature. In our system, n_D increases when H_{SOI} is reduced. As a consequence, E_I^{BULK} cannot be kept constant, as it decreases when n_D is increased [92]. E_I^{BULK} was then evaluated using the incomplete ionization model of Altermatt *et al*. [92].

We assume that the two opposite contributions to E_I, caused by the increase in n_D and the effect of dielectric mismatch, can be independently determined and that their overall effect can be accounted for by a simple additive procedure. The R parameter in eq. 3.4 was assumed as $H_{eff}/2$. The carrier concentration values expected considering the effect of the dielectric mismatch are reported in the bronze range in Figure 3.20, for D_{IT} values between 1 and 6×10^{12} cm^{-2} eV^{-1}. When D_{IT} increases, H_{eff} decreases, resulting in a higher E_I correction from eq. 3.4.

Interestingly, the model significantly underestimates the fraction of ionized P impurities when $H_{SOI} \geq 20$ nm. The same effect was observed in the original paper of Bjork *et al*., in which less than 30 % of dopants were assumed to be ionized at room temperature, even in the case of thick nanowires ($R \geq 30$ nm) and high P concentrations ($n_D = 3 \times 10^{19}$ cm^{-3}) [30]. In this respect, it is worth noting that the 1D dielectric mismatch parametrization is based on the incomplete ionization model of Xiao *et al*. [107], which assumes a constant E_I^{BULK} and strongly overestimates the incomplete ionization in bulk Si when $n_D > 10^{18}$ cm^{-3} [92].

When $H_{SOI} \geq 30$ nm, the experimental results were perfectly described by the incomplete ionization model for bulk Si of Altermatt *et al*. (red line in Figure 3.20) further supporting the idea that above this threshold the system behaves like bulk Si. Conversely, when $H_{SOI} \leq$ 20 nm, E_I rapidly increases, and the proposed model predicts a significant apparent dopant incomplete ionization. In particular, the model underestimates the ionization observed in the 6 nm thick SOI when $D_{IT} = 1 \times 10^{12}$ cm^{-2} eV^{-1} but tremendously overestimates the ionization when $D_{IT} = 6 \times 10^{12}$ cm^{-2} eV^{-1}, with n_e values dropping lower than 3×10^{16} cm^{-3}. In this D_{IT} range, n_e values predicted by the 1D dielectric mismatch model overlap the n_e values measured and corrected to account for the reduction of H_{eff}.

The apparent incomplete ionization observed in these ultra-thin SOI samples measured quickly after removal from vacuum could be tentatively described by the significant increase in E_I and the effect of the interface states, assuming a D_{IT} value in the proposed range. A 2D parametrization in planar geometry would be necessary to further improve the accuracy of the proposed model. Additional quantum confinement phenomena could expected to play a role in SOI samples when H_{SOI} is approximately 2 times the effective Bohr radius of P in Si [108].

Finally, it should be noted that this first set of samples featured an uncontrolled interface and a constant P dose, which correlated the variation of the thickness of the film with the dopant concentration in the Si device layer. Therefore, further systematical studies were conducted to properly discriminate between each interface effects and investigate the independent contribution of H_{SOI} and n_D.

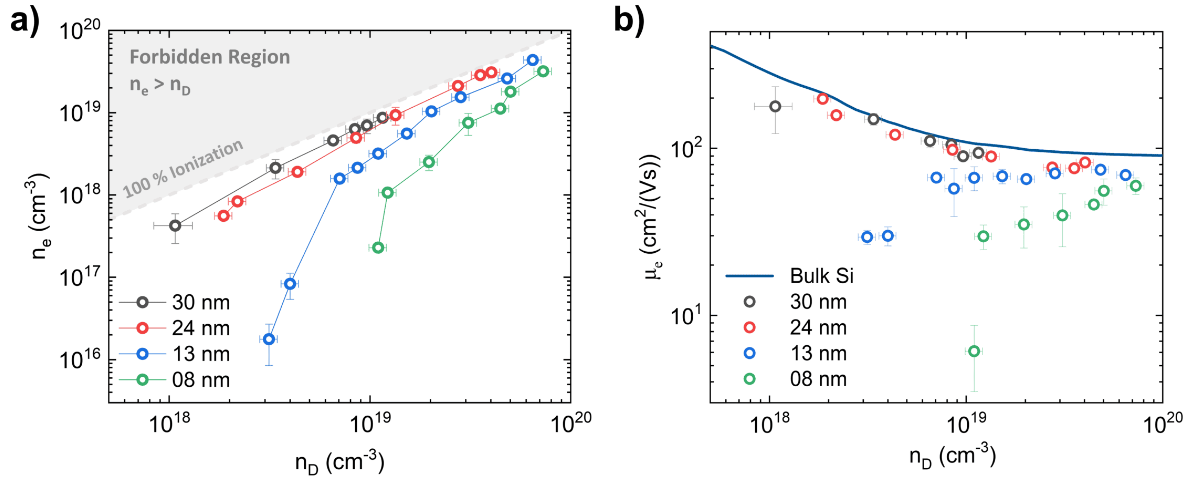


Figure 3.22: (a) The concentration of charge carriers (n_e) vs the total dopant concentration (n_D) for SOI with variable H_{SOI}. (b) mobility (μ_e) values as a function of n_D for the same SOI samples. Electron mobility in bulk Si (line) is shown for comparison [7].

3.6 Interface states and dielectric mismatch

To investigate the impact of interface states and dielectric mismatch at the SiO_2/Si interface on dopant activation and ionization in ultrathin SOI layers, a series of samples with H_{SOI} ranging from 24 nm down to 8 nm were fabricated and doped using PS-P polymers. By systematically varying the processing parameters, as described in Section 3.2, it was possible to tune the incorporated dopant concentration over more than two orders of magnitude. This approach allowed a comprehensive analysis of how dopant activation, ionization, and transport properties evolve with both H_{SOI} and n_D independently, thereby providing insight into the fundamental mechanisms involved in P incorporation and activation in ultrathin SOI structures.

Figure 3.22a reports the results of electrical and compositional analysis in the case of SOI samples with $H_{SOI} = 24 \pm 1$, 13 ± 1 and 8.2 ± 0.4 nm. The results already discussed in section 3.4 for $H_{SOI} \sim 30$ nm are also reported for comparison. For these ultrathin samples the n_e values are really far away from 100 % ionization, with η_a values quickly dropping well below 10 % when decreasing n_D. The collected data clearly indicate that lower n_D and stronger 2D confinement (lower H_{SOI}) result in significantly lower n_e values. These results apparently suggest the occurrence of a dopant incomplete ionization, which is progressively increasing when both H_{SOI} and n_D are reduced. As briefly discussed in section 3.4, a similar effect was observed in the 30 nm thick SOI samples with $n_D \sim 1 \times 10^{18}$ cm^{-3}, exhibiting a n_e value that corresponds to an average $\eta_a \sim 55$ %. Interestingly, at high n_D values, the effect is progressively reduced, and no signature of incomplete ionization is observed, even in the case of ultrathin SOI with $H_{SOI} \sim 13$ and 8 nm.

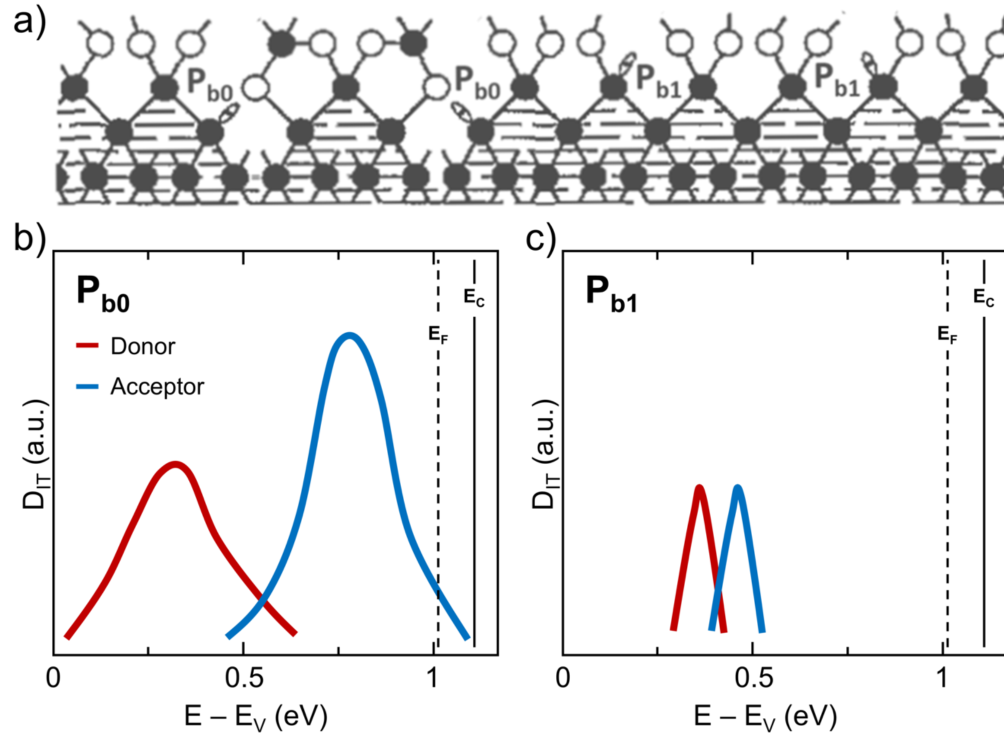


Figure 3.23: (a) P_{b0} and P_{b1} defects located at a (100) SiO_2/Si interface. Estimated density of states distribution of P_{b0} (b) and P_{b1} (c) centers at the (100) SiO_2/Si interface. The positions of the conduction band minimum (E_C) and Fermi level (chemical potential, E_F) for a doped *n*-type Si ($n_D \sim 10^{18}$ cm^{-3}) are indicated for reference.

These phenomena cannot be explained on the basis of the model proposed by Altermatt [92]. In Section 3.5, it was observed that when H_{SOI} is reduced below 30 nm, this model, that was developed for bulk Si, cannot be directly applied to ultrathin SOI substrates, because of the combined effect of the TOX and BOX interfaces [39]. In particular, as surface-to-volume ratio increases, conducting properties transition away from a bulk-like to an interface-driven behavior.

3.6.1 Interface states

At this level, the main interface effect to be considered is the presence of non-passivated interface state traps at the SiO_2/Si TOX and BOX interfaces. These interface states are strictly related to the presence of different types of Si dangling bonds, like P_{b0} and P_{b1} , which are typically located at a (100) SiO_2/Si interface [109]. A schematic representation of this unfinished Si bond is shown in Figure 3.23a. All types of dangling bonds are reported to be of amphoteric nature [110, 111, 112]. Their energy distribution comprises of two

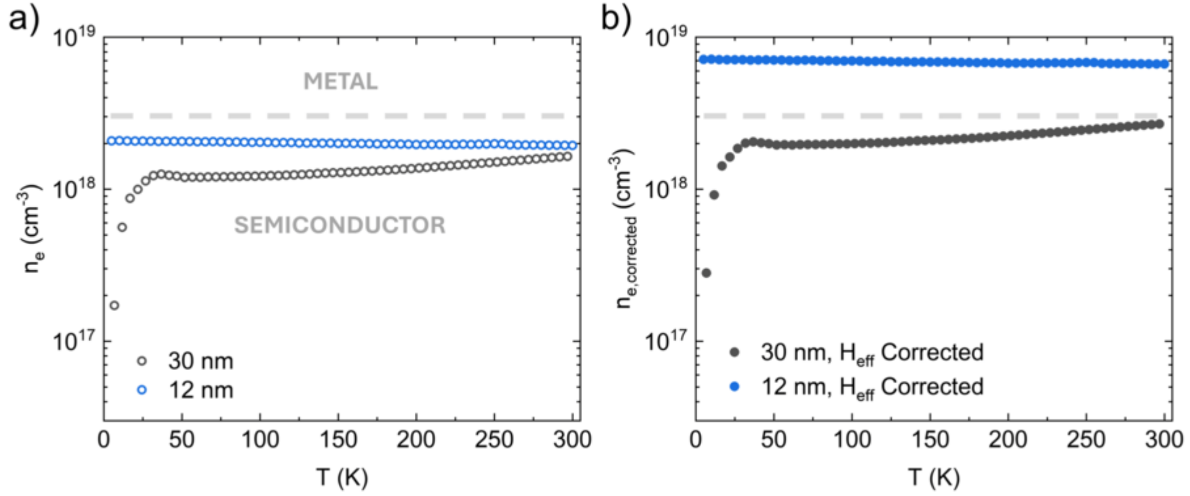


Figure 3.24: (a) Low temperature carrier concentration n_e evolution for samples with different H_{SOI} showing the same n_e at room temperature . (b) n_e values are corrected considering the reduction of H_{eff}.

distinct peaks in the Si band-gap, located in the lower and upper half of the band-gap, which introduce donor-like and acceptor-like energy levels, respectively. The estimated density of states distribution of P_{b0} and P_{b1} centers at the (100) SiO_2/Si interface is shown in Figure 3.23b and Figure 3.23c. The number of P_{b1} centers is assumed to be lower than that of P_{b0} centers, which also exhibit a much broader energy distribution due to their sensitivity to local interfacial disorder and bonding variations [109].

In an *n*-type Si, the Fermi-level (E_F) is located in the upper half of the bandgap, and the acceptor-like energy levels between the Fermi-level and the middle of the bandgap are negatively charged, while the ones above the Fermi-level are neutral. Negative mobile charges trapped in the dangling bonds at the Si/SiO_2 interface do not contribute to charge conduction, which results in a depletion of mobile charges near the interface with the formation of an extended positive space charge region [101]. As a result, the effective thickness of the conductive channel (H_{eff}) is lower than the physical thickness H_{SOI}. As the density of interface states (D_{IT}) of the Si/SiO_2 interface increases, H_{eff} is reduced considerably [39].

By comparing two samples exhibiting the same $n_e \sim 2 \times 10^{18}$ cm^{-3}, as determined at room temperature from Hall effect measurements, but with significantly different H_{SOI}, namely $H_{SOI} \sim 12$ nm and $H_{SOI} \sim 30$ nm, a significant difference in the low-temperature evolution is observed. For this n_e values, both samples would be expected to show similar resistive behavior, since n_e lies below the critical value for the MIT. The evolution of n_e as a function of temperature from 1.8 to 300 K is reported in Figure 3.24a.

The sample with $H_{SOI} \sim 30$ nm behaves as expected for bulk Si, exhibiting a typical

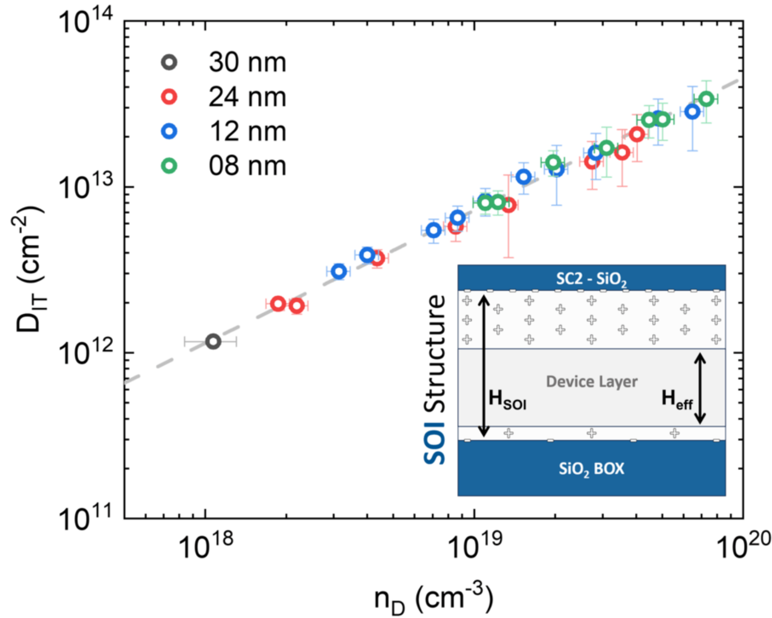


Figure 3.25: D_{IT} values of SC2-SiO_2/Si interfaces vs n_D for SOI with different H_SOI estimated using eq. 3.6. In the inset, schematic representation of the effect of trapped charge carriers at the interfaces.

thermally activated decrease in n_e due to the energy gap between the dopant band and the conduction band. Specifically, n_e decreases slightly as temperature is lowered and then drops sharply below 20 K when strong freeze-out of the P dopants occurs. In contrast, the sample with $H_{SOI} \sim 12$ nm shows nearly temperature-independent conduction, suggesting the complete overlap between the conduction and dopant bands, indicative of metallic behavior. This significant difference is linked to the effect of the apparent incomplete ionization. Actually, in the thinner sample, the donor concentration n_D is substantially higher, exceeding 8.5×10^{18} cm^{-3} and remains high in the very thin conductive channel whose thickness is highly reduced by the presence of non-passivated interface states.

The corresponding corrected n_e values, computed from Ne values obtained by Hall measurements considering the reduction of H_{eff}, is shown in Figure 3.24b for comparison. For the thicker sample with $H_{SOI} \sim 30$ nm, the influence of the D_{IT} on the H_{eff} is negligible since only a small correction is introduced. However, in the thinner sample, the correction introduce a significant shift since it yields an effective $H_{eff} \sim 3.5$ nm.

The corrected data reveal the expected semiconducting and metallic behavior, positioning the $H_{SOI} \sim 12$ nm sample above the critical MIT value further supporting the idea that conduction occurs within a effective thinner layer, significantly smaller than the physical thickness of the device layer.

The inset of Figure 3.25 shows a schematic representation of the SOI structure elucidating

the typical effect of the TOX and BOX interfaces in *n*-type-doped SOI. In section 3.5, the proposed interpretation assumed perfectly equal and symmetric contribution coming from the two Si/SiO_2 interfaces [39]. Experimental data herein reported suggests that the most dominant contribution is to be attributed to the TOX interface, as will be discussed in the next section. In general, the quality of the chemically grown SC2-TOX is worse than the pristine and as-fabricated BOX, leading to a larger depletion zone around the Si/TOX interface. It is important to note that the overall reduction of H_{eff} is not affected by the effective distribution of the depletion layers in the device layer at the different interfaces.

The intensity of the effect of interface states is directly related to both n_D and H_{SOI}. Lower n_D implies larger depletion regions to fully compensate for the D_{IT}. As shown in the case of the lowly doped sample with $H_{SOI} \sim 30$ nm, a non-negligible contribution can be introduced even in the case of thick SOI. Similarly, if H_{SOI} is reduced, a proportionally bigger fraction of the volume of the device layer is depleted resulting in an apparent incomplete ionization of the dopant with a significant reduction of n_e that could ultimately lead to a fully depleted Si device layer.

This apparent incomplete ionization strongly correlates with the degradation of the mobility observed in the inset of Figure 3.22a in the case of ultrathin SOI. For a fixed H_{SOI} value, the μ_e values are significantly reduced at low n_D but they approach bulk mobility values at high n_D. Experimental data clearly suggest a relation with the dimensions of the depleted regions created by interface states. Moreover, the mobility degradation is progressively enhanced when reducing the H_{SOI} value. This effect cannot be explained considering scattering induced by interface roughness. Mobility degradation is clearly observed already in SOI samples with $H_{SOI} \sim 13$ nm, while interface roughness is typically expected to play a major role only for $H_{SOI} < 5$ nm [113]. Additionally, considering the samples with $H_{SOI} \sim 8$ nm, μ_e is observed to increase as n_D increases. This is totally counterintuitive since in bulk Si, higher n_D is associated with a larger number of ionized dopants and consequently to a higher Coulomb scattering contribution determining a mobility degradation.

Accordingly, mobility evolution in ultrathin SOI substrates suggests a physical mechanism that is significantly different from the typical bulk-like one. Depleted regions are characterized by the presence of a space charge determined by the impurity ions that act as scattering centers for the electrons traveling in those regions. Impurity scattering contribution is greatly enhanced in those regions because Thomas-Fermi screening of ions is almost negligible [114, 115]. Higher n_D results in smaller depleted regions and higher screening.

The values of the total D_{IT} which would result in such apparent incomplete ionization, can be estimated by assuming full depletion of the space charge region, i.e., assuming an abrupt transition between the depletion layer and the non-depleted semiconductor material. According to the incomplete ionization model of Altermatt the density of electrons $N_e^{\text{Altermatt}}$ in the device layer is directly connected to the active dopant concentration by the following equation:

$$N_e^{\text{Altermatt}} = n_D \, f^{\text{Altermatt}}(n_D) \, H_{SOI} \tag{3.5}$$

where $f^{Altermatt}$ is the donor ionization fraction [92]. The difference between the calculated $N_e^{Altermatt}$ value and the measured N_e value indicates the amount of electrons trapped at interface states. Accordingly, we calculate the total D_{IT} as:

$$D_{IT} = \Delta N = N_e^{Altermatt} - N_e \tag{3.6}$$

Moreover, once the total D_{IT} contribution in each sample is known, the effective thickness H_{eff} is computed by subtracting the portion of the conductive channel that is depleted from H_{SOI}:

$$H_{eff} = H_{SOI} - \frac{D_{IT}}{n_D \, f^{Altermatt}(n_D)} \tag{3.7}$$

The calculated total D_{IT} values are plotted in Figure 3.14d as a function of n_D for all the different H_{SOI} values. In addition, since we are considering highly doped Si substrates, the Fermi level is expected to be close to the conduction band minimum. Consequently, the calculated D_{IT} values account for almost all the acceptor-like interface state in the upper half of the Si bandgap. It is important to note that the present D_{IT} values have been calculated using the model of incomplete ionization that was developed for bulk Si by Altermatt. Its direct application to ultrathin SOI films represents a first order approximation that still provides a physically motivated estimate of the fraction of active P dopants, allowing the evaluation of both H_{eff} and n_D.

The computed D_{IT} values for $H_{SOI} \sim 24$, 13 and 8 nm are consistent with the range reported in the literature for similarly non-passivated Si/SiO_2 interfaces [103, 104]. The increase in D_{IT} values with higher n_D, as shown in Figure 3.25, could be attributed to enhanced segregation of P dopants at the interface, potentially causing additional traps and doping-induced defects [102]. Interestingly, the computed D_{IT} values for $H_{SOI} \sim 24$, 13 and 8 nm follow the same experimental trend, suggesting a H_{SOI} independent mechanism. The apparent incomplete ionization observed in ultrathin SOI substrates is most significantly driven by the quality of the Si/SiO_2 interfaces and interface states, which are the same SC2 grown in all samples.

To further corroborate this model, electrical paramagnetic resonance (EPR) characterization of the samples at cryogenic temperatures was performed, providing additional information regarding the ionization of the P dopants in the Si device layer, as well as the quality of the SiO_2/Si TOX interface. In particular, EPR measurements at 4.2 K were performed on three reference SOI samples with $H_{SOI} \sim 30$ nm and P concentration ranging from 1 to 5×10^{18} cm^{-3}, as measured by calibrated ToF-SIMS depth profiles. The EPR spectra of these SOI samples are presented in Figures 3.26a and 3.26b. All the spectra are characterized by a broad background signal, which is attributed to the substrate, as confirmed by independent measurements of the pristine SOI substrates [38]. The same background signal is in fact visible in all three substrates. A detailed description of the EPR experimental protocol, including the microwave power saturation studies and the g-factor calibration, is provided in Section 2.2.5.

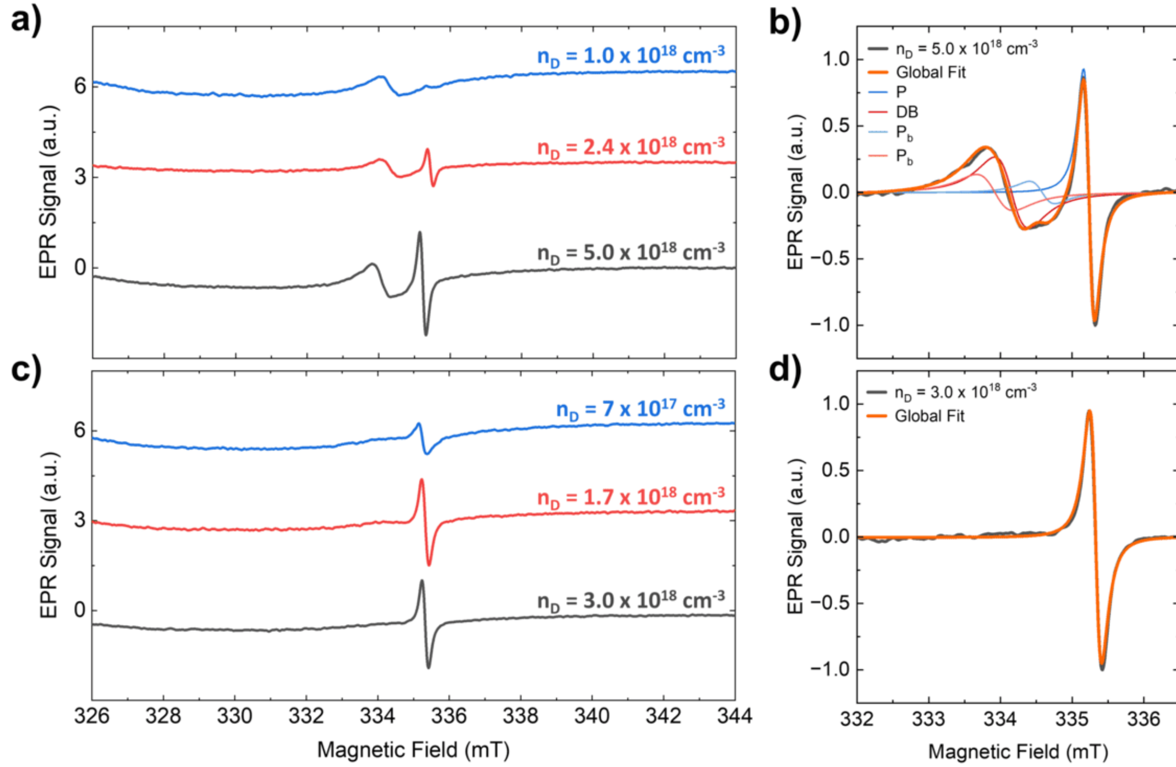


Figure 3.26: (a) EPR spectrum of 30 nm thick SOI doped in various P concentrations with SC2-TOX capping layer. (b) Zoomed view of a representative spectrum from (a). A single P line and a significant bump attributed to DB an P_{b0} centers are detected. (c) EPR spectrum of the same SOI samples upon oxidation at 900 °C. (d) Zoomed view of a representative spectrum from (c). A single P line is detected. The signals attributed to interface defects are significantly reduced close to or below the sensitivity limit of the setup. EPR spectra were acquired at 4.2 K, with B // (011) and microwave power of 1 mW.

A main single line with $g = 1.9991 \pm 0.0005$ and linewidth of 0.15 ± 0.02 mT is detected. This single line is consistent with the P dopants, considering the high n_D value in all the SOI samples [116]. The intensity of the peak is reducing progressively with the reduction of n_D and correlates the reduction of free carriers observed in Figure 3.14a when n_D is reduced. Almost no P signal is detected in the SOI sample doped with the lowest n_D. In addition to the P signal, other EPR resonance lines are observed at higher g-factors. Two lines at $g = 2.0030 \pm 0.0005$ and $g = 2.0070 \pm 0.0005$ are consistent with the P_{b0} centers at the Si/SiO_2 interface [117, 118]. A third line at $g = 2.0056 \pm 0.0005$ can be attributed to Si DBs [119].

The same samples were shortly oxidized at T = 900 °C for 40 s in O_2 atmosphere (RTO). A 5 nm thick SiO_2 TOX film was thermally grown on top of the Si device layer with a

reduction of the Si device layer of about 2 nm. The low annealing temperature is expected to limit P diffusion into the SiO_2 layers surrounding the Si device layer. Additionally, the SC2 layer was not removed prior to the thermal oxidation to prevent a significant out-diffusion of the P dopants from the Si surface during the initial stages of the oxidation process. Upon oxidation, all the samples exhibit a ~ 30% reduction of P concentration, as highlighted by ToF-SIMS analysis.

The EPR spectra of the SOI samples upon oxidation are presented in Figures 3.26c and 3.26d. The spectra are characterized by a similar broad background signal, which is again attributed to the substrate. A main well defined single line is detected and consistent with the presence of conduction electrons generated by the P dopants [116], even in the case of the SOI substrate with the lowest P concentration. The P signal detected in the SOI sample with $n_D = 0.7 \times 10^{18}$ cm^{-3} after oxidation is significantly higher than the one obtained in the pristine sample even if, during oxidation, a fraction of P atoms out-diffused from the Si device layer into the SiO_2 causing a significant n_D reduction. A similar consideration applies for the sample with $n_D = 1.7 \times 10^{18}$ cm^{-3}.

Even more important, the EPR signals associated with the interface defects are significantly suppressed in the samples after the oxidation. Oxidation at 900 °C greatly improves the quality of the Si/SiO_2 interface by reducing the density of interface states at the Si/TOX interface as well as providing field effect passivation [120, 117]. A secondary broader component near the detection limit may still be present, suggesting that a small but finite DIT may persists even after the RTO treatment. No significant improvements of the Si/BOX interface are expected to occur because of the RTO treatment.

These data are fully consistent with the model we proposed to account for the apparent incomplete ionization: a lower D_{IT} results in smaller depleted regions [39] and lower trapping of electrons at the interface determining higher n_e values as observed in the EPR spectra after RTO. These results suggest RTO as a valuable tool to improve Si/TOX interface quality and reduce the trapping of electrons at the interface determining the depletion of the Si device layer.

Accordingly, doped SOI samples with $H_{SOI} \sim 30$ nm were prepared by means of a single grafting-hashing cycle using PS-P (Table S1). Upon drive-in of the dopants, the samples were oxidized in O_2 atmosphere at 900 °C for different times progressively reducing the H_{SOI} to ~ 20.3, 17.8, 14.0 and 10.4 nm. The calibrated ToF-SIMS P depth profiles of these samples after oxidation are reported in Figure 3.27a. The P depth profiles are shifted to align the position of the Si/BOX interface. ToF-SIMS analysis demonstrates a uniform distribution of the P atoms into the Si device layer. No significant P signal is observed in the TOX and BOX films. Moreover, after oxidation, the dopant concentration is almost the same in all samples irrespective of H_{SOI}. The average P concentration in the device layer was determined to be $n_D = (5.9 \pm 0.4) \times 10^{18}$ cm^{-3} and is indicated as a grey dashed line in Figure 3.27b.

Interestingly, the average n_D expected after one doping cycle with this specific PS-P is 9×10^{18} cm^{-3}, confirming a significant 35 % reduction of the P concentration after high temperature RTO. All the samples exhibit the same reduction of P concentration irrespective

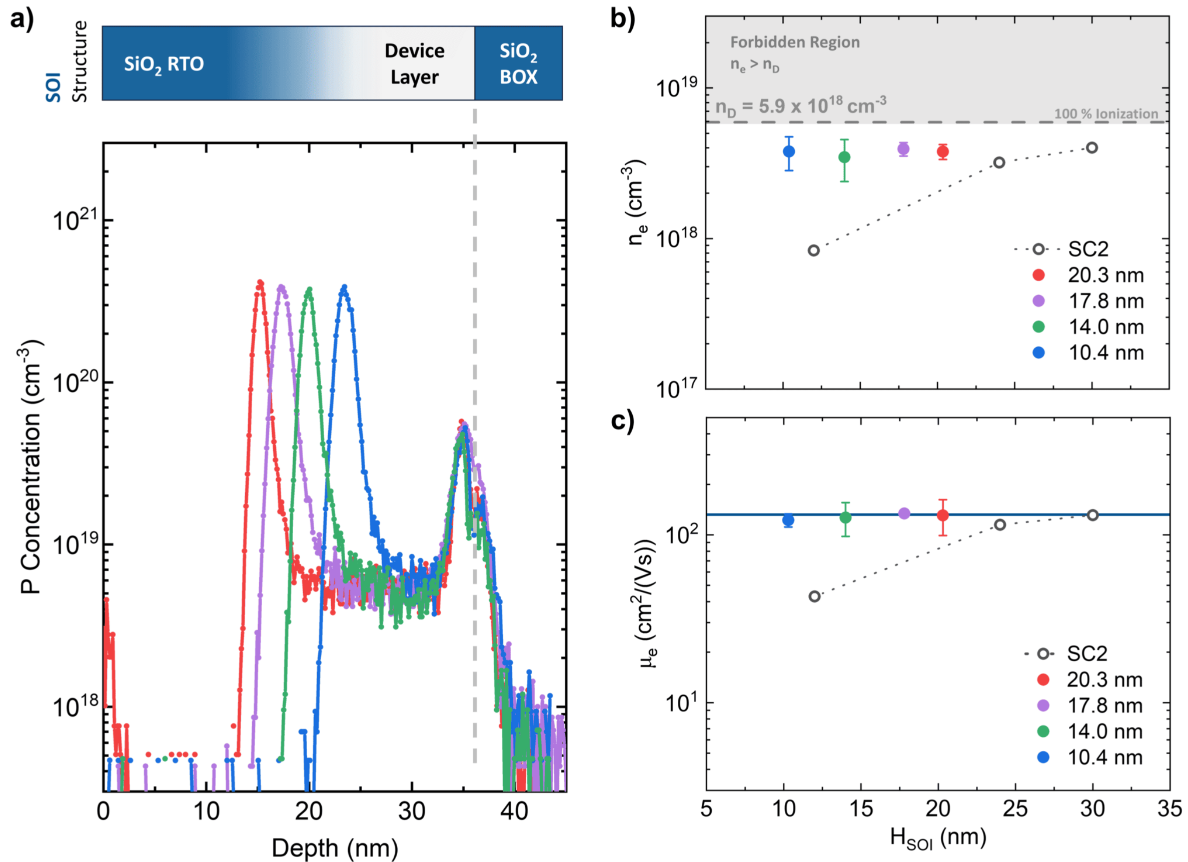


Figure 3.27: (a) ToF-SIMS depth profiles obtained on SOI samples upon RTO at 900 °C. The duration of the treatment was selected to produce H_{SOI} ranging from 10.4 to 20.3 nm. (b) n_e versus H_{SOI} upon RTO vs SC2. Dashed line corresponds to the average n_D value. (c) μ_e versus H_{SOI} upon RTO vs SC2. Blue solid line corresponds to the μ_e value in bulk Si [7].

of the annealing time. Combining these ToF-SIMS data with those obtained in the case of samples used for the EPR analysis, we speculate that this reduction of P concentration is essentially related to a significant out-diffusion of the P atoms taking place during the initial stages of the RTO process, because of the low quality of the SC2-TOX film. Upon formation of a good quality thermal SiO_2 no further reduction of P concentration is observed.

Figure 3.27b shows the carrier concentration n_e obtained from Hall measurements versus H_{SOI} for all the four SOI samples upon oxidation. The results are compared to those (black open symbols) obtained on similarly doped SOI samples capped with a SC2-TOX layer. Figure 3.27b clearly shows a significant increase of n_e in the samples with RTO-TOX capping layer. Moreover, no significant variation of the n_e value is observed when reducing the thickness of the Si device layer. In particular, almost 10 times higher n_e is observed in the

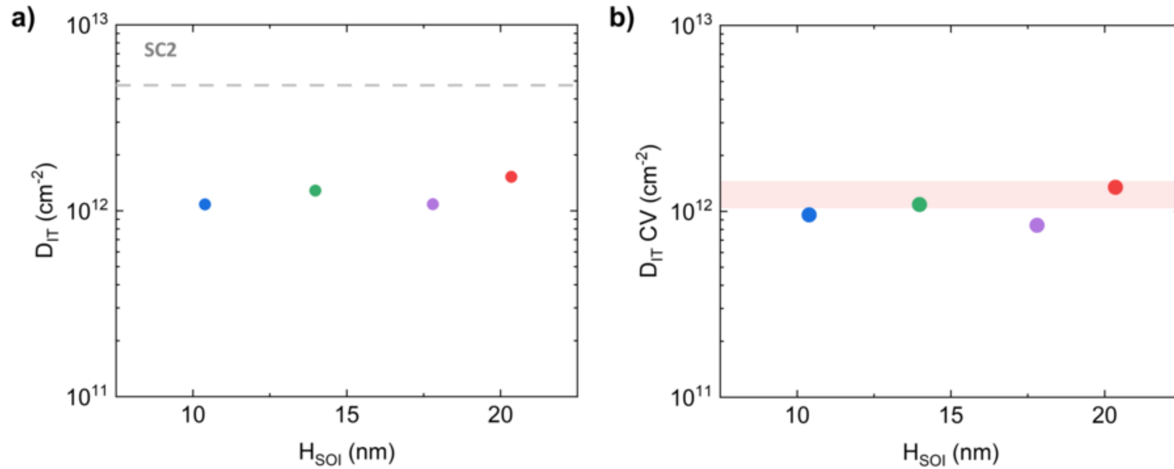


Figure 3.28: (a) D_{IT} versus H_{SOI} computed using eq. 3.6 for the set of samples with RTO-TOX capping layer in Figure 3.27, compared to the average value expected for SOI samples with the same n_D and SC2-TOX capping layer. (b) D_{IT} values obtained by CV measurements versus H_{SOI} for the same set of samples.

SOI sample with RTO-TOX capping layer with $H_{SOI} = 10.4$ nm with respect to the 12 nm thick samples with SC2-TOX capping layer. The n_e values measured in the samples upon RTO processing indicated that an average $\eta_a = 80\%$ was achieved in all samples, within the limit of the theoretical model of incomplete ionization proposed by Altermatt *et al*. [92].

Considering a uniform P distribution in the Si device layers, as demonstrated by ToF-SIMS depth profiles in Figure 3.27a, the μ_e values in the different samples are directly computed by means of eq. 2.13 from the combination of separate sheet resistance and Hall measurements. Figure 3.27c reports the computed μ_e values versus H_{SOI}. The μ_e values are fully consistent with those reported in the literature for bulk Si (blue line) [7]. Mobility values (black open symbols) of SOI films with SC2-TOX capping layer having the same dopant concentration are reported for comparison. The collected data clearly highlight that the degradation of the mobility which was observed in Figure 3.22b reducing the Si device layer thickness is completely recovered replacing the SC2-TOX capping layer with the RTO-TOX capping layer.

The values of the total D_{IT} which result in such a small depletion of the Si device layer are estimated again by matching N_e measured by Hall analysis to the fraction of n_D expected to be ionized at room temperature by the incomplete ionization model of Altermatt. The computed values of the expected D_{IT} are plotted in Figure 3.28a versus H_{SOI}. The average D_{IT} value was determined to be $= (1.1 \pm 0.2) \times 10^{12}$ cm^{-2}. Expected data are compared to the average D_{IT} value computed in the case of sample with SC2-TOX capping layer and $n_D \sim 5.9 \times 10^{18}$ cm^{-3}. A reduction by a factor of 4 is clearly observed in the samples with RTO-TOX capping layer. Better quality of the thermally grown RTO-TOX film and

consequently of the Si/TOX interface results in lower D_{IT} values and lower trapping of charges at the interface states. Accordingly, curing the interface results in almost negligible depleted regions and almost full ionization as well as bulk mobility values even in the case of the ultrathin SOI sample with $H_{SOI} < 30$ nm.

Taking advantage of the high quality of the RTO-TOX capping layer, CV measurements were performed onto simple MOS capacitors using square aluminum contacts deposited by thermal evaporation on top of the RTO-TOX layer. Back contact to the Si device layer was achieved by locally removing the RTO-TOX layer and depositing Al to form an ohmic contact with the Si device. The CV curves were acquired sweeping the applied voltage between inversion to accumulation at frequencies ranging from 1 kHz to 1 MHz in a dark environment in a shielded probe station. CV and conductance curves were analyzed to extract the average D_{IT} value at the Si/TOX interface.

The average D_{IT} values extracted following eq. 2.19 from the analysis of the CV curves, are reported in Figure 3.28b and compared to the average D_{IT} value calculated combining n_D and n_e values obtained form ToF-SIMS analysis and electrical Hall measurements, respectively. Measured D_{IT} values are compatible with those extracted from the results of the electrical and compositional analysis. Interestingly, the D_{IT} values measured in SOI samples with the RTO-TOX capping layer are fully consistent with those measured in bulk Si with the same kind of RTO-TOX (Figure 3.30). It is worth to remember that the D_{IT} extracted from the combination of the electrical and compositional analysis refers to the total amount of interface states which should contribute to trapping to account for the reduction of n_e resulting in an apparent incomplete ionization. Conversely, the D_{IT} extracted from CV measurements refers to only the interface states at the Si/TOX interface without considering the contribution of the Si/BOX interface.

On the basis of the experimental results, we expect that the major contribution to interface states is from the high-quality Si/TOX interface which was significantly modified during the RTO treatment while the Si/BOX interface is essentially unaffected by the thermal treatment. For this reason, in Figure 3.25, the contribution of the two interfaces is assumed to be significantly different with an important channel depletion in the proximity of the Si/TOX interface.

3.6.2 Different interfaces

Because the electrical properties of ultrathin SOI devices strongly depend on the D_{IT} and overall quality of the interface, alternative capping layers and surface passivation techniques were investigated to improve the SiO_2/Si interface. One widely used approach is the forming gas (FG) anneal, which consists of annealing the sample in a hydrogen-rich atmosphere (5% H_2 in N_2) at 400 °C. During FG anneal, hydrogen diffuses to the SiO_2/Si interface and passivates dangling bonds, particularly P_b centers, by forming Si–H bonds. This reduces the number of electrically active interface traps, lowering the D_{IT}, and improving carrier mobility and device performance.

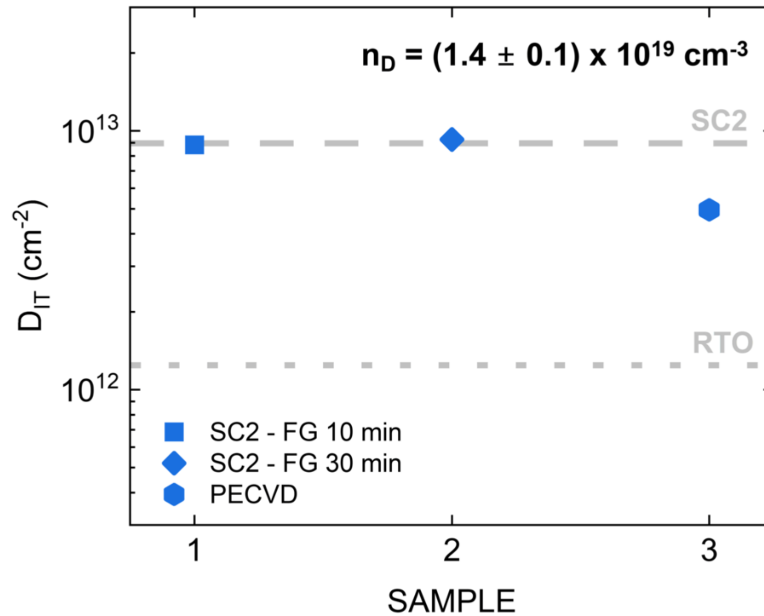


Figure 3.29: Interface state density (D_{IT}) extracted for SOI samples in the case of PECVD-SiO_2/Si interface compared to SC2-SiO_2/Si interface as deposited and after 10 and 30 min forming gas anneal. The value obtained for RTO-SiO_2/Si interface is also shown for reference.

To investigate the effectiveness of this treatment, two different SOI samples were doped following a single grafting-ashing cycle of PS-P polymers. After deposition of a 2 nm SC2 SiO_2 capping layer, the samples (1 and 2) underwent FG anneal at 400 °C for 10 min and 30 min, respectively. Another sample was prepared following the same doping procedure and SC2 capping. After removal of the 2 nm SC2 capping layer in 2% HF solution, the sample (3) was capped with a 10 nm SiO_2 layer deposited via Plasma-Enhanced Chemical Vapor Deposition (PECVD) at 350 °C. The deposition was performed following a standardized facility recipe to ensure a stable and reproducible dielectric environment. After photolithographic patterning and Al contact deposition, all samples were electrically characterized at room temperature to extract the carrier concentration n_e. The dopant concentration in the device layer was directly measured using ToF-SIMS depth profiling. All the samples showed and average $n_D = (1.4 \pm 0.1) \times 10^{19} cm^{-3}$ Following the same procedure presented in the previous section, combining the results of the electrical and compositional analysis enabled the extraction of the D_{IT}. Actually, D_{IT} values obtained provides information about the modification of the SiO_2/Si TOX interface, since it is assumed the only one changed during processing.

Figure 3.29 reports the measured D_{IT} values and compares them to the as-deposited SC2-SiO_2/Si interface without additional treatment and the as-grown RTO-SiO_2/Si interface. The data indicate that forming gas anneal is largely ineffective for SC2-grown oxide interfaces,

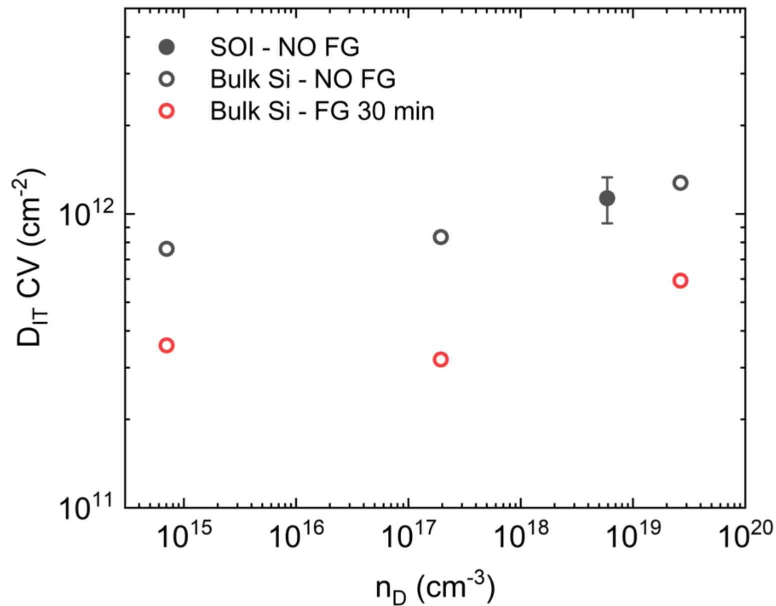


Figure 3.30: Interface state density (D_{IT}) obtained by CV measurements for RTO-SiO_2/Si interfaces in bulk Si versus P concentration (n_D) before (black open circles) and after a 30 min forming gas anneal (red open circles). Values are compared to the average D_{IT} extracted for SOI samples (black dot).

suggesting that the intrinsic poor structural quality of this oxide, high defect density and incomplete Si bonding cannot be significantly improved by hydrogen passivation. In contrast, the PECVD-SiO_2/Si interface showed a clear improvement in interface quality, consistent with reduced D_{IT} values and improved interface quality. However, the best results, with the lowest trap density, was achieved in samples treated with RTO.

The effect of FG anneal was investigated on RTO-SiO_2/Si interfaces grown on bulk Si substrates following the exact same procedure applied to the SOI samples. After removal of the native oxide, the samples were first chemically oxidized in SC2 solution, followed by RTO at 900 °C. In order to investigate the influence of n_D on the D_{IT}, the process was repeated on a set of P-doped Si substrates with n_D values around 10^{15}, 10^{17}, and 10^{19} cm^{-3}.

The extracted D_{IT} values, obtained from CV measurements, are shown in Figure 3.30. Experimental data indicate that for low doping levels ($n_D \leq 10^{17}$ cm^{-3}), the D_{IT} remains nearly constant, while at higher n_D the D_{IT} increase. This behavior, already suggested comparing the expected D_{IT} data for SC2-SiO_2/Si TOX interfaces, may be related to P-induced modifications of the interface chemistry, enhanced P segregation at the SiO_2/Si interface and dopant-induced interface states.

The results in Figure 3.30 are compared to those obtained from CV analysis on RTO-capped SOI samples. The D_{IT} values extracted from the SOI and bulk Si substrates show

excellent agreement, confirming that the oxidation process and interface formation are not significantly affected by the SOI substrate. This validates the reproducibility of the process and indicates that no additional interface degradation mechanisms are introduced by the presence of the buried oxide.

FG annealing was performed on all Si substrates for durations ranging from 5 to 30 min in 5 min increments. The data presented in Figure 3.30 also include the results for the 30 min anneal, which show a clear decrease in D_{IT} after FG passivation. Progressive hydrogen diffusion and effective passivation of dangling bonds and P_b centers is achieved over time.

Further improvements can be achieved even for ultrathin SOI samples through optimized FG anneal. However, changing the capping oxide already greatly enhanced interface quality, almost completely recovering the influence of interface traps at room temperature for the H_{SOI} values considered. For even thinner films and stronger 2D confinement, additional passivation strategies, such as FG anneal, may be required to minimize the contribution of non-passivated interface states.

3.6.3 Dielectric mismatch

The experimental data reported in Figure 3.27 indicate that at room temperature the doped SOI samples with RTO-TOX capping layer behave like bulk Si even for samples with Si device layer thickness well below 30 nm. Actually, the situation is a bit more complex as highlighted by sheet resistance and Hall measurements at low temperature.

Figure 3.31 illustrates the low temperature evolution from 5 to 300 K of R_s (top) and N_e (bottom) in the doped SOI films with RTO-TOX capping layer when H_{SOI} is progressively reduced from 29.0 nm to 20.3, 14.0 and 10.4 nm. At $H_{SOI} \sim 30$ nm the system behaves as a metallic material, in line with the expectation for bulk Si doped above the MIT. The average dopant concentration in the device layer is $(5.9 \pm 0.4) \times 10^{18}$ cm^{-3}. The carriers remain delocalized, and the conductivity shows only weak temperature dependence.

Upon reducing H_{SOI} to 20 nm, the metallicity begins to break down: a partial freeze-out of carriers is observed as temperature decreases below 25 K, suggesting that the effective donor ionization energy is already increasing in this regime. The trend becomes much more pronounced in the 14 and 10 nm thick films, where the conductivity is thermally activated and the carrier concentration essentially vanishes at low temperature, that is indicative of strong dopant freeze-out.

The data indicate a shift of the P threshold concentration corresponding to MIT in agreement with data reported by Tanaka *et al*. [121]. The average activation energy of the dopants for the samples with $H_{SOI} \sim 14.0$ and 10.4 nm extracted from the Arrhenius behavior of the conductivity is (51 ± 3) meV, a value significantly larger than the one expected in similarly doped bulk Si, pointing to a fundamental modification of the donor energy in ultrathin SOI layers. Especially considering the reduction of E_a which should be observed in bulk Si at high n_D [92].

In general, surface phenomena cannot be discounted as thickness approaches and

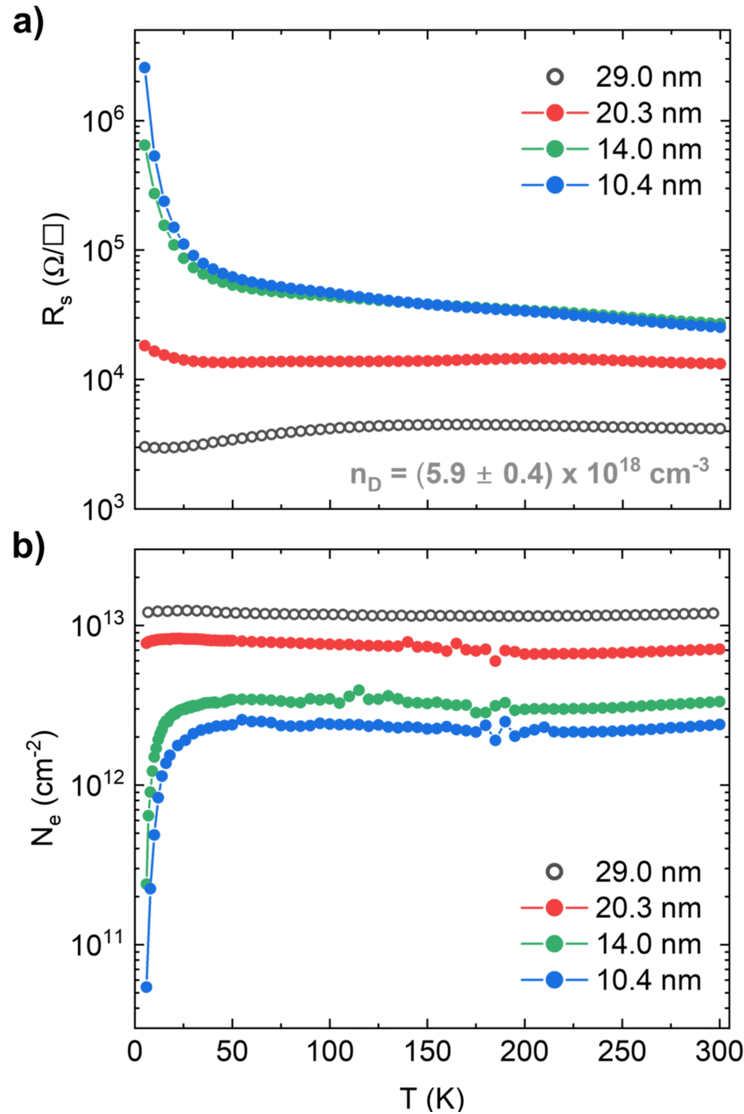


Figure 3.31: (a) low temperature sheet resistance R_s and total carrier dose N_e (b) obtained on SOI samples in Figure 3.27 with different H_{SOI} and $n_D = (5.9 \pm 0.4) \times 10^{18}$ cm^{-3}.

decreases below 10 nm. Many effects must be considered at these scales such as carrier surface scattering, dielectric screening [31], interface states [30], as well as decreased doping efficiency [25], increased dopant trapping [122], and an increase in Si bandgap [123].

It is important to note that such behavior cannot be explained solely by quantum confinement, since at $H_{SOI} \sim 10$ nm the Si device layer is still much thicker than the Bohr radius of donors (~ 2.5 nm) and the electronic states are not strongly quantized in the

conduction band. Instead, we assume that the dominant mechanism highlighted here is associated to the dielectric mismatch due to the surrounding SiO_2 [39]. The dielectric constant mismatch between Si ($\varepsilon_{Si} \approx 11.7$) and SiO_2 ($\varepsilon_{SiO2} \approx 3.9$) alters the Coulomb interaction of charged impurities: the lower dielectric constant of the oxide reduces the screening of the donor potential, thereby strengthening the Coulomb attraction and increasing the donor binding energy. This dielectric mismatch effect accounted for the strong increase of donor ionization energy that was reported in thin Si nanowires embedded in SiO_2 [30]. Data therefore provide direct experimental evidence of this dielectric confinement mechanism in ultrathin SOI.

Consequently, despite the dopant concentration being above the threshold for Mott transition in bulk materials, carriers in the 10.4 and 14.0 nm thick layers become localized at low temperatures because of the enhanced ionization energy. This explains the crossover from metallic behavior at 30 nm to semiconducting, activated behavior at 10.4 and 14.0 nm. The observed increase of activation energy with decreasing thickness reflects the progressive strengthening of dielectric mismatch as the Si channel becomes thinner, in agreement with theoretical expectations [30, 39].

These findings provide direct experimental evidence of this effect on 2D confined Si films, which have been explored only in 1D systems like Si NWs. Further work will be necessary to fully elucidate the complex interplay between these interface effects with device layer thickness and dopant concentration.

3.7 Kondo effect

The relentless miniaturization of semiconductor devices necessitates a fundamental understanding of quantum transport phenomena that become dominant at the nanoscale. Modern SOI technology, which utilizes ultrathin Si films, operates precisely in the regime where strong electron–electron and electron–impurity interactions dictate device performance at low temperatures. The study of quantum transport in low-dimensional semiconductor systems is a cornerstone of condensed matter physics, offering insights into many-body interactions and providing blueprints for future quantum devices.

A central phenomenon in this domain is the Kondo effect, which originates from the coherent scattering of conduction electrons off localized magnetic moments, resulting in a characteristic logarithmic increase in resistivity below a temperature-dependent minimum [124, 125, 126, 127]. The energy scale governing this phenomenon is the Kondo temperature (T_K), which dictates the size of the surrounding Kondo screening cloud. In Si, the localized magnetic moments are typically provided by strongly interacting dopant atoms such as phosphorus. This phenomenon has been well-established in heavily doped bulk silicon [128, 129] and has also been explored in highly confined one-dimensional (1D) silicon nanowires [124], where quantum confinement drastically alters the electronic structure and, consequently, the exchange coupling strength.

A major knowledge gap remains, however, in the 2D confined Si nanofilms. As the film thickness approaches the characteristic length scales of the dopant wavefunctions and the Kondo cloud, the system undergoes a dimensional crossover, which could fundamentally alter the density of states (DOS) at the Fermi level and, thus, the Kondo temperature [129, 125]. To date, there are no systematic reports investigating the magnetotransport signatures of the Kondo effect and the concurrent weak localization (WL) in P-doped ultra-thin Si films [130]. While the fundamental Kondo physics is well-documented in model systems, from dilute metallic alloys to artificial quantum dots and strongly confined 1D silicon nanowires [124], its presence and evolution in mass-produced, quasi-2D P-doped Si nanofilms have been largely overlooked. This constitutes a significant oversight, as the 2D geometry offers unprecedented electrostatic control, making it an ideal platform for engineering correlation effects.

Low-temperature transport in disordered metallic systems is governed by quantum interference effects, primarily WL and the Kondo effect [131]. These two mechanisms lead to competing magnetoresistance (MR) signatures: WL yields a positive magnetoconductance (negative MR), while the Kondo effect yields a negative magnetoconductance (positive MR), which is later suppressed by the magnetic field, leading to a low-field negative MR that competes with the WL signature.

At high doping concentrations of $n_D \sim (2-5) \times 10^{19}$ cm^{-3}, the impurity band is fully merged with the conduction band, resulting in a metallic state with delocalized electrons [92]. In this regime, localized magnetic moments can emerge due to incomplete screening and electron correlation effects [127]. Near the MIT, many-body interactions, disorder, and carrier localization play a crucial role in shaping the electronic and magnetic properties of

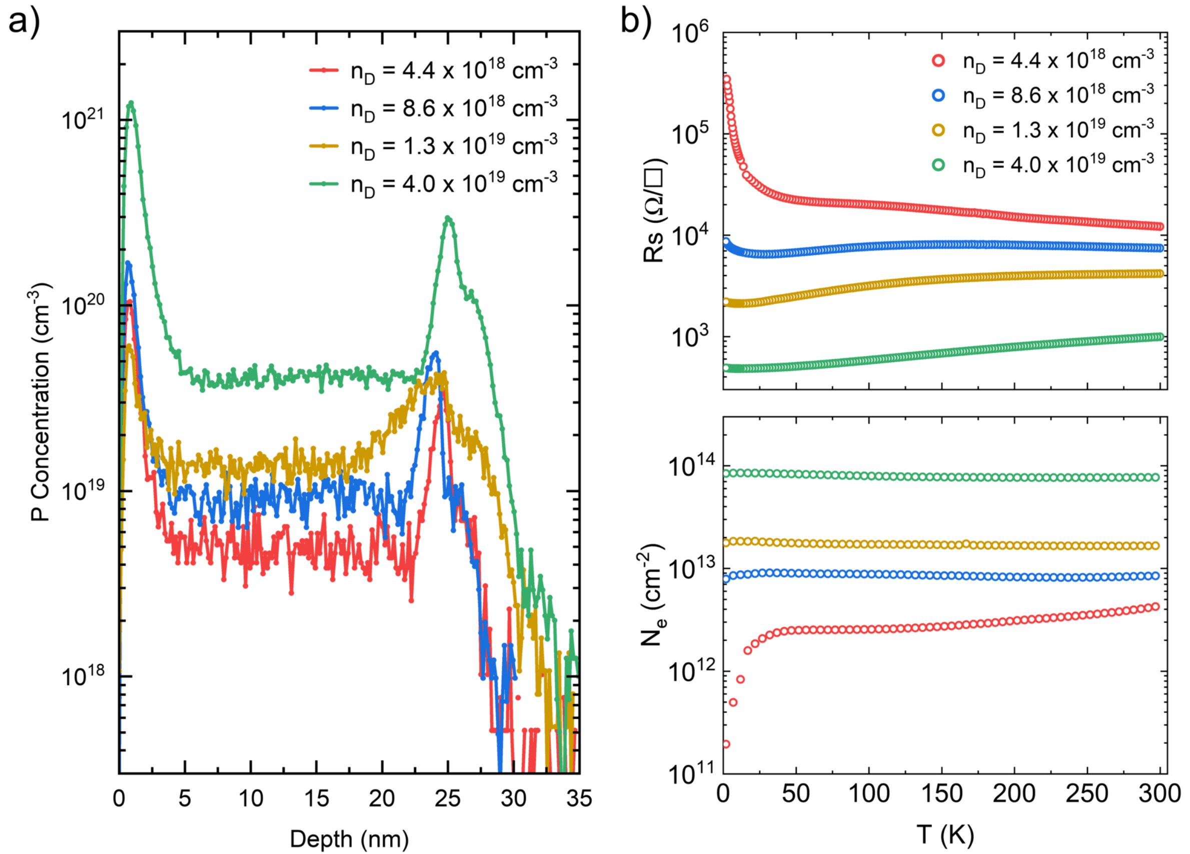


Figure 3.32: (a) ToF-SIMS P depth profiles of SOI samples with $H_{SOI} = 13 \pm 1$ nm doped following different sample preparation procedures. (b) Low-temperature sheet resistance R_s (top) and total carrier dose N_e (bottom) obtained on SOI samples with different $H_{SOI} = (23.5 \pm 0.6)$ and different n_D values.

Si:P. Investigating the magnetotransport and conduction properties of a system with free, delocalized electrons is particularly important to validate the classical metallic state while investigating the inherent disorder and quantum correction effects.

This investigation is of particular interest in 2D systems, where the confinement directly influences the DOS and amplifies interference and coupling. The presence of delocalized conduction electrons facilitates the observation of collective phenomena, including quantum coherence effects, as WL, and electron spin-exchange interactions [129, 132]. Demonstrating and controlling these quantum effects in highly doped Si films shows that complex quantum phenomena can be integrated into a mainstream semiconductor platform, providing a potential platform for spintronics, sensors, and quantum computing architectures.

1×1 cm^2 SOI dies with H_{SOI} ranging from 30 to 8 nm were doped using PS–P poly-

mers [60, 39]. Accurate control of the dose of dopants injected into the Si device layer was achieved as described in detail in section 3.2. This alternative doping approach ensures precise control over the effective number of atoms injected into the Si device layer and a homogeneous P concentration, as confirmed by calibrated ToF-SIMS P depth profiles reported in Figure 3.32a for SOI samples with $H_{SOI} = 23.5 \pm 0.6$ nm.

Varying the processing conditions, the P concentration n_D is accurately varied over one order of magnitude, from 4×10^{18} to 4×10^{19} cm^{-3}. At higher n_D, the apparent increase in the P signal at the device layer/BOX interface suggests P segregation and partial diffusion into the BOX [39].

The electrical properties of the doped SOI samples with $H_{SOI} = 23.5 \pm 0.6$ nm were accurately investigated through sheet resistance and Hall effect measurements in vdP configuration for temperatures ranging from 1.8 to 300 K. Figure 3.32b reports the evolution of R_s (top) and total carrier dose N_e (bottom) as a function of temperature for the SOI samples.

These P concentration values were expected to place all the samples above the transition from semiconductor to metal, since in bulk Si it is reported to occur at $n_D \sim 3 \times 10^{18}$ cm^{-3} [92, 96]. However, in the case of the sample with $n_D = 4.4 \times 10^{18}$ cm^{-3}, the typical temperature behavior of a resistive material is observed. The lowest doped sample is characterized by an increase of R_s when decreasing temperature, which perfectly correlates with the progressive decrease of N_e, suggesting a semiconductor-like behavior dominated by freeze-out at low temperatures [92].

This result indicates that, for ultrathin H_{SOI}, the critical concentration for the MIT is shifted to a higher n_D than in bulk Si. This upward shift is attributed to increased activation energy induced by the dielectric mismatch between the Si device layer and the surroundings. In all other samples, R_s decreases with T and is still measured even at $T = 1.8$ K, suggesting an overlap between the dopant and the conduction band and the absence of dopant freeze-out [92].

N_e remains constant in the entire temperature range, correlating with the reduction of R_s. When the temperature is reduced, the decrease in the number of phonons results in increased mobility and lower resistivity, characteristic of a electron Fermi gas [7, 96]. This results in the linear T dependence observed decreasing the temperature from 300 to 50 K. By reducing the temperature even further, a distinct crossover to the classic Fermi liquid is observed, where the dominant scattering mechanism shifts from electron–phonon to electron–electron interaction, resulting in a quadratic dependence $R_s \propto T^2$.

The magnetoresistance (MR) at low temperature ($T = 10$ K) serves as a direct indicator of 2D confinement within the Si device layer for the SOI samples with $H_{SOI} = 23.5 \pm 0.6$ nm. The data, presented in Figure 3.33a, reveal a clear crossover in transport mechanism dependent on n_D. Specifically, the lowest doped sample with $n_D = 4.0 \times 10^{18}$ cm^{-3} exhibits a positive MR, as expected from classical ordinary magnetoresistance. This positive MR arises from the Lorentz force, leading to a quadratic resistance increase described by the Drude model [114]:

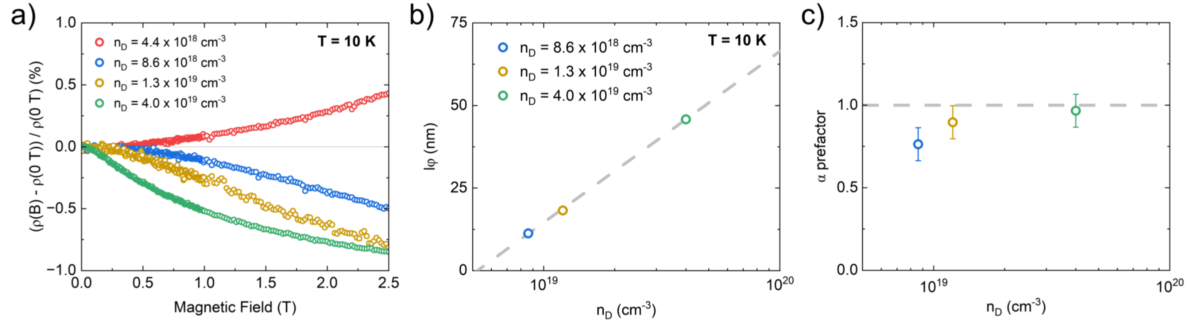


Figure 3.33: (a) Magnetoresistance of the SOI samples with $H_{SOI} = 23.5 \pm 0.6$ and different n_D values obtained ad T = 10 K. Coherence length l_Φ (b) and α prefactors (c) extracted from the HLN fitting function as eq. 3.10.

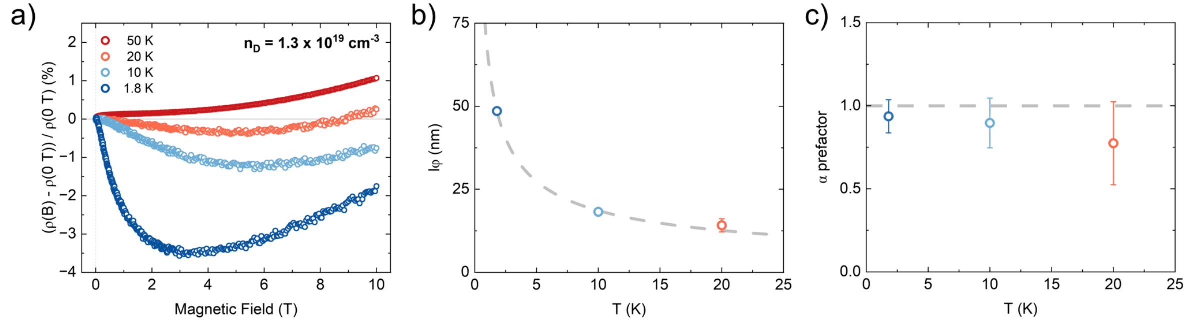


Figure 3.34: (a) Magnetoresistance as a function of temperature of the SOI sample with n_D = 1.3 x 10^{19} cm^{-3}. Coherence length l_Φ (b) and α prefactors (c) extracted from the HLN fitting function as eq. 3.10.

$$\frac{\Delta\rho}{\rho_0}(B) = \frac{\rho(B) - \rho_0}{\rho_0} = A(\mu_e B)^2 \tag{3.8}$$

Conversely, as n_D increases, MR transitions from positive to negative. This negative MR, and particularly the sharp cusp at low fields, is the signature of WL, a quantum interference effect dominant at low temperatures in disordered electronic systems [133]. To quantitatively analyze WL, it is convenient to consider the magnetoconductivity (MC), defined as the change in conductivity under an applied magnetic field

$$\Delta\sigma_\square = \sigma_\square(B) - \sigma_\square(0) = \frac{1}{R_s(B)} - \frac{1}{R_s(0)} \tag{3.9}$$

MC can be described using the Hikami–Larkin–Nagaoka (HLN) equation [133]:

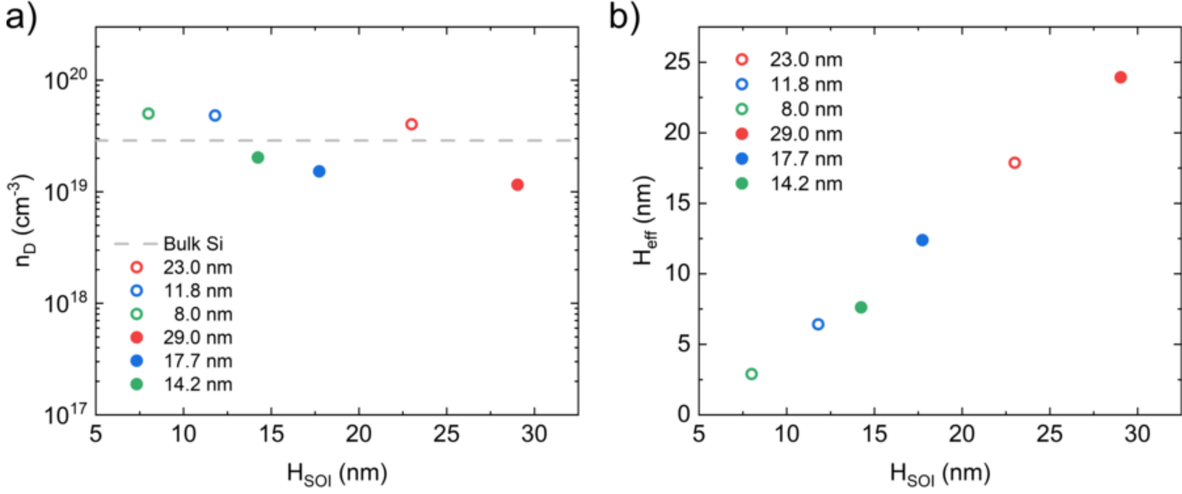


Figure 3.35: (a) Average P concentration n_D obtained by ToF-SIMS depth profiles as a function of H_{SOI}. (b) H_{eff} versus H_{SOI} calculated by eq. 3.7 for the same set of samples.

$$\Delta\sigma_{\square}(B) = -\alpha\frac{e^2}{\pi h}\left[\ln\left(\frac{h}{8\pi e l_\phi^2 B}\right) - \Psi\left(\frac{1}{2} + \frac{h}{8\pi e l_\phi^2 B}\right)\right] \tag{3.10}$$

where Ψ is the digamma function, l_ϕ is the phase coherence length, and α is the prefactor indicating dimensionality ($\alpha = 1$ for single 2D channel [134]).

A modified version of the HLN equation includes a parabolic background to account for classical and additional contributions to the MC that are not described by the quantum correction:

$$\Delta\sigma_{\square}(B) = -CB^2 - \alpha\frac{e^2}{\pi h}\left[\ln\left(\frac{h}{8\pi e l_\phi^2 B}\right) - \Psi\left(\frac{1}{2} + \frac{h}{8\pi e l_\phi^2 B}\right)\right] \tag{3.11}$$

Analysis of the HLN fits shows l_ϕ (Figure 3.33b) increases with n_D, indicating better screening and delocalization. The α prefactor (Figure 3.33(c)) approaches $+1$, confirming dominant 2D WL. Temperature-dependent MR in Figure 3.34a shows that WL diminishes with increasing temperature, consistent with $l_\phi \propto T^\beta$ and $\beta = -0.56 \pm 0.03$, close to the theoretical value $-1/2$ for 2D electron–electron scattering [132, 130].

Having confirmed the 2D nature of the charge transport at high doping concentration and ultrathin SOI, a new set of highly doped SOI samples with $H_{SOI} < 30$ nm was prepared, specifically targeting the metallic regime to investigate strong confinement and 2D transport. The average n_D measured via calibrated ToF-SIMS depth profiles is reported in Figure 3.35a as a function of H_{SOI}, confirming the control of the high n_D. The samples, compared to a P-doped bulk Si substrate with $n_D \sim 3 \times 10^{19}$ cm^{-3} (grey dashed line), which is used a

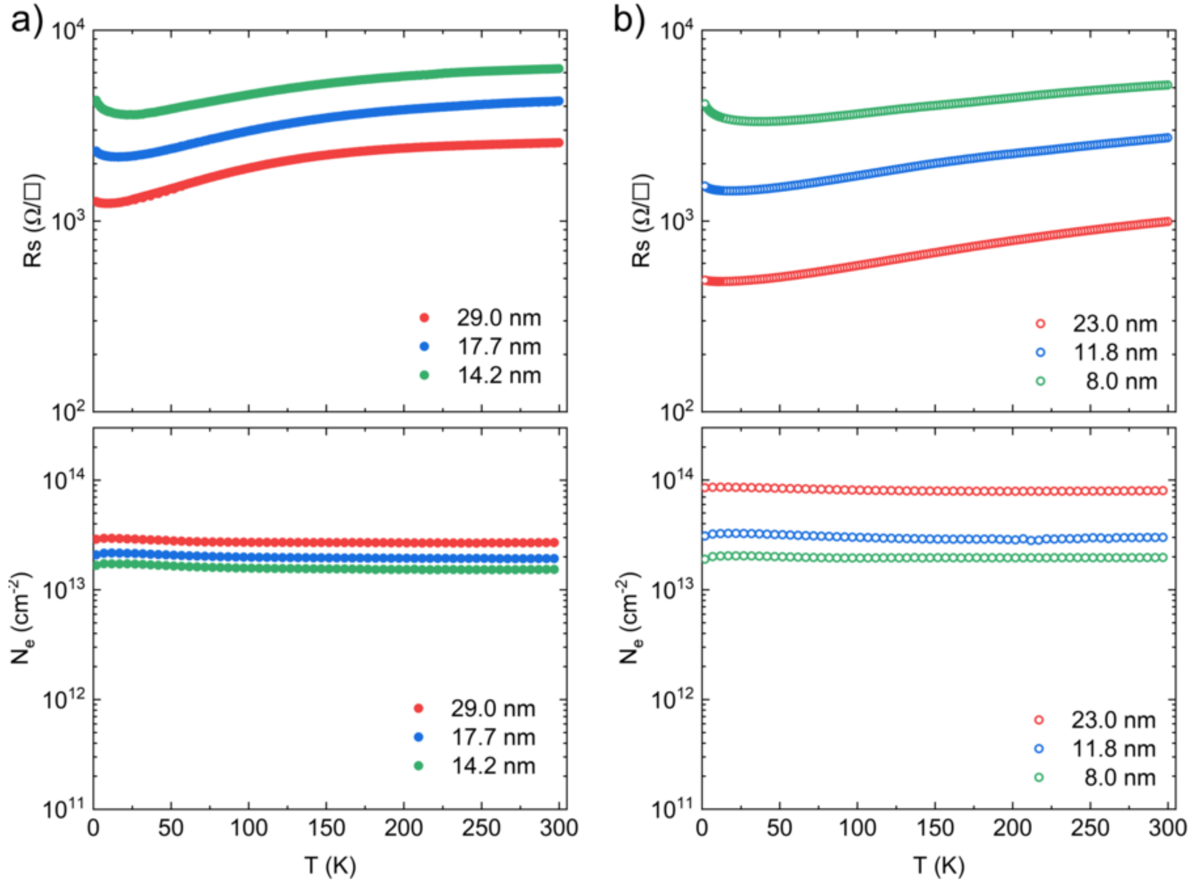


Figure 3.36: Low-temperature sheet resistance R_s (top) and total carrier dose N_e (bottom) obtained on SOI samples with $n_D = (1.6 \pm 0.4) \times 10^{19}$ cm^{-3} (a) and $n_D = (4.6 \pm 0.5) \times 10^{19}$ cm^{-3} (b) for different H_{SOI}.

reference fall into two distinct sets: a low dose with $n_D = (1.6 \pm 0.4) \times 10^{19}$ cm^{-3} and a high dose with $n_D = (4.6 \pm 0.5) \times 10^{19}$ cm^{-3}.

The electrical properties at room temperature were used to estimate the effective H_{eff} of the conductive channel, following the procedure described in Section 3.6, which accounts for carrier depletion at non-passivated interface states present at the SC2-SiO_2/Si capping layer interface. The calculated H_{eff} values, reported in Figure 3.35b, show a clear linear reduction as H_{SOI} decreases, consistent with samples having similar n_D and D_{IT} values. Once H_{eff} is determined, the resistivity ρ in the conductive film of reduced dimensionality can be computed from the measured sheet resistance R_s as $\rho = R_s H_{eff}$.

Figure 3.36a reports the low-temperature evolution of R_s (top) and N_e (bottom) from 1.8 to 300 K for samples in the low-dose set with $n_D = (1.6 \pm 0.4) \times 10^{19}$ cm^{-3}. At T = 300 K, R_s increases and N_e decreases with reduction of H_{SOI}, as expected for constant nominal n_D. N_e

remains constant across the entire temperature range, confirming these films are metallic with full overlap between dopant and conduction bands.

The decrease in R_s with decreasing temperature reflects enhanced carrier mobility due to reduced electron–phonon scattering, consistent with prior results. Interestingly, a clear upturn in R_s is observed when $T < 25$ K, becoming more pronounced as H_{SOI} decreases to 14.2 nm. This low-temperature upturn is examined in subsequent paragraphs.

Figure 3.36b report the low-temperature evolution of R_s and N_e for the high-dose set ($n_D = (4.6 \pm 0.5) \times 10^{19}$ cm^{-3}). Consistent with Figure 3.36a, N_e remains constant across temperature, while R_s decreases with decreasing T. The evolution of R_s shows for $T < 50$ K, a transition from $R_s \propto T$, suggesting a electron–phonon dominated scattering mechanism, to $R_s \propto T^2$ Fermi liquid regime, electron–electron scattering dominated. A clear resistivity upturn is observed for $T < 25$ K, particularly for the thinnest sample ($H_{SOI} = 8.0$ nm).

This upturn may arise from electron–electron interactions, weak localization, or exchange-induced electron transport. In heavily doped bulk Si:P, a transition from Fermi liquid to a Kondo-singlet-like state occurs near $T_K \sim 1$ K, forming a correlated Kondo lattice [128]. The Kondo effect, arising from localized magnetic impurities interacting with conduction electrons, leads below T_K to a resistivity minimum followed by a logarithmic upturn, saturating for $T \ll T_K$. Such behavior has been reported in bulk Si and Si nanowires [128, 124, 129]. Confinement enhances the density of states at the Fermi level, potentially increasing T_K.

Figure 3.37a reports the MR measured at $T = 1.8$ K for magnetic fields up to 10 T for samples in the low-dose set with $n_D = (1.6 \pm 0.4) \times 10^{19}$ cm^{-3}. All samples show negative MR, with a sharp WL-related cusp at low fields. The parabolic background term (classical contribution) decreases with reduced H_{SOI}, consistent with lower μ_e, resulting in reduced C parameter in Eq. 3.11. Magnetoconductivity $\Delta\sigma$ was fitted using Eq. 3.10. The parameters extracted from the HLN fit are reported in Figure 3.37, with error bars that are shown or smaller than the symbol size. The α-prefactor (Figure 3.37b) remains close to $+1$, confirming predominant 2D transport. No significant trend in α is observed across the samples within fitting uncertainty. Clear decrease of l_ϕ (Figure 3.37c) is observed when reducing H_{SOI}, with error bars from the HLN fit smaller than the symbol size. This reduction is consistent with enhanced carrier scattering at SiO_2/Si interfaces, reducing quantum coherence.

Figure 3.38a shows MR evolution with magnetic field at 1.8 K for for samples in the high-dose set with $n_D = (4.6 \pm 0.5) \times 10^{19}$ cm^{-3}, both displaying negative MR, consistent with WL. HLN parameters from Eq. 3.10 are shown in Figures 3.38b and 3.38c. Higher n_D yields longer l_ϕ, consistent with stronger screening. l_ϕ decreases with H_{SOI}, more significantly than in the low-dose set. The α prefactor remains $\sim +1$ for $H_{SOI} = 11.8$ nm but decreases substantially at 8.0 nm, suggesting additional scattering mechanisms, as roughness, electron–electron interaction, and exchange interactions. This enhanced scattering correlates with reduced WL contribution, shorter l_ϕ, and the observed resistivity upturn for $T < 25$ K.

The Kondo contribution increase to the resistivity is commonly modeled at $T < 100$ K by an empirical function combining residual resistivity ρ_0, a Fermi liquid T^2 term, and the Kondo scattering term [135]:

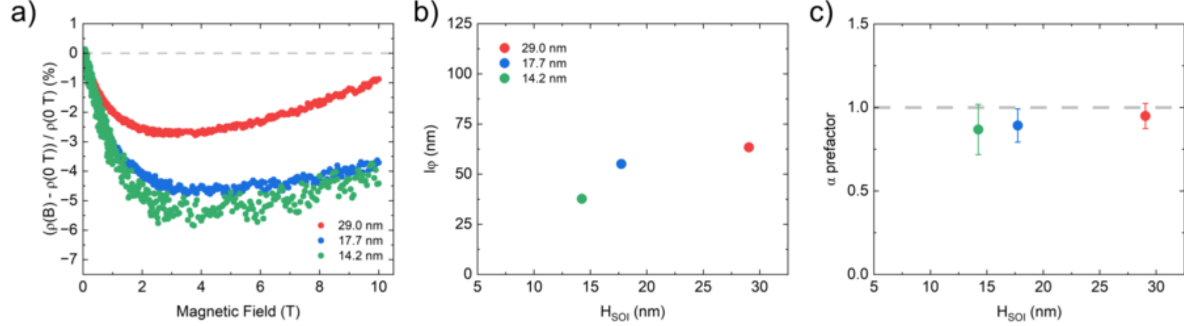


Figure 3.37: (a) Magnetoresistance of the SOI samples with with $n_D = (1.6 \pm 0.4) \times 10^{19}$ cm^{-3} obtained ad T = 1.8 K. Coherence length l_Φ (b) and α prefactors (c) extracted from the HLN fitting function as eq. 3.10.

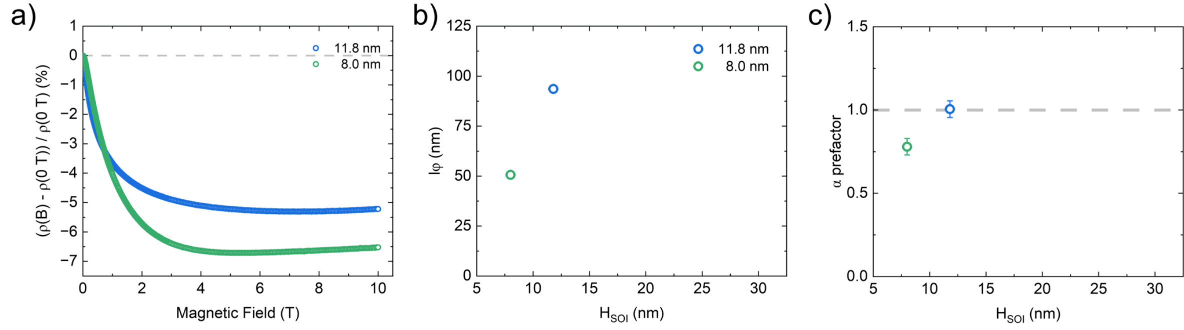


Figure 3.38: (a) Magnetoresistance of the SOI samples with with $n_D = (4.6 \pm 0.5) \times 10^{19}$ cm^{-3} obtained ad T = 1.8 K. Coherence length l_Φ (b) and α prefactors (c) extracted from the HLN fitting function as eq. 3.10.

$$\rho = \rho_0 + AT^2 + \rho_{K,0} \left(\frac{1}{1 + (2^{1/s} - 1)(T/T_K)^2} \right)^s \tag{3.12}$$

where T_K in the Kondo temperature,$\rho_{K,0}$ the residual resistivity at T = 0 K due to Kondo scattering, and s an empirical fitting parameter, typically fixed at 0.225. Data from both sample sets were fitted using Eq. 3.12. Figures 3.39 show normalized resistivity $\rho(T)/\rho_0$ for the low (a) and high-dose (b) set. The normalization enables the direct comparison across the samples, enhancing the upturn observes at low temperature. Figure 3.39b also shows the results of the bulk Si reference ($n_D = 3 \times 10^{19}$ cm^{-3}), showing only the T^2 Fermi liquid dependence without any upturn in the measured range. However, prior work in the literature observed such upturn for a similarly doped bulk Si sample at lower temperatures ($\sim$ 1 K) [128]. Therefore, an increase of the measured ρ is to be expected even in the bulk sample below the measurement range.

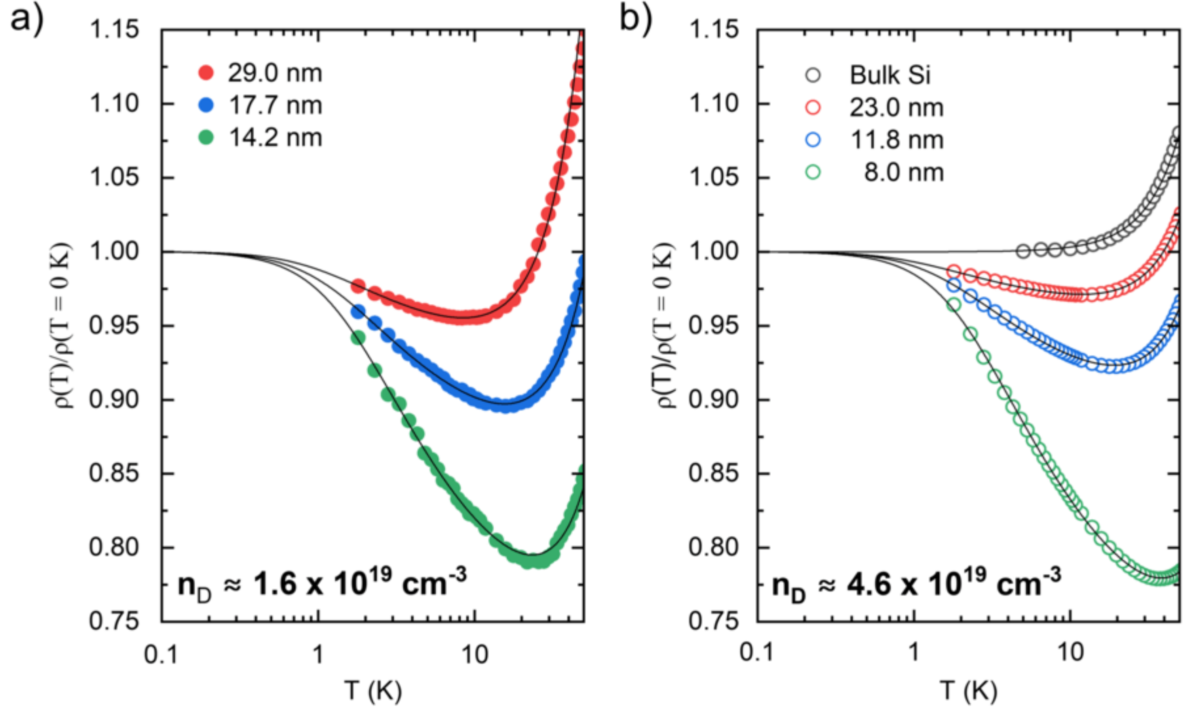


Figure 3.39: Low-temperature normalized resistivity for SOI samples with $n_D = (1.6 \pm 0.4) \times 10^{19}$ cm^{-3} (a) and with $n_D = (4.6 \pm 0.5) \times 10^{19}$ cm^{-3} (b).

A hallmark of Kondo scattering is that normalized Kondo contribution to the resistivity:

$$\rho_K/\rho_{K,0} = \frac{\rho - \rho_0 - AT^2}{\rho_{K,0}} \tag{3.13}$$

follows a universal curve when plotted versus T/T_K, as the Kondo effect depends on a single energy scale $k_B T_K$ [136]. Figures 3.40a and 3.40b show this collapse for all samples from both doping sets, matching the theoretical universal Kondo curve, validating the hypothesis that the resistivity upturn originates from Kondo scattering.

The extracted T_K parameters for all SOI samples are plotted in Figure 3.41 versus H_{SOI}. The two thickest samples show larger uncertainty since their low-temperature Kondo upturn is only just visible. Interestingly, data follow a consistent trend independent of n_D, suggesting that above the MIT, T_K is dominated by geometric 2D confinement rather than impurity density. Data in Figure 3.41 are fitted with a power law:

$$T_K = T_{K,0} + A\, H_{SOI}^{\beta} \tag{3.14}$$

with a fixed offset $T_{K,0} = 1$ K, corresponding to the value in bulk Si. The experimental fit to the data results in a scaling exponent $\beta = -0.85$.

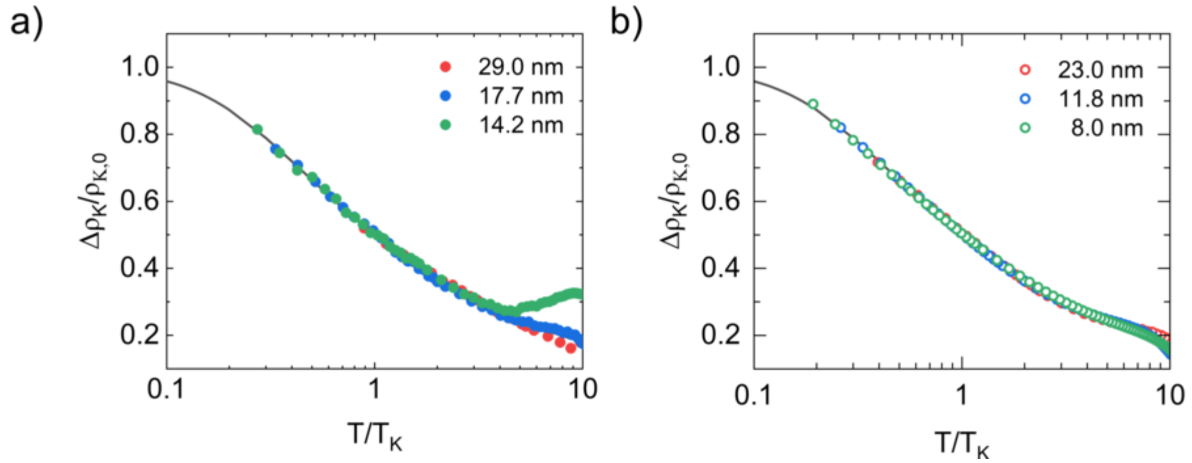


Figure 3.40: Normalized Kondo resistivity plotted as a function of T/T_K for SOI samples with $n_D = (1.6 \pm 0.4) \times 10^{19}$ cm^{-3} (a) and with $n_D = (4.6 \pm 0.5) \times 10^{19}$ cm^{-3} (b).

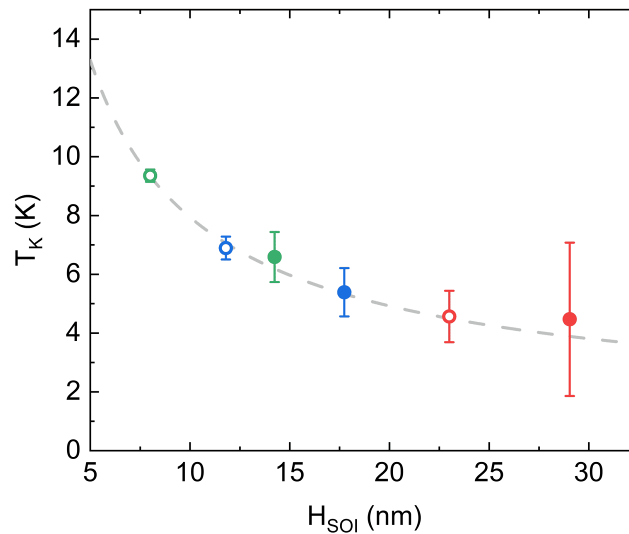


Figure 3.41: Kondo temperature T_K extracted from Eq. 3.12 for SOI samples as a function of H_{SOI}. Experimental data are fitted as Eq. 3.14.

The observation of 2D Kondo scattering mechanisms in a technologically mature material such as Si provides an accessible platform for exploring the interplay of confinement, disorder, and electron interactions. The ability to control and modulate the quantum Kondo temperature via 2D confinement is highly interesting for practical applications. Integrating the Kondo effect into Si-based devices enables spin-dependent scattering control, offering potential pathways toward spintronics, sensing, and quantum information processing.

3.8 Topology transfer on SOI

The discovery and isolation of graphene signed a fundamental turning point for the research of 2D materials [137]. The hexagonal topology with sp^2 covalent bonding results in extraordinary chemical-physical properties, including mechanical strength and flexibility, as well as outstanding thermal and electrical conductivity. Additionally, the electronic properties can be tuned through doping or external fields [138]. The electronic characteristics of graphene arise primarily from its honeycomb topology, which generates a band structure where the conduction and valence bands meet at discrete points. In the vicinity of these points, the energy dispersion is linear, forming *Dirac cones*, where electrons behave as massless Dirac fermions, exhibiting extremely high mobility and nearly ballistic transport even at room temperature [139]. These properties motivated extensive research into graphene for electronics, optoelectronics, energy storage, and biomedical applications.

Despite these advantages, the lattice structure of graphene is fixed, making it difficult to modify its band structure and lattice constant. Importantly, the exceptional properties of graphene arise largely from its topological symmetry. This insight has motivated researchers to explore whether Dirac-like electronic dispersion can be reproduced in other systems by imposing similar honeycomb periodicity. In particular, artificial graphene (AG) systems of 2D electron gas (2DEG) patterned with a honeycomb potential have demonstrated that Dirac cones can emerge purely from lattice topology, allowing unprecedented control over the electronic band structure [140, 141].

Implementing this concept in doped ultrathin Si nanofilms offers a pathway to merge the exceptional transport characteristics of graphene-like materials with the scalability and CMOS compatibility of the Si platform. By etching a honeycomb lattice onto a 2D Si film, it becomes possible to impose a periodic boundary condition that structurally mimics the sp^2 covalent bonding of graphene [142]. If this honeycomb topology induces Dirac-like states, charge carriers experience a lower effective mass and reduced scattering, leading to enhanced mobility. Moreover, the resulting bandgap and effective mass become tunable through the dimensions and periodicity of the transferred topology. Achieving Dirac-like states in Si requires a periodic honeycomb modulation with a lattice constant smaller than the electron coherence length ($a_L < l_\Phi$), ensuring coherent coupling and the formation of Dirac-like bands. Heavy doping enhances band-like conduction and increases l_Φ, while low H_{SOI} ensures strong 2D confinement.

Recent advances in nanofabrication, particularly block copolymer (BCP) lithography, provide a practical route to realize these structures [76, 77]. BCP self-assembly generates highly ordered hexagonal patterns with characteristic feature sizes ~ 10 nm, directly supplying the periodicity needed to impose a honeycomb potential. These patterns can be transferred into doped Si films using RIE, precisely defining lattice constant and pore diameter. Optimized etching conditions ensure highly anisotropic profiles with vertical, narrow sidewalls, which are crucial for preserving the intended geometry, maximizing quantum confinement in the small neck, and facilitating the emergence of Dirac-like electronic dispersion. The combined

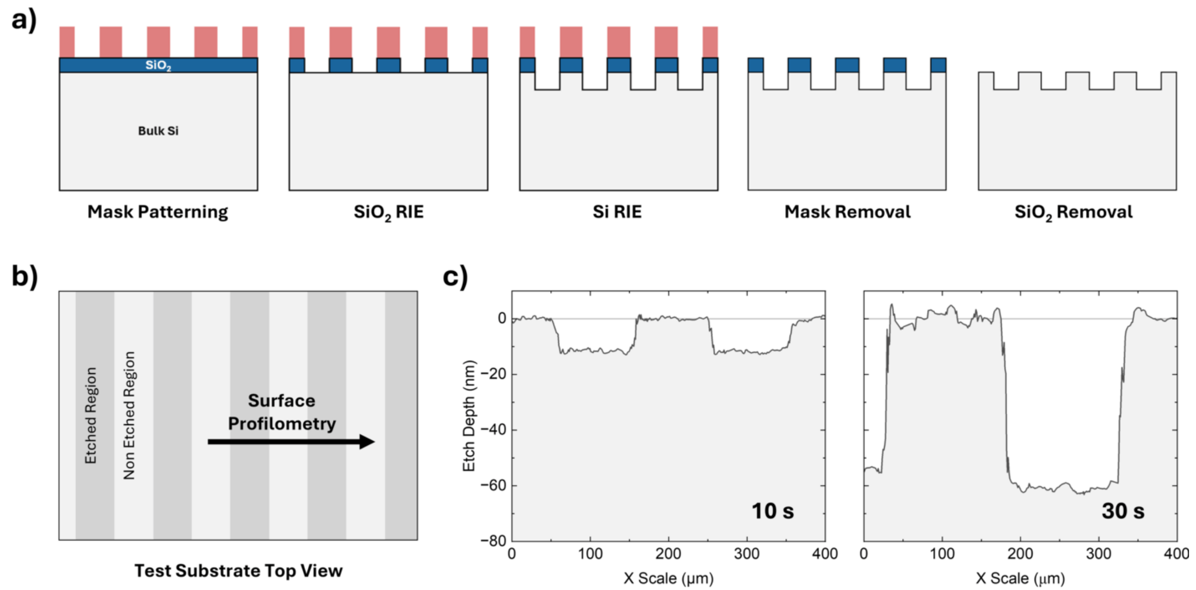


Figure 3.42: (a) Schematic representation of the two-step RIE process. (b) Top-view schematic of the test substrate illustrating the alternating etched and non-etched pattern and the direction of the surface profilometry measurement. (c) Profilometry analysis showing the etched depth for the Si substrate after removal of the SiO_2 hard mask in the case of a 10 s etch (left) and 30 s etch (right).

control of heavy doping, precise nanoscale pattern transfer, and 2D confinement could provides a viable route to engineer Dirac-like electronic states within the fully CMOS-compatible Si platform.

Initial process calibration for RIE was performed on bulk Si wafers capped with a 10 nm thick SiO_2 hard mask and a 1 μm thick resist patterned with standard photolithography. The etching protocol involved two sequential RIE steps (Figure 3.42a) to produce alternating micrometric stripes of etched and non-etched Si, as shown in the top-view schematic (Figure 3.42b).

The first RIE used an Ar + CHF_3 gas chemistry for 2 min to anisotropically open the SiO_2 hard mask, which was then used for the subsequent Si etching step. The second, and more critical, step involved patterning the underlying Si substrate via a Pseudo-Bosch RIE process. Unlike the traditional alternating-cycle Bosch process, the Pseudo-Bosch method achieves anisotropic etching using a single CHF_3 + C_4F_8 + SF_6 gas mix. The polymerizing gases (CHF_3 and C_4F_8) continuously deposit a sidewall passivation layer, while the etchant (SF_6) preferentially attacks the trench floor, maintaining vertical sidewalls without alternating cycles. The duration of this second step was varied to calibrate the etch rate. Profilometer analysis was performed on samples etched for 10 and 30 s (Figure 3.42c) before and after removal of the SiO_2 hard mask. The analysis confirmed accurate Si etching and survival

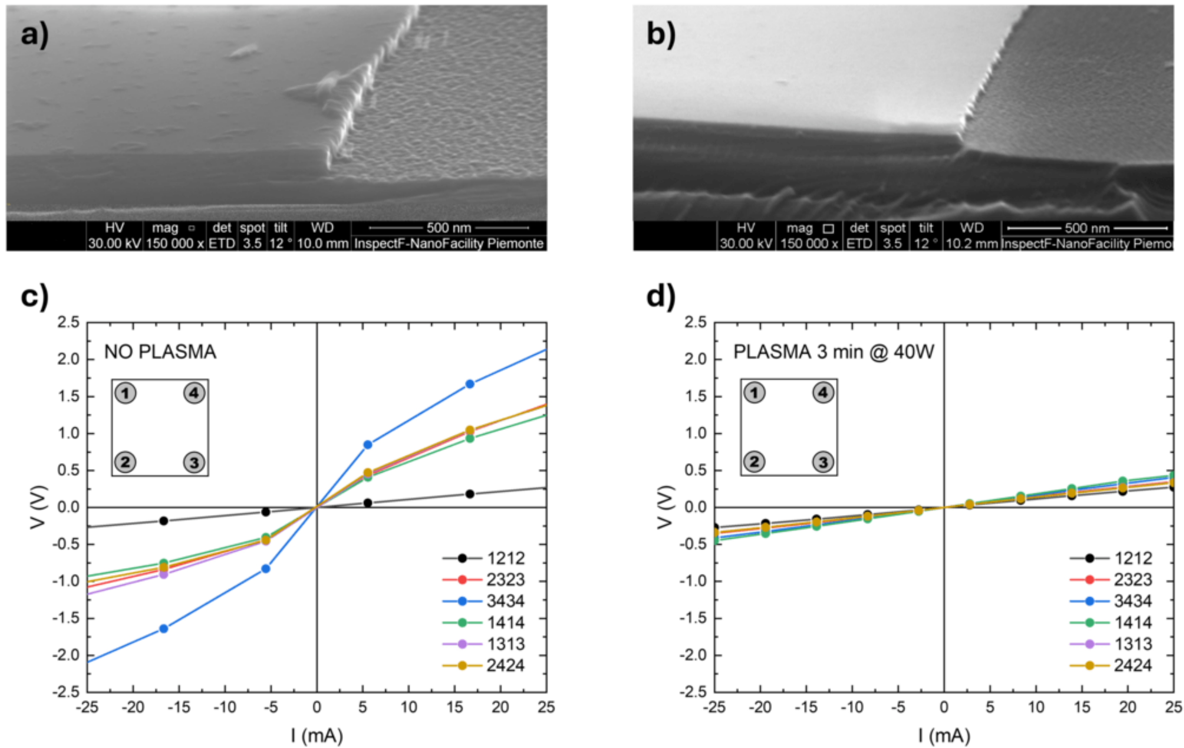


Figure 3.43: Comparison of etched surface quality before (a) and after (b) introducing a 3 min O_2 plasma cleaning step at 40 W, demonstrating significant improvement in edge and surface cleanliness. IV curves of Al electrical contacts deposited in the openings without (c) and with (d) the O_2 plasma cleaning treatment demonstrating significant improved quality and linearity.

of the mask after RIE. An etch depth of around 10 nm was achieved after 10 s, while 30 s resulted in an etch depth of 60 nm. The apparent non-linear etching rate is attributed to transient plasma conditions during ignition and stabilization of the RIE process, which strongly affect short etch steps before reaching the steady-state regime. Figure 3.42c suggests that an etch duration of 30 s is sufficient to fully etch the 30 nm thick device layer down to the BOX.

A 3 min O_2 plasma treatment at 40 W was introduced after resist opening and development to improve the quality of the RIE process. Accurate cleaning of the surface before RIE resulted in much cleaner surfaces and edges, as shown in SEM images (Figure 3.43a,b). As a result, Al contacts deposited in the openings after HF dip showed significantly improved electrical quality, with perfectly linear current-voltage (IV) characteristics and reduced voltage necessary for the same current (Figure 3.43c,d).

To reach nanometric dimensions required for quantum effects, where lateral dimensions

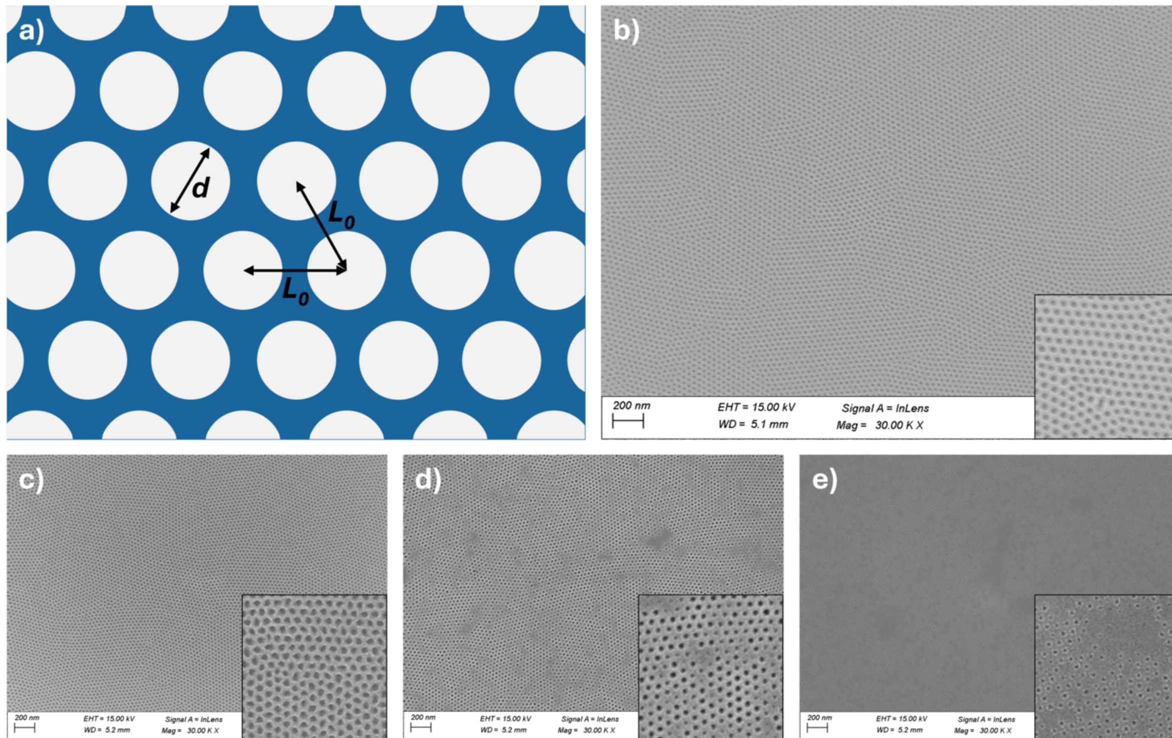


Figure 3.44: (a) Schematic representation of the cylindrical BCP template (blue) after opening of the pores, with characteristic dimensions (d and L_0) indicated. Planar SEM image of the cylindrical PS-b-PMMA BCP mask before (b) and after (c) the two subsequent RIE processes. (d) Pattern transfer to the SiO_2 hard mask after removal of the BCP mask. (e) Pattern transfer to the Si device layer after removal of the SiO_2 hard mask.

must match the electron l_Φ and the dopant wave function, BCP lithography was employed. In this work, a PS−b−PMMA BCP mask was employed to produce a cylindrical pattern suitable for the honeycomb lattice geometry, with feature sizes ∼ 30 nm (Figure 3.42a).

A 50 nm thick cylindrical PS−b−PMMA mask was deposited on a 10 nm thick SiO_2 hard mask, which itself sat atop a 20 nm thick SOI device layer doped with one PS−P doping cycle. The RIE processing sequence aligns with that used for micrometric stripes (Figure 3.42a) but scaled down to tens of nanometers. SEM images were acquired after each step (Figure 3.44): planar BCP mask after pore opening (Figure 3.44b), mask after two RIE steps (Figure 3.44c), underlying SiO_2 hard mask after BCP removal (Figure 3.44d), and bare Si device layer after removal of SiO_2 hard mask (Figure 3.44e). Non-uniformity in pattern transfer was observed, especially considering accurate transfer to the SiO_2 hard mask.

After SiO_2 hard mask removal, a 2 nm SC2 SiO_2 capping layer was grown on the Si device layer. Mesa patterning and Al deposition followed the same procedures as flat SOI samples. SEM images inside different devices (Figure 3.45) show non-uniformity and incorrect pattern

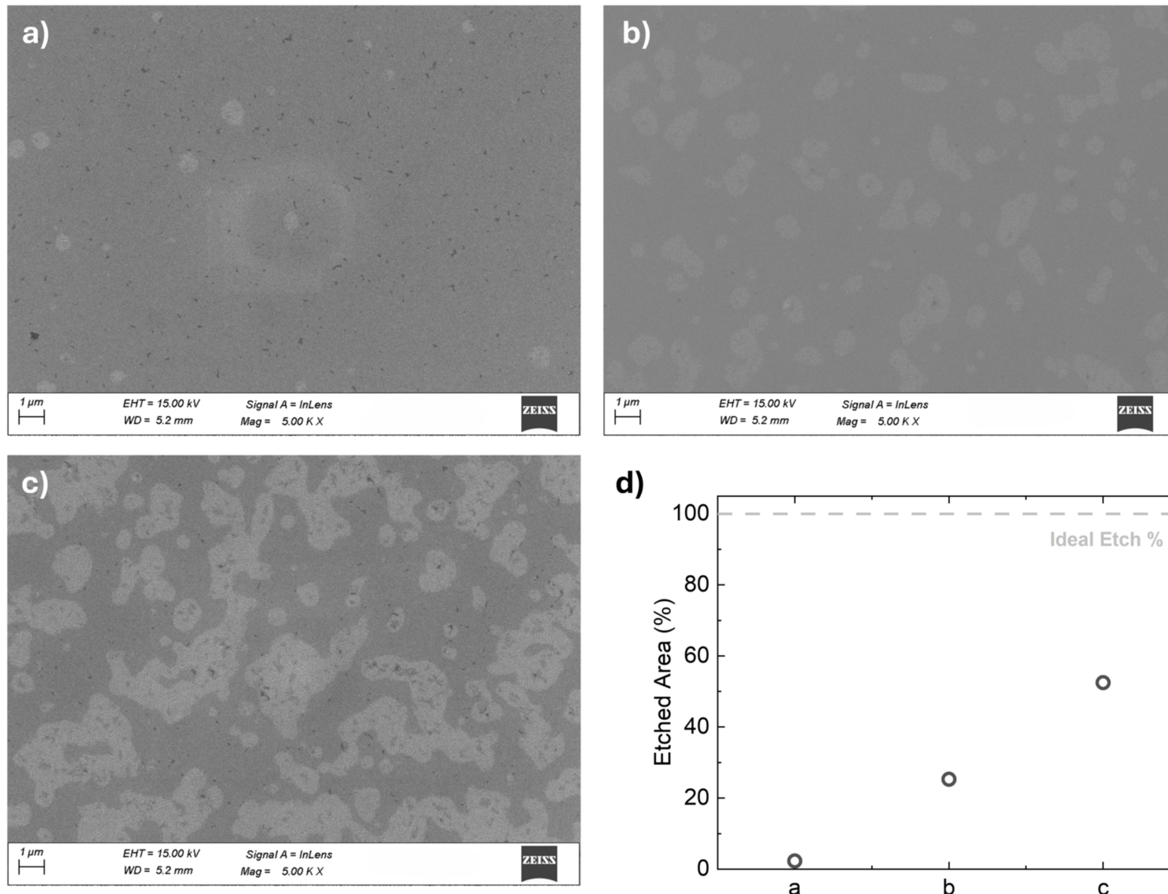


Figure 3.45: SEM images (a, b, c) of three patterned regions, illustrating the process non-uniformity. (d) Etched Area Fraction for the three regions: low (a), medium (b), and high (c).

transfer. Analysis with ImageJ quantified the etched area (Figure 3.45d), ranging from almost zero to 50 %. This data was used in an Effective Medium Approximation (EMA) model to fit spectroscopic ellipsometry (SE) data, using a two-layer model: patterned layer (void-to-Si ratio) and underlying flat Si. Only ~ 6 nm of Si was etched with the BCP mask, confirming that reduced pore size significantly slowed the etching rate.

Three devices were electrically analyzed at low temperature, labeled LOW (low area, almost flat), MED (medium etched), and HIGH (high area, ~ 50 % etched). Figure 3.46a shows sheet resistance R_s and Hall carrier dose N_e from 5 to 300 K, indicating metallic conduction. N_e is consistent across samples, and R_s decreases with temperature due to reduced phonon scattering. Normalized R_s (Figure 3.46b) shows identical evolution for LOW and MED, but differences in HIGH. Mobility evolution (Figure 3.46c) shows reduction with increasing etched area, as expected due to enhanced interface and roughness scattering.

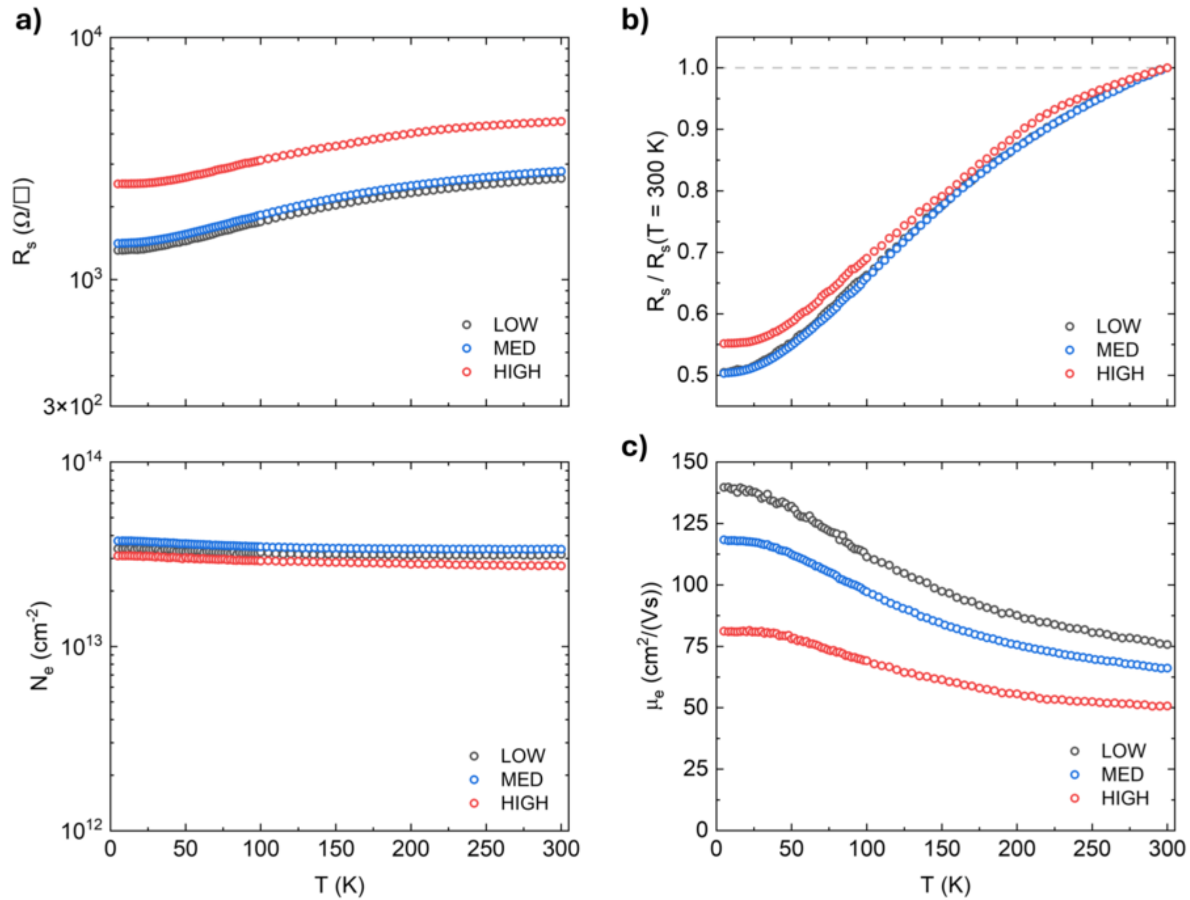


Figure 3.46: (a) Low temperature sheet resistance (R_s, top) and Hall carrier dose (N_e, bottom) evolution for the LOW, MED, and HIGH devices measured across a temperature range from 5 to 300 K. (b) Normalized sheet resistance vs temperature. (c) Low temperature carrier mobility (μ_e) evolution for the same set of samples.

Even with only 6 nm etched, conduction was maintained, and differences compared to flat substrate were observed.

Pattern transfer issues were traced to non-uniform opening of the BCP mask. The SiO_2 etching is highly anisotropic, so RIE duration could be increased, but the O_2 plasma step for opening the 8 nm random copolymer is critical: it must fully open the copolymer down to the SiO_2 surface without degrading the BCP mask. Insufficient duration resulted in high non-uniformity during polymeric mask transfer to the Si device layer.

Over-etching tests showed that almost correct patterning can be achieved down to the SiO_2 BOX by controlling processing parameters. Figure 3.47 shows SEM images for proper etching (Figures 3.47a,b) and over-etching (Figures 3.47c,d), where small Si necks are

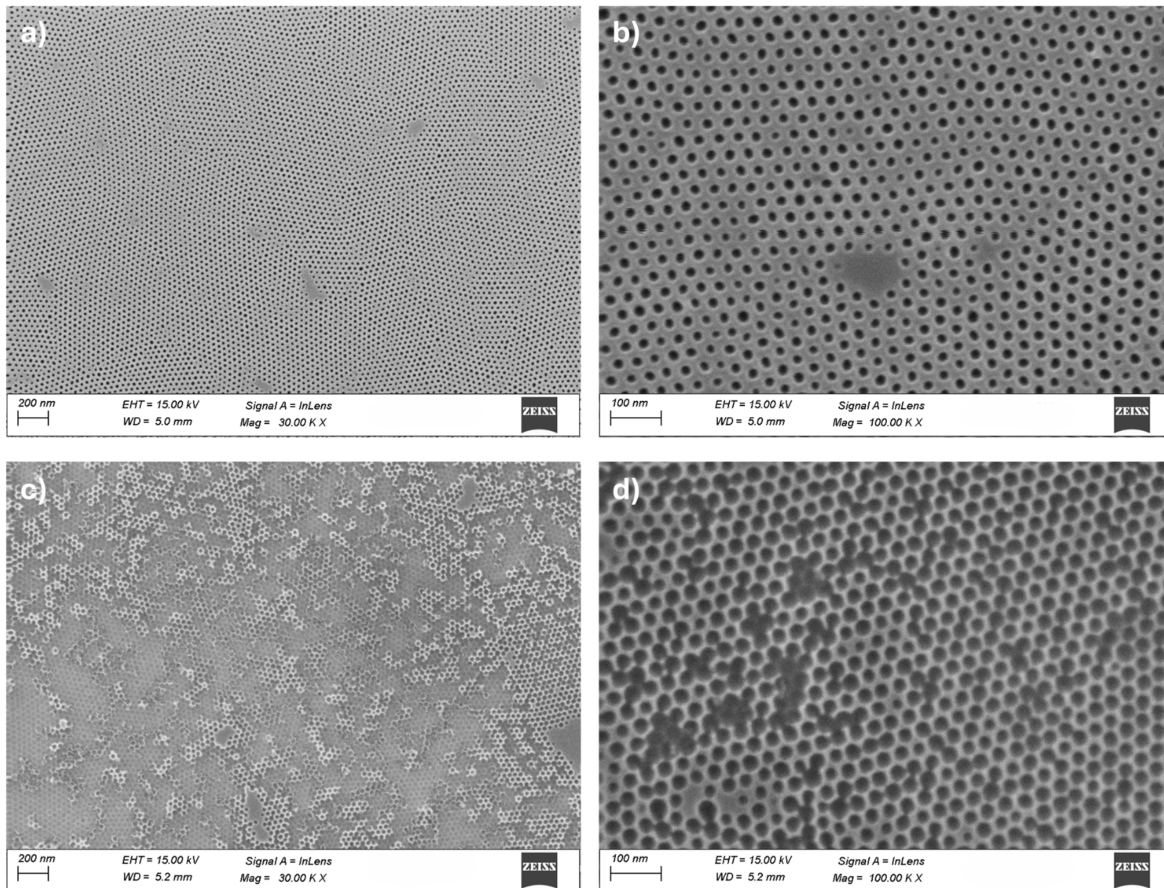


Figure 3.47: SEM images (a at low mag, b at high mag) showing successful, anisotropic pattern transfer to the Si device layer after process optimization. SEM images (c at low mag, d at high mag) illustrating the effect of over-etching, where isotropic etching severely reduces the thickness of the Si necks, leading to structural destruction and island formation.

destroyed. Tilted SEM microscopy (Figure 3.48a,b) confirms pattern transfer through the Si device layer and 10 nm SiO_2 mask.

Using refined parameters, a second generation of samples was prepared, parallel to flat control sets, patterned across various thicknesses (8 to 12 and 24 nm) and doping cycles (1, 5, 10). They are ready for final electrical characterization. The O_2 plasma step remains critical to fully open the random copolymer without degrading the BCP mask.

Since the etching rate was greatly reduced for the nanometric features, another test sample was patterned for a longer RIE duration to investigate the effect of over-etching on the Si device layer and to assess the anisotropy of the Pseudo-Bosch RIE process. It was discovered that accurate and correct patterning down to the SiO_2 BOX layer can be achieved

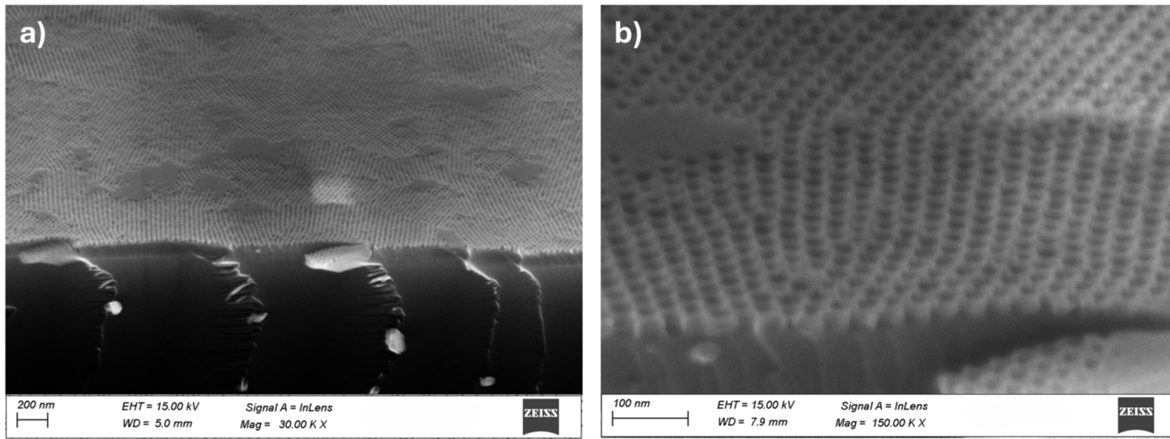


Figure 3.48: Tilted SEM images (a and b) confirming highly anisotropic etching and accurate pattern transfer through the 10 nm SiO_2 hard mask and the entire Si device layer down to the BOX layer.

by careful control of the processing parameters.

Figure 3.47 shows the effect of over-etching on the device layer. Figures 3.47a and 3.47b present SEM images at 30× and 100×, respectively, for well-etched areas with correct pattern transfer. Figures 3.47c and 3.47d show SEM images at the same magnifications in regions affected by over-etching. In these areas, the isotropic component of the Si etch reduces the thickness of the small Si necks in the honeycomb pattern until they are completely destroyed and disconnected. As observed in Figure 3.45c, some areas are more severely affected, leaving only isolated islands after the RIE step and removal of the SiO_2 mask via BOE.

Well-etched areas were further investigated using tilted SEM imaging. Figures 3.48a and 3.48b clearly show the pattern transfer through the Si device layer and the 10 nm thick SiO_2 mask, demonstrating accurate etching control throughout the entire device layer.

Chapter 4

Advanced devices on SOI

This chapter investigates some of the device functionalities realized on the doped SOI platform, highlighting their relevance for developing advanced electronic applications and unconventional computing devices. This section of the work illustrates the crucial role of SOI-based structures as a platform for exploring fundamental charge transport phenomena and for pushing the boundaries of unconventional and quantum electronics.

First, I present the fabrication and initial results obtained from eight-contact devices designed for unconventional computing. This section highlights the potential to implement novel computational architectures within a well-controlled SOI platform. Next, I describe in detail the fabrication steps developed for the realization of junctionless transistors on doped SOI films, taking advantage of their simplified design. Finally, I discuss the electrical characterization of nanotransistors fabricated on co-doped ultrathin SOI films, performed at the Research Institute of Electronics (RIoE) laboratories at Shizuoka University in Hamamatsu, Japan. I present the low-temperature measurements carried out to investigate and provide evidence of Coulomb blockade and single-electron tunneling through dopant-induced quantum dots in the Si nanochannel.

4.1 Unconventional computing on SOI

This part of the work was carried out within the framework of the Italian PRIN project *DONORS* (grant number 2022WBPHKF, Figure 4.1). The project received funding from the Italian programme for Research Projects of National Interest (PRIN) in the framework of the National Recovery and Resilience Plan (PNRR).

The continuous miniaturization of CMOS technology has encouraged the research for alternative, so called Beyond CMOS computing paradigms, as discussed in section 1.1. The exponentially growing volume of data being generated, stored, transferred, and processed poses major challenges concerning energy consumption, memory bandwidth, and carbon footprint [143, 144]. This pursuit has given rise to the field of unconventional computation (UC), which exploits the intrinsic physical properties of materials and devices to implement

Figure 4.1: Logo of the PRIN project DONORS (grant number 2022WBPHKF) which funded this part of the research.

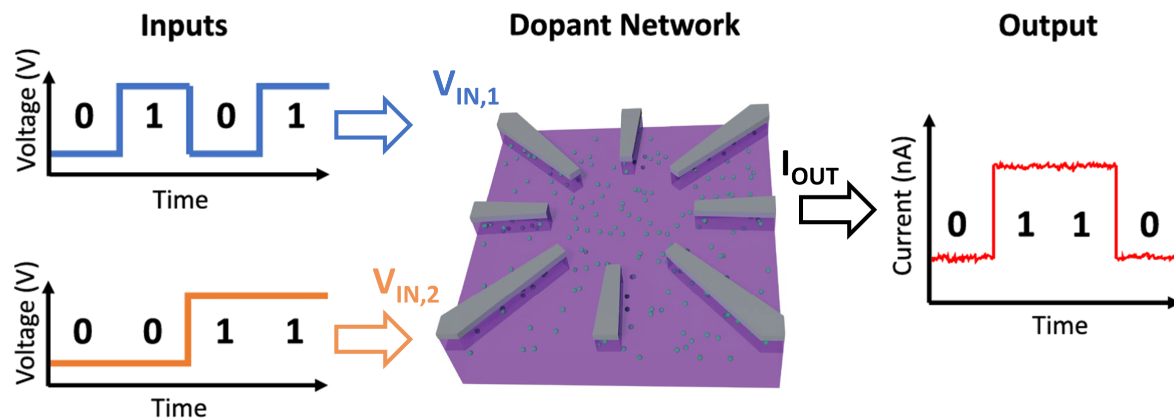


Figure 4.2: Sketch of the DNPU functionality. Applying a learned voltage configuration to the control electrodes implements the classifier, e.g., XOR, as an output current. Figure adapted from [147] and [148].

novel computing paradigms. UC aims to move beyond the classic Von Neumann architecture, overcome the energy-intensive data transfer between memory and processing units, and perform information processing in a more efficient, adaptive, and inherently parallel manner [145].

Unconventional computation explores a broad range of materials and nonlinear effects that can be exploited for computation. Drawing inspiration from physical, chemical, and biological systems, UC exploits the functional properties of matter to design architectures that support emergent computing behavior, as neuromorphic and reservoir computing. A promising direction is *in-materia* computing, which exploits the inherent physics of a material to perform computation. This concept drives the search for *intelligent matter*: materials capable of sensing inputs, adapting internal states, storing information, and learning from experience [146].

Recent research has shown that networks of disordered dopant atoms in Si can serve as the foundation for physical computing systems, the so-called Dopant Network Processing Units (DNPUs) in Figure 4.2 [147]. Originally developed at the University of Twente, The Netherlands, a DNPU is a nanoscale device consisting of a random network of acceptor or donor atoms in Si. The active area is designed by 8 electrodes positioned with a distance

between facing tips of ~ 300 nm. These devices have been proposed as a scalable platform for *in-materia* computing due to their intrinsic nonlinear response [147].

The DNPU response is generated by interactions between the electrodes and the substrate and can be tuned to yield complex nonlinear behavior, most importantly the Negative Differential Resistance (NDR). In a typical experiment, two electrodes are used to apply input voltages, one electrode measures the output current, and the remaining electrodes serve as control terminals which can be optimized to produce the desired outputs. It has been demonstrated that DNPUs can be reconfigured through artificial evolution to implement all basic Boolean logic gates [148]. The presence of an NDR region is crucial for solving linearly inseparable classification problems, such as the XNOR logic gate. Thus, NDR serves as an important signature of DNPU tunability [148].

Device optimization remains an active area of research. In bulk substrates, diffuse *n-p* junctions can cause significant leakage currents, increasing power consumption and degrading performance. Transitioning the DNPU technology to the SOI platform offers several distinct advantages for improving performance, scalability, and reproducibility.

SOI substrates provide enhanced electrostatic control, reduced parasitic capacitance, and leakage. SOI substrates exhibit low defect densities and high-quality Si/SiO_2 interfaces, contributing to greater device reliability and reproducibility. Finally, H_{SOI} can be precisely controlled down to ~ 10 nm, while maintaining uniform doping profiles, enabling fine control over the active region. The well-defined geometry and reduced dimensionality of SOI films enable the systematical investigation of the nonlinear charge transport and collective electronic effects that drive the complex multi-contact DNPU operation. In summary, the adoption of SOI technology is a natural step toward the optimization of DNPUs, combining the maturity of Si processing with the structural and electrostatic advantages of the SOI platform.

4.1.1 Device fabrication

This section provides a comprehensive description of the fabrication process for the multi-terminal devices realized on SOI substrates.

Initial photolithography tests were performed on bulk Si substrates to determine the minimum feature dimensions achievable with the AZ5214 resist and the μMLA 150 system. After opening of the resist mask, the SiO_2 native oxide is removed by bath in 30:1 BOE. A test mask was designed on KLayout software to investigate the effect of contact width, tip angle, and spacing (Figure 4.3a and 4.3b) The width of the contacts was varied from 1 to 5 μm with a step of 0.5 μm. The shape of the tip was varied between a round shape, and point tip with an angle ranging from 90° to 15°. Actually, the main limiting factor for spacing is the width of the contacts themselves. Insufficient spacing resulted in lines and features that cannot be resolved individually. Figure 4.3b shows the SEM images after Al deposition and liftoff showing merged contacts as a result of excessive scaling in the spacing between the electrodes.

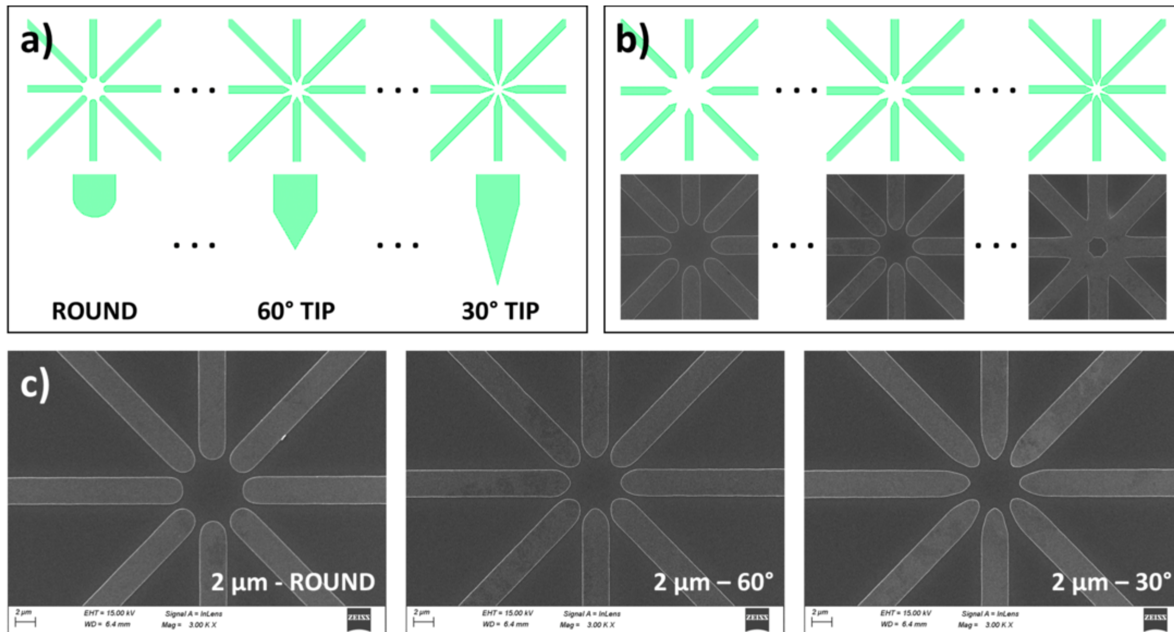


Figure 4.3: Initial photolithography tests on bulk Si showing the variation of tip shape (a) and contact spacing (b). SEM images of Al contacts after lift-off, illustrating the merging of contacts with insufficient spacing. (c) SEM images of the three optimized configurations of Al contacts after lift-off.

The SEM images upon liftoff of the optimized configuration are shown in Figure 4.3c. The contact line width is fixed at 2 µm and the Al thickness at $80 - 100$ nm in order to favor the lift-off process. Three design tip shapes are employed: rounded, 60°, and 30°. The spacing is optimized such that the diagonal distance between two adjacent tips was approximately 1 µm. While sharper tips (30°) are rounded during processing, they allow for closer effective positioning of the Al contacts, with a distance ~ 5 µm between facing tips. The three different shapes are employed in the final design to investigate the effect of different tip shapes and reduce the effective distance between electrodes.

The sample preparation procedure for SOI involves an additional patterning and mesa definition step to define the active area of the device. Circular 20 µm diameter regions and alignment marks were patterned on the device layer via wet etching in 22 wt% KOH, following the procedure described in Section 3.2. The eight Al ohmic contacts and metal pads were aligned and deposited via thermal evaporation, following a subsequent photolithography step. After opening of the resist mask, the SiO_2 is removed by bath in 30:1 BOE. The Klayout design of the entire device together with the contact configuration of the three different shapes is shown in Figure 4.4.

Figure 4.5 reports the SEM images obtained of the active area on the first 30 nm thick SOI at the end of the process, after mesa patterning and contact deposition. The darker

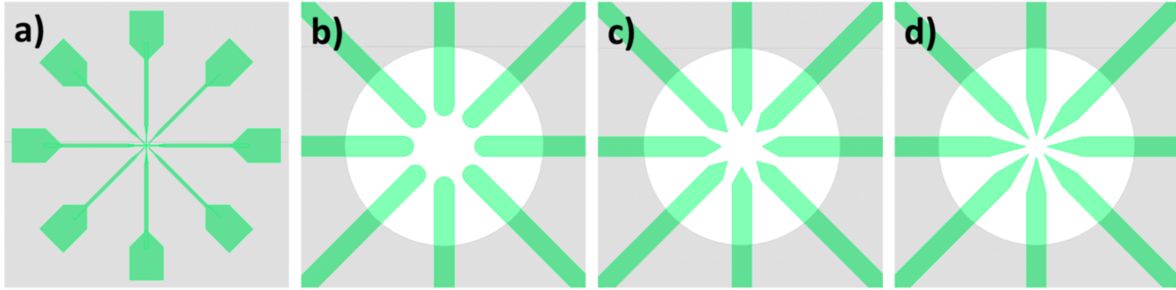


Figure 4.4: Mask design on SOI. (a) Schematic showing the overview of the entire design of a SOI DNPU device. Zoomed-in active regions showing the design of the circular mesa (white) and the geometries of the 8 Al contacts (green): (b) rounded tips, (c) 60° tips, and (d) 30° tips.

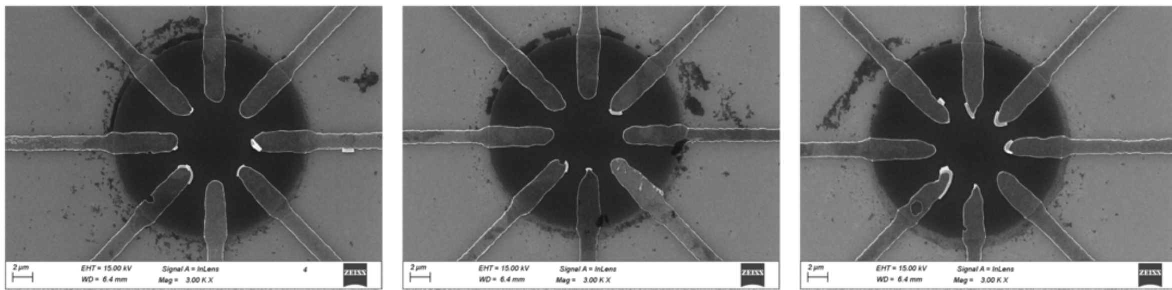


Figure 4.5: SEM images of the active regions of the initial test on SOI showing successful mesa patterning and contact alignment, but with clear evidence of non-uniformity and line edge roughness of the Al contacts.

color indicates the circular Si active area while the lighter one corresponds to the SiO_2 BOX underneath, exposed after etching and removal of the Si device layer. Initial tests on SOI successfully reproduced the mask design.

However, closer inspection of the Al contacts revealed significant edge roughness and non-uniformity. This suggested insufficient development time, leaving resist residue at the corner of the openings, which caused the Al deposited on top to be subsequently removed during the lift-off process. Furthermore, the mesa step increased the criticality of the metal deposition, as the steep topography could lead to breaking or thinning of the deposited Al wire at the edge. To address these issues, additional over-etching during the development step and longer O_2 plasma clean were introduced. While necessary, increasing the time in the developer solution is highly critical: it causes each line to widen significantly, increasing the risk of the contacts merging. This trade-off between residue removal and preventing lateral line widening makes the development of the Al contacts the most critical step in the sample preparation, particularly due to the high sensitivity to local variability in the thickness of the resist mask.

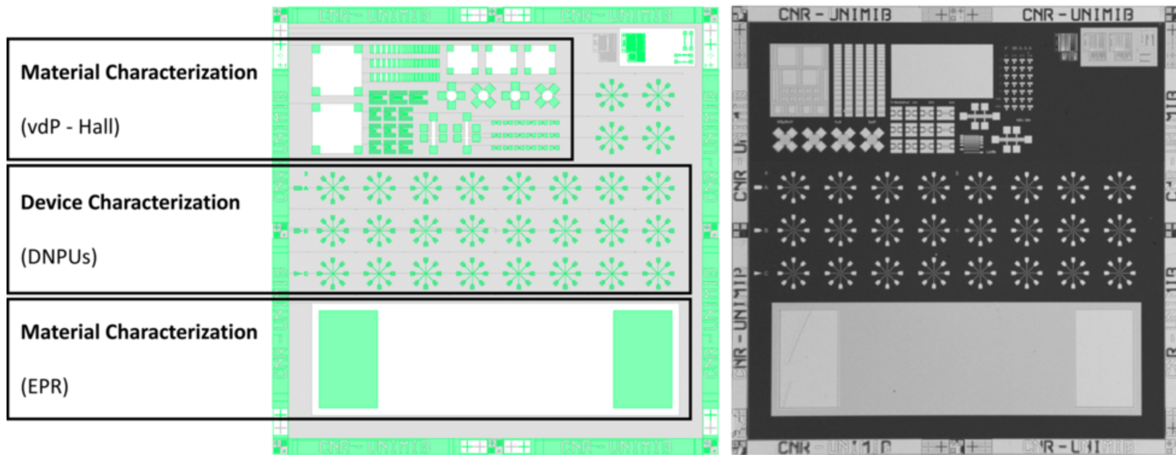


Figure 4.6: (a) Improved mask design on SOI, showing the three distinct characterization regions on the 1.1 × 1.1 cm^2 chip for material and DNPU Characterization. (b) Image of the complete mask realized on SOI at the end of the process.

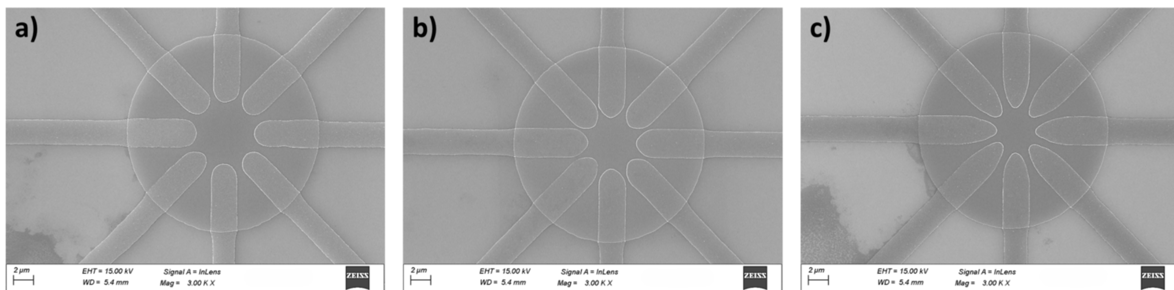


Figure 4.7: SEM images of the active regions demonstrating improved quality of the process. (a) Rounded tip design resulting in a distance of 6 μm between facing tips. (b) 30° tip design resulting in a distance of 5 μm. (c) 60° tip design resulting in a distance of 4 μm.

The improved final mask design which was developed to allow for the entire characterization process on a single 1.1 × 1.1 cm^2 SOI chip, is shown in Figure 4.6a. The design of the chip is divided into three regions aiming for the characterization of the film material at the macroscale for sheet resistance and Hall measurements in vdP configuration (top) and EPR analysis (bottom), and DNPU characterization for multi-terminal IV measurements (center). A small region in the top right is also reserved for EPR characterization during DNPU operation to investigate potential spin-dependence of the device functionality. At the end of process, the finished chip is manually diced into each individual sections and cleaned in isopropanol before characterization.

Improvements in sample preparation and processing yielded a complete, high-quality chip as shown in Figure 4.6b. The active region of this second generation mask is shown in

Figure 4.7. Accurate mesa patterning is achieved, and the Al contacts were well-aligned with minimal line edge roughness, validating the optimized process flow. The effective width of each Al contact at the end of the process is ~ 2.5 μm. The rounded sharper tips enables a minimum spacing between two adjacent contacts down to ~ 750 nm and resulting in reduced active areas. The resultant distance between facing Al electrodes is therefore progressively reduced by changing the tip shape: from ~ 6 μm for the rounded contact, to ~ 5 μm for the 60° tip, and to ~ 4 μm for the 30° tip (Figure 4.7).

4.1.2 Material characterization

Understanding the physical properties of the material is crucial to understand the device functionality, which constitute the foundation of *in-materia* computing approach.

The first-generation SOI-DNPUs were fabricated on SOI sample with $H_{SOI} \sim 30$ nm. The doping process was carried out using PS-P polymers via the *Double Annealing* approach, described in detail in section 3.2. The first drive-in treatment was performed at 1000°C for 1 s. The process was optimized to target a donor concentration $n_D \sim 1 \times 10^{18}$ cm^{-3} in order to guarantee ohmic contacts between the Al electrodes and the Si active region. After the removal of the 10 nm e-beam SiO_2 capping layer used to prevent out-diffusion of the P dopants during the second redistribution treatment at 1000°C for 100 s, a 2 nm SiO_2 capping layer was chemically grown via SC2, following the same procedure described in section 3.2. Mesa patterning and Al contacts deposition followed the same mask design and processing steps described for the test SOI substrate.

ToF-SIMS analysis of the sample was performed at the end of the process in one of the 4PP vdP test structures. Figure 4.8a confirms that the P concentration is uniform throughout the 30 nm device layer, with an average concentration determined to be $n_D \sim 9.0 \times 10^{17}$ cm^{-3}. This concentration value is close to the sensitivity limit of the instrument around 1 to 2×10^{17} cm^{-3}, justifying the observed variability. The spot size of the SIMS analyzer beam, 100×100 μm^2, is not significantly larger than the dimensions of the active area to assume significant n_D variations in the device region compared to the flat. This concentration is expected to result in a dopant mini-band at room temperature [92].

Room-temperature IV measurements on the 4PP vdP geometry are shown in Figure 4.8b. Current is injected across two contacts (I_{jk}) and the voltage drop is measured across the same two (V_{jk}). IV measurements demonstrate linear and uniform resistance, confirming the high quality of the lithography and the ohmic Al contacts at this n_D value. Moreover, adjacent versus opposite contacts correctly show higher resistance for longer-distance paths ($V_{14}I_{14}$ versus $V_{24}I_{24}$), supporting good sample uniformity. The room-temperature electron dose was determined by Hall measurements in four different 4PP test structures. The average value was $N_e = (1.5 \pm 0.6) \times 10^{12}$ cm^{-2}.

The low-temperature evolution of R_s (top) and N_e (bottom) is reported in Figure 4.9a. R_s increases as the temperature decreases, correctly correlating with the reduction of N_e and confirming the thermally activated conduction in the 30 nm thick active layer. Fitting of the

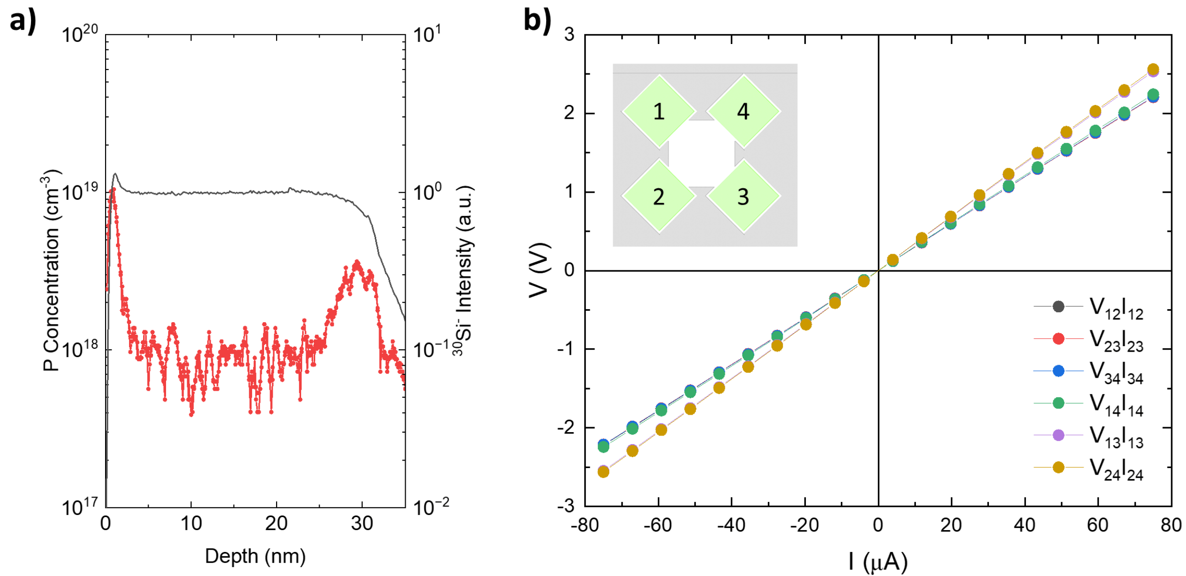


Figure 4.8: (a) ToF-SIMS P depth profile (red) confirming uniform doping throughout the 30 nm device layer. The $^{30}Si^{-}$ signal (black) is also reported to show the SOI structure. (b) Room-temperature IV measurements on 4PP vdP geometry.

conductivity allowed for the determination of the dopant activation energy in the sample, $E_a \sim 29.2$ meV, and a dopant mini-band of ~ 2 meV compatible with values for SOI in this H_{SOI} and doping range.

The EPR spectra obtained at $T = 4.2$ K in the same doped chip are shown in Figure 4.9b. The detection of a single P dopant line ($g = 1.9996$) confirms a high concentration of active dopants. No hyperfine interaction of isolated P was detected [116]. Information about interface quality are provided by the two distinct lines ($g = 2.0028$ and $g = 2.0071$) attributed to P_{b0} centers, the interface defects present at the non-passivated SC2-SiO_2/Si TOX interface as discussed in Section 3.6. Finally, a broad peak with $g = 2.0056$ is attributed to any additional Si dangling bonds contribution and to wafer dicing.

4.1.3 Negative differential resistance and tunability

The first-generation of SOI-DNPUs were characterized at room temperature using two and three electrodes IV measurements to identify the characteristic nonlinear response and tunability required for *in-materia* computing.

Two-electrode IV neasurements between contacts are shown in Figure 4.10a. The results show linearity only in a small voltage range, with high-field non-linearity appearing at higher currents. This evolution suggests a potential small Schottky barrier at the Al-Si contact interface, contrasting with the ideal linear response observed for much larger contacts (Figure 4.8b). The current correctly scales with the distance between contacts, validating

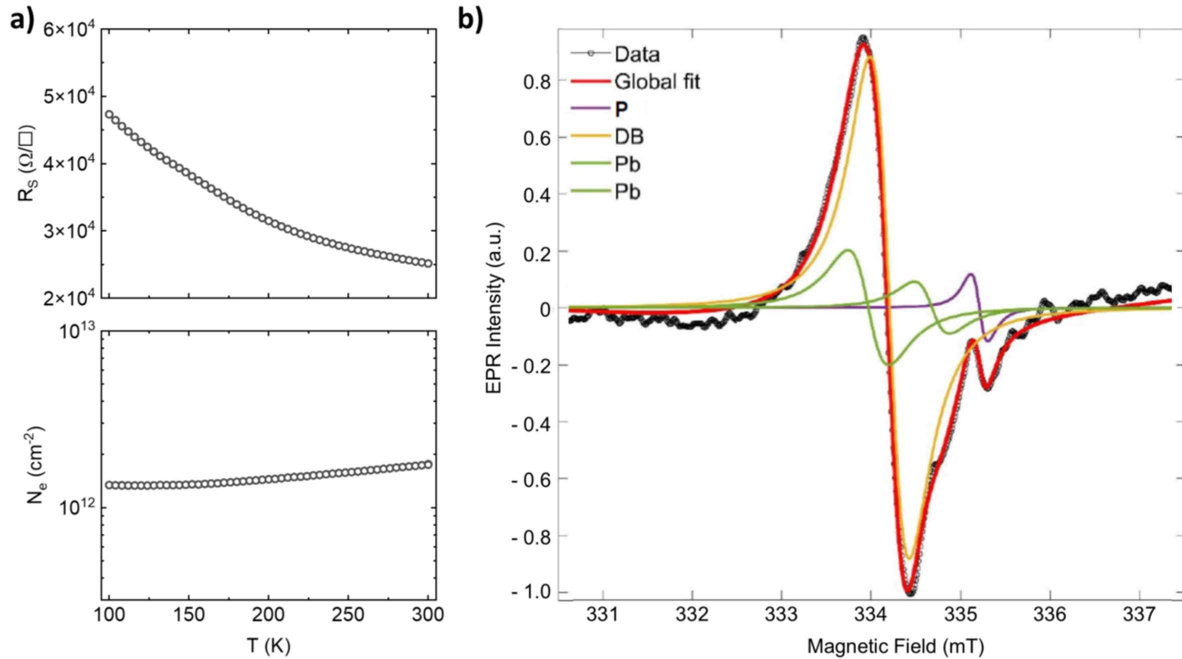


Figure 4.9: Material characterization of the doped SOI film. (a) Low temperature evolution of the R_s (top) and N_e (bottom). (b) EPR spectra obtained at $T = 4.2$ K indicating the presence of a single line attributed to P dopants and P_{b0} interface defects.

the fabricated geometry. Minor device-to-device variability was observed, indicating small local non-uniformities within the active region and the Al contacts. Devices with larger tip distance showed higher resistance, correctly correlating with reduced contact area and increased electrode spacing used in the different configurations.

The tunability and functionality of the SOI-DNPUs was demonstrated by applying a voltage to a third control electrode. IV measurements obtained with three electrodes are shown in Figure 4.10b. The applied control voltage (V_C) introduces a more complex, nonlinear response. Crucially, applying a negative control voltage effectively tunes the response to achieve NDR at room temperature. Significant variations and improved control is observed when V_C is applied to the electrodes closer to the output one. Asymmetric response is found when changing two opposite control electrode, highlighting some local variability in the disordered dopant network and contacts quality.

The successful demonstration and control of NDR at room temperature in a micro-scale system is highly significant. The larger dimensions are much easier to control, and the integration of this protocol with the precise control over H_{SOI} and n_D granted by the SOI platform is extremely promising. Initial tests already demonstrated controllabale non-linear response which offered greater tunability than the first generation of DNPUs on bulk Si. Actually, the physics of this multi-electrode system is complex and is yet not fully understood.

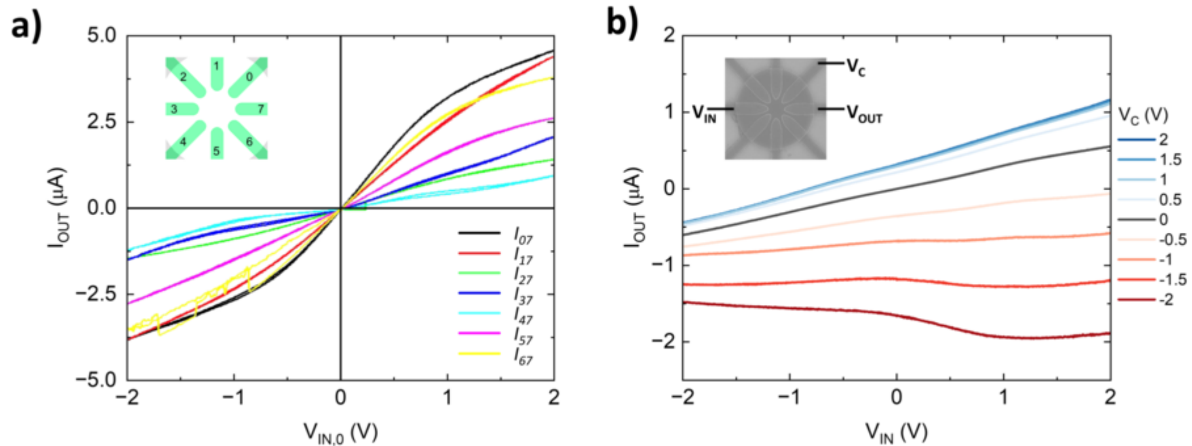


Figure 4.10: Room-temperature IV characterization of the SOI-DNPU. (a) Two-electrode IV measurements between contacts. (b) Three-electrode measurements demonstrating tunability and the presence of NDR when a negative control voltage is applied to one of the electrodes.

The presence of non-passivated interface states at the SC2-SiO_2/Si TOX interface induce a depletion of the channel, effectively reducing H_{eff}. This effect, discussed in detail in Section 3.6, is beneficial as the reduced dimensions can enhance the nonlinear response of the device. H_{eff} was determined to be ~ 23 nm by comparing the results of the electrical and compositional analysis. Significant variations in the conduction mechanisms itself should not be expected in the conductive layer considering this H_{eff} value. However, variations in the depleted regions created underneath the Al contacts by the polarization of Schottky barriers as well as the back handle wafer could contribute to the observed NDR by closing the channel. Investigations are needed to clarify the origin of the observed reproducible NDR at room temperature. The ability to control all processing parameters will allow for systematical investigation and correlation of the underlying physics driving the SOI-DNPUs functionality, paving the way for optimized SOI-based DNPUs for boolean logic and other unconventional paradigms.

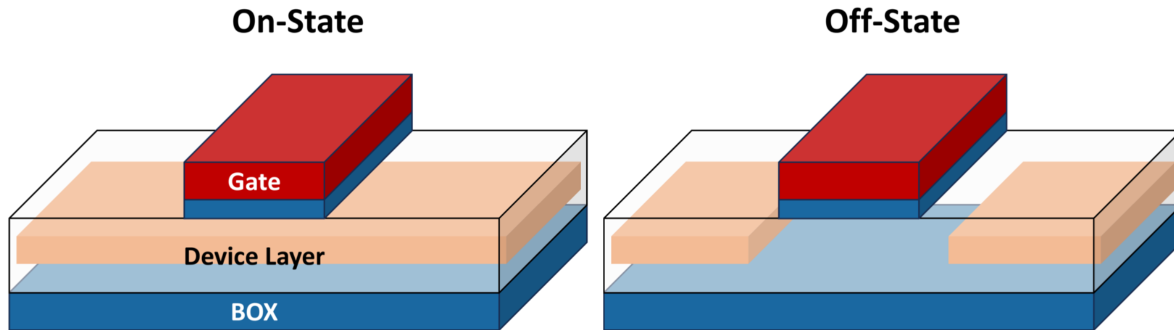


Figure 4.11: Illustration of the effect of the gate voltage on the conductive channel (orange) in JLTs realized on SOI, in the on-state (a) and in the off-state (b).

4.2 Junctionless transistors on SOI

One alternative promising approach for transistor scaling is to eliminate the requirement for abrupt *p-n* junctions entirely. Conventional transistors (such as *npn* or *pnp*) rely on junctions to define the source (S) and drain (D) regions. Devices that remove this requirement are called Junctionless Transistors (JLTs) [149]. Unlike conventional MOSFETs, the JLT architecture relies on a uniformly doped channel whose conductivity is modulated by the gate electrode.

The schematic mechanism of JLTs is shown in Figure 4.11. A JLT can function as an ON/OFF switch depending on the polarity and intensity of the gate voltage applied. Complete pinch-off of the conductive channel results in cut-off and full-depletion of charges in the conductive path between the S and D regions, bringing the JLT in the off-state. Control of the conductive channel by the gate electrode and good electrical properties can happen only if it maintains both a sufficiently high doping level and a very low channel dimensionality [149].

JLTs remove the complexities associated with forming and controlling *p-n* junctions in typical FETs, particularly minimizing dopant-fluctuation effects at these boundaries, which are particularly crucial for reduced dimensions but do not inherently solve issues related to the discreteness or statistical fluctuation of dopants within the channel itself. This design inherently reduces fabrication complexity and minimizes short-channel effects, making it highly suitable for micrometer and nanometer-scale technologies. The incorporation of this device structure on SOI substrates offers a promising approach for high-performance electronic devices due to their simplified fabrication process and enhanced electrostatic control by the presence of the BOX.

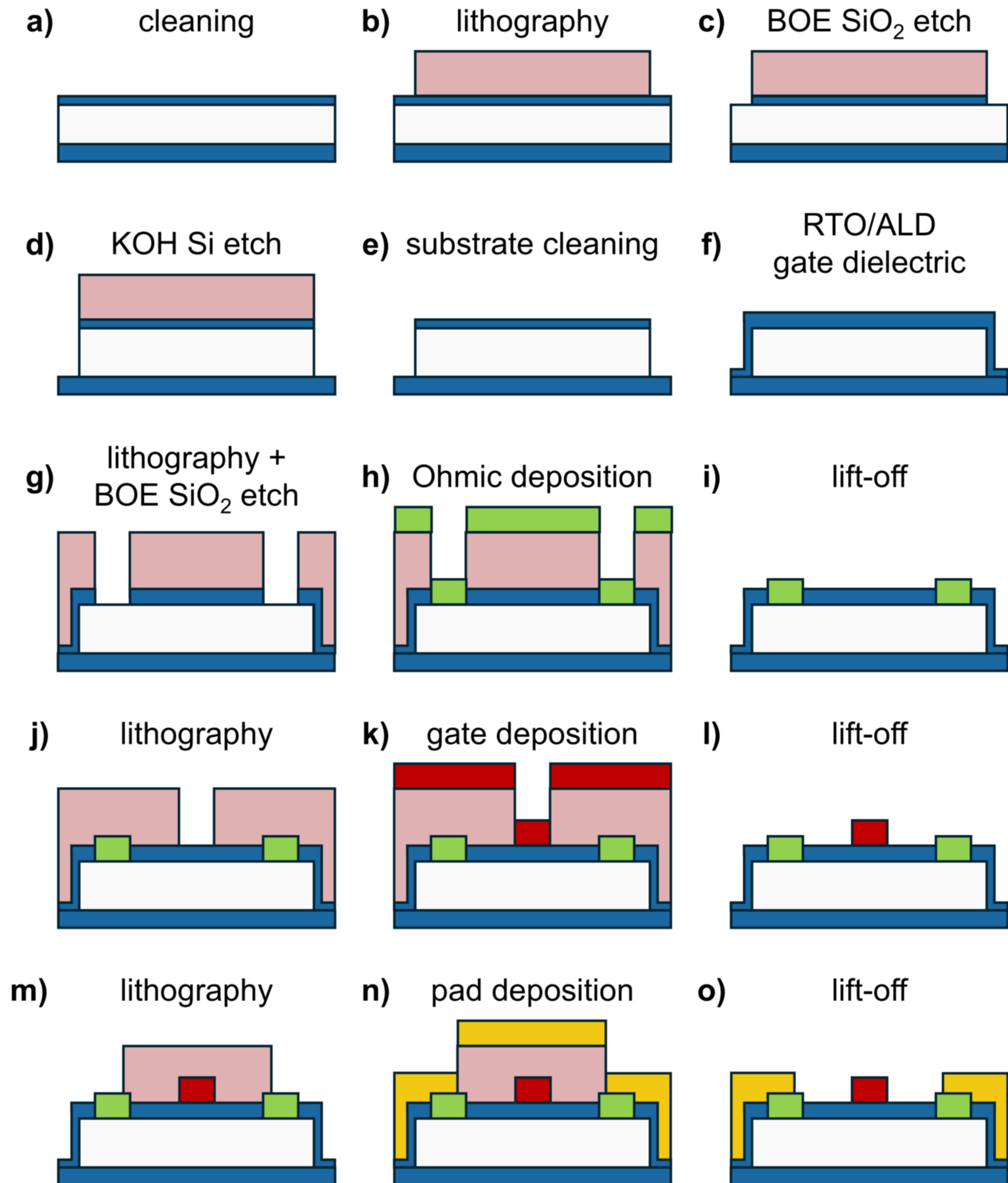


Figure 4.12: Full process flow for the fabrication of JLT on SOI samples.

4.2.1 Device fabrication

The fabrication process of JLTs take advantage of the SOI platform and the inherent simple JLT architecture. This process was developed following training in advanced lithography procedures at the IAP laboratories of the Technische Universität Bergakademie Freiberg in Germany, enabling the implementation of complex procedures previously unexplored in our CNR-IMM lab on the Si platform. The entire process flow is reported in Figure 4.12 and involves four main lithography exposures:

1. **Substrate doping:**
   The sample is thinned down to reduce H_{SOI} and doped following the procedure described in section 3.2. The processing parameters are varied in order to tune the desired n_D in the device layer.

2. **Mesa definition:**
   The substrate is cleaned by acetone and isopropanol bath for 5 min (a). The first lithography step defines the active regions of the JLT as well as the source and drain areas (b). An O_2 plasma cleaning is performed to ensure a high-quality and complete opening of the resist mask after each opening step. The exposed SiO_2 capping layer is wet-etched in 30 : 1 BOE (c), followed by subsequent etching of the Si device layer using 22 wt% KOH at room temperature until the BOX is reached (d), electrically isolating individual devices. The width of the active area typically varies between 5 and 50 μm.

3. **Gate oxide formation:**
   After residual resist removal in acetone (e), the sample undergoes an RTO at 90 °C to grow a thin, high-quality SiO_2 layer that will serve as the gate dielectric (f). Different materials and procedures can be implemented to vary the gate dielectric.

4. **Source and drain contacts deposition:**
   The second lithography step aligns and patterns the source and drain leads at the edges of the active areas. 30 : 1 BOE etching is used to selectively remove the gate oxide layer in these areas, ensuring ohmic contact (g). ~ 150 nm thick Al contacts are deposited via thermal evaporation (h) and subsequent lift-off in acetone (i).

5. **Gate contact deposition:**
   The third lithography step patterns the gate electrode, precisely aligned between the source and drain contacts, above the oxidized channel region (j). The width of the gate electrode typically varies between 2 and 5 μm. ~ 150 nm thick Al contacts are deposited via thermal evaporation (k) and subsequent lift-off in acetone (l).

6. **Pad contacts deposition:** The fourth lithography (m) and Al metallization sequence (n) forms the large-area bonding pads for external electrical probing and wire bonding (o).

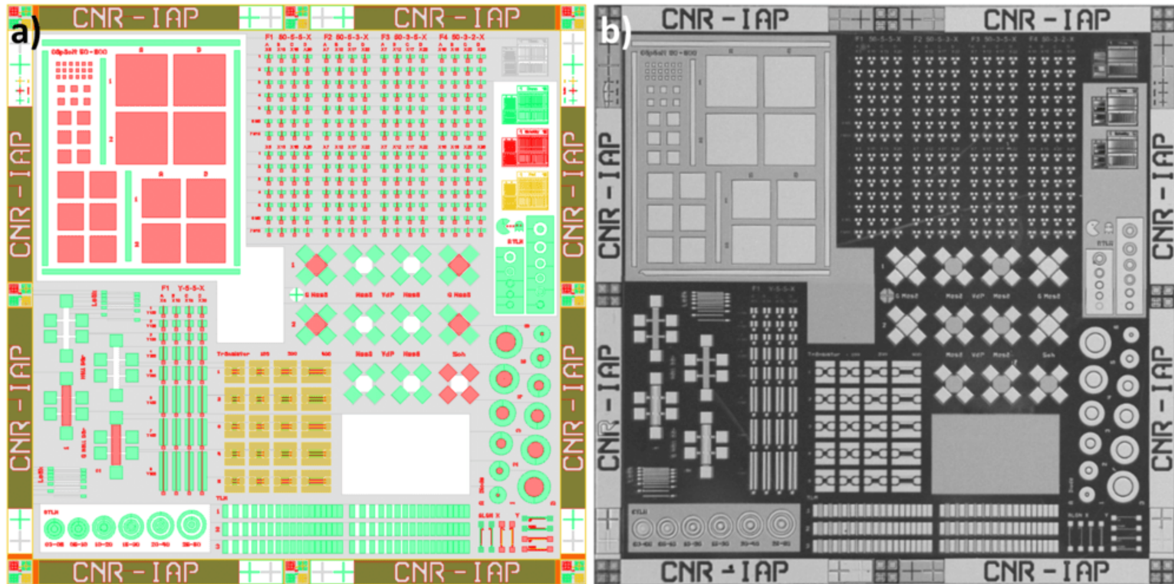


Figure 4.13: (a) Transistor Mask design, integrating vdP structures, Hall bars, capacitors, contact resistance patterns, and JLT arrays. (b) Image of the chip fabricated at the end of the process.

The KLayout mask (Figure 4.13a) developed, incorporates several regions and structures for the complete characterization of both devices and material on a single chip.

Non-patterned regions are included for ToF-SIMS P depth profiling in the device layer to determine the exact n_D value and to verify the uniformity of the P distribution. Material characterization structures are implemented for sheet resistance (R_s) and Hall measurements (N_e) using both 4PP vdP and Hall bar geometries, as well as for contact resistance measurements to evaluate the quality of the Al/Si contact. Circular TLM are introduced to minimize the contribution of contact transfer leght and improve the accuracy in ultrathin films. To assess the gate oxide quality, MOS capacitors are patterned for CV measurements, which enable the direct evaluation of the oxide integrity and extraction of the D_{IT}. Finally, JLT Devices are included, fabricated with varying channel lengths and widths, as well as different gate widths, to investigate the effect of device geometry on the performance.

The successful implementation of this advanced photolithography process is shown in Figure 4.13b. It demonstrates the improved capability to produce complex transistor structures on the SOI platform in the CNR-IMM laboratory and offers a promising path toward nanoscale device realization. The first generation of samples has already been fabricated and are ready for the comprehensive electrical characterization of the performance of the JLTs devices.

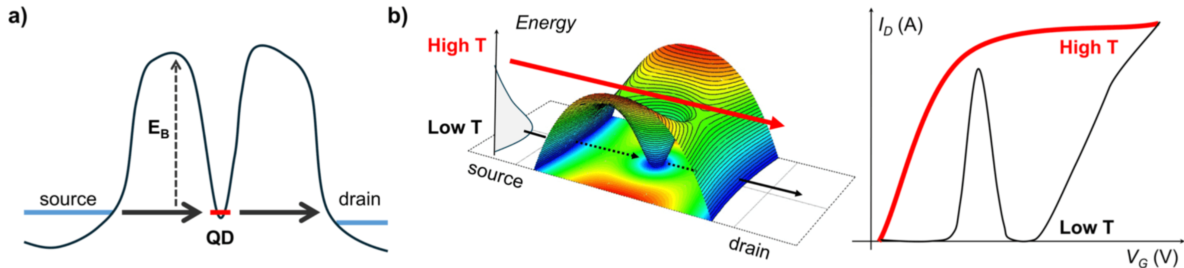


Figure 4.14: (a) Schematic energy band diagram showing Single-Electron Tunneling (SET) mechanism through a QD at low temperature. (b) Current-Voltage characteristics at low and high temperatures, illustrating the transition from SET current peaks to Field-Effect Transistors (FET).

4.3 Single-electron tunneling

The search for *Beyond CMOS* computing has led to alternative conduction mechanisms, with Si-based Single-Electron Tunneling (SET) transistors being the focus of this section of the work [150]. SET devices operate by controlling the quantum tunneling of individual electrons through nanoscale islands, the quantum dots (QDs). Si-based QDs can be formed by intentionally Si nanostructures or naturally occurring potential wells around dopant clusters. These QDs are isolated from the source and drain leads by tunnel barriers with a height E_B which prevents thermally-activated current to flow over the barrier.

The operational principle is governed by the Coulomb blockade theory [151], which dictates that the electrostatic repulsion from a single electron localized in the QD well raises the energy of the system by a quantity defined as charging energy E_{ch}, effectively blocking the addition of further electrons until the gate potential is precisely tuned or the thermal broadening of the Fermi-Dirac distribution in the leads is sufficient to overcome the Coulomb blockade effect. This mechanism, illustrated schematically in Figure 4.14a, provides the foundation for ultra-low-power functionalities by controlling charges at the elementary level.

In the context of Si nanodevices, dopant atoms, such as P donors or B acceptors, are not merely carrier providers but can act as host sites for an extra electron or hole, effectively behaving as naturally occurring QDs [152, 153, 154]. Typically, SET effects are only observable at cryogenic temperatures ($\sim 8 - 15$ K) where SET via single dopants can be resolved [155]. Figure 4.14b illustrates the temperature-dependent conduction:

- **Low temperature:** A current peak is observed only when V_G aligns the QD energy state with the source Fermi level, allowing SET. The tunneling probability is directly related to the geometry and height of the energy barrier that controls the Coulomb blockade, i.e, the distance of the QD from the leads and E_B.

- **High temperature:** Thermal energy k_BT becomes sufficient to overcome the E_{ch} and the barrier E_B. Conduction is no longer limited by SET, and the device transitions to

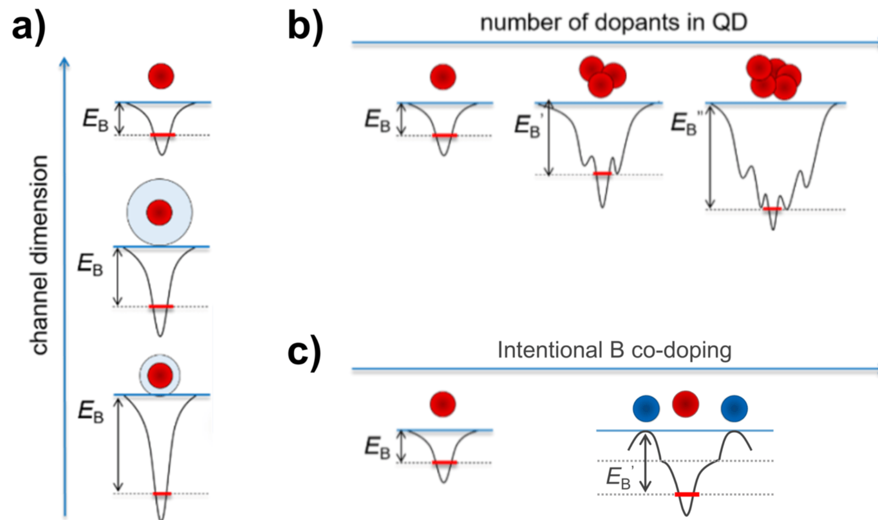


Figure 4.15: Strategies for increasing the SET operation temperature: (a) reducing channel dimensions, (b) utilizing dopant clusters, and (c) employing co-doping to enhance the charging energy E_{ch} and tunnel barrier height E_B.

typical FET behavior.

A critical challenge is to raise the SET operation temperature for practical applications. This requires maximizing both E_{ch} and E_B. As shown in Figure 4.15, this is achieved through three complementary strategies which rely on significantly reducing the dimensions of the channel (a), using clusters of a few dopants (b) and co-doping (c).

- **Reduced dimensionality:** Reducing the physical dimensions of the channel enhances quantum confinement and dielectric mismatch effects, which deepens the ground-state energy level by increasing the dopant ionization energy [30].
- **Dopant clustering:** When two or more donors are closer than the Bohr radius ($r_B \sim$ 2.5 nm) but separated by Si atoms, their wave functions couple. This P-cluster acts as a single, deeper QD, resulting in an enhanced E_B [156, 157]. Actually, more finer, smaller peaks are also associated to multi donor QDs.
- **Co-doping:** The intentional introduction of both donors (P) and acceptors (B) provides an electrostatic way to enhance the potential barriers surrounding a donor QD. Moreover, compensation effects reduces the effective dopant concentration in the channel. Strategically located acceptors can effectively increase E_B, further boosting E_{ch}.

This section explores the use of co-doping in Si nanostructures, suggesting that the interaction between donors and acceptors in nanoscale channels can enhance both the

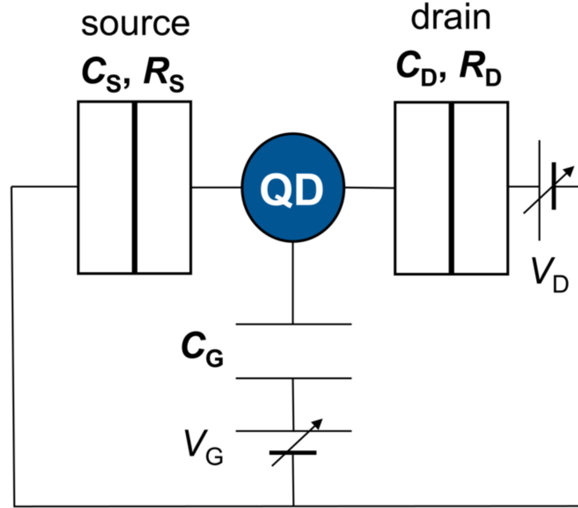


Figure 4.16: Equivalent circuit of a single QD SET transistor, showing the capacitances (C_S, C_D, C_G) and tunnel resistances (R_S, R_D) of the source, drain, and gate couplings.

process yield and the tunability of electron-transport properties, thereby potentially raising the SET operating temperature. Specifically, we address the basic effects of co-doping on electron transport through P-donor clusters embedded in Si nanotransistors.

4.3.1 Theoretical background of single-electron transport

The SET transistor system consists of an island (QD) capacitively coupled to the gate (C_G) and coupled to the S and D by two tunnel junctions modelled by C_S, C_D and R_S, R_D [158, 151]. Its equivalent circuit is shown in Figure 4.16.

The fundamental requirements for observing SET transport are high E_{ch} and high tunnel resistance. The energy required to add a single electron must be significantly larger than the thermal energy.

$$E_{ch} \gg k_B T \quad (> 10 k_B T) \tag{4.1}$$

This condition is necessary to suppress thermal fluctuations that would otherwise allow continuous current flow, thereby blocking the addition of a second electron in the QD.At room temperature, $k_B T \approx 26$ meV. Consequently, achieving room-temperature operation is extremely challenging with conventional shallow donors in silicon, as $E_{ch} \approx k_B T$. To overcome this limitation and maintain SET functionality at higher temperatures, it is essential to implement one of the strategies described above to significantly increase E_{ch}.

The tunnel resistance of the junctions must be greater than the quantum resistance (R_Q).

$$R_S, R_D \gg \frac{\hbar}{e^2} = R_Q \quad (\approx 25.8\ \text{k}\Omega) \tag{4.2}$$

This condition, derived from the uncertainty principle, is necessary to ensure that the electron is localized on one side of the tunnel barrier for a sufficient time, enabling the discrete, one-by-one tunneling description. Large R_S and R_D result in improved localization but significantly reduced measurable current. When these conditions are met, SET is described by the electrostatics of the equivalent capacitive circuit, which dictates the distribution of charges on each node. The theoretical formalism was described in detail in the literature for a single-QD system [158, 151] and it was also analytically extended to systems of two, three, and more QDs coupled to a single gate [159, 160, 161].

SET behavior is typically visualized by two signatures:

- **Transfer characteristics:** I_D-V_G or $|I_S|$-V_G plots show the characteristic current peaks only at certain V_G for a finite fixed V_D.
- **Stability diagram:** A contour plot of I_D (or $|I_s|$) in the V_G-V_D space, showing the Coulomb diamonds boundaries, which are diamond-shaped regions of near-zero current.

The QD properties can be extracted from the transfer characteristics and stability diagram features by analyzing the periodicity and slopes at the boundaries of the Coulomb diamonds. C_G is determined directly from the period ΔV_G between consecutive current peaks, based on the fundamental relation

$$C_G = e/\Delta V_G \tag{4.3}$$

Assuming a parallel-plate model, C_G then relates to the QD projected planar area (A_{QD}) and the thickness of the SiO_2 dielectric (H_{SiO_2}):

$$C_G = \frac{\varepsilon_0 \varepsilon_{SiO_2} A_{QD}}{H_{SiO_2}} \tag{4.4}$$

Actually, determining the effective H_{SiO_2} in the nanotransistor is quite challenging. A protocol developed exploits the gate leakage current (I_G) to grant information about its quality and thickness value by comparing the results to those expected for thin SiO_2 films [7]. Finally, the ratio between capacitances (C_S/C_D), which describe the coupling asymmetry of the QD to the S and D leads, are extracted from the positive and negative slopes of the Coulomb diamond boundaries (α^+ and α^-)

$$\frac{\delta V_D}{\delta V_G}^{-} = \alpha^- = -\frac{C_G}{C_D} \tag{4.5}$$

$$\frac{\delta V_D}{\delta V_G}^{+} = \alpha^+ = \frac{C_G}{C_S + C_G} \tag{4.6}$$

The resulting C_S/C_D ratio provides insight into the QD placement within the nanoscale conductive channel.

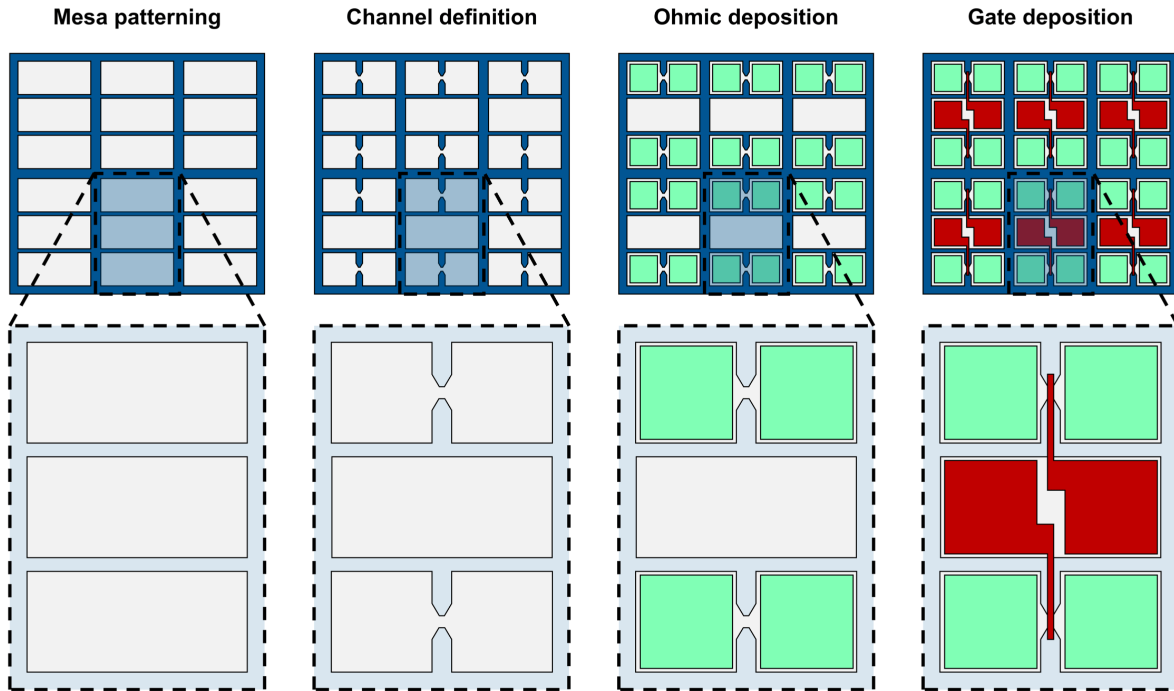


Figure 4.17: Schematic fabrication process flow for the co-doped SOI-SET transistors.

4.3.2 Device fabrication

To investigate the effects of co-doping, devices were already fabricated at the RIE laboratories in Hamamatsu, Japan, using a CMOS-compatible process based on a SOI FET structure [151]. This process is not different than the one developed in this work sor the SOI JLTs in Section 4.2. The schematic process flow is reported in Figure 4.17.

1. **Mesa and lead patterning:** Large Si pads and S/D extensions ($60 \times 60\ \mu m^2$) are defined using electron-beam lithography (EBL).

2. **Substrate co-doping:** Co-doping of the substrate was performed sequentially via spin-on-dopants. For P donors (OCD P-59230), pre-deposition is performed at 600°C in N_2 followed by drive-in at 860°C for 20 min in N_2. For B acceptors (PBF 6M-10), pre-deposition is performed at 600°C in O_2 followed by drive-in at 950°C for 5 min in N_2.

3. **Nanoscale channel patterning:** The nanoscale channel was patterned by EBl and etched using RIE. The designed width (W) was varied from 10 nm to 500 nm, and the designed length (L) ranged from 0 nm (point contact) to 100 nm.

4. **Gate oxidation:** RTO treatment is performed to grow the SiO_2 gate dielectric layer

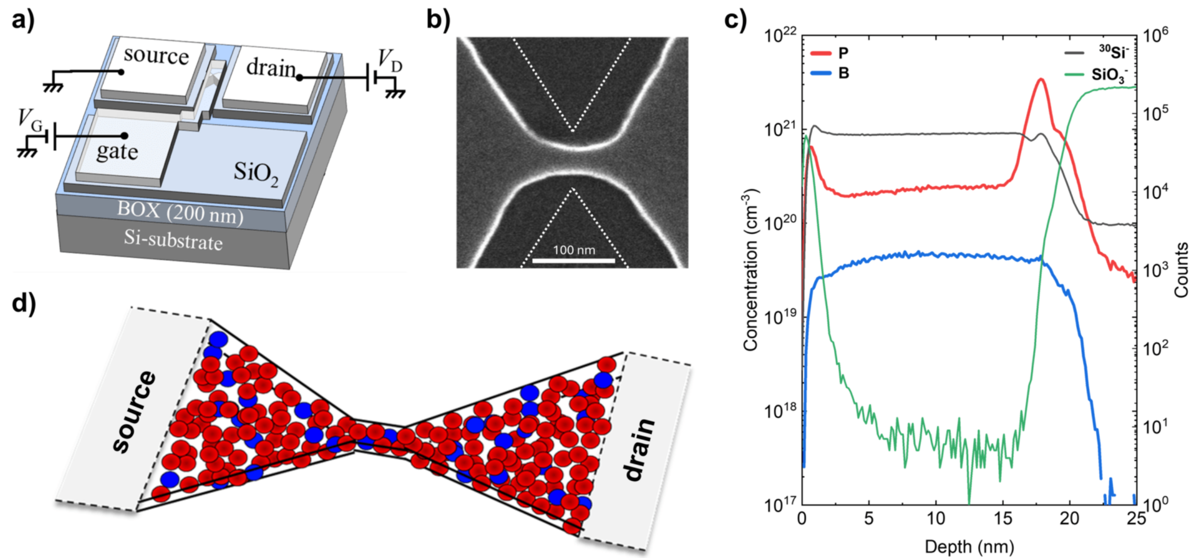


Figure 4.18: (a) Schematic of the SET nanotransistor. (b) SEM image of a nanoscale channel after processing with design $L = 0, W = 70$ nm (also shown for reference). (c) ToF-SIMS depth profile on a flat co-doped sample. (d) Schematic of the co-doped nanoscale channel illustrating P (red) and B (blue) dopants.

with a target thickness of 9 ± 1 nm.

5. **Contact formation:** ohmic contact openings were created, followed by lift-off process to form ~ 250 nm thick Al electrodes for source and drain electrodes. A subsequent deposition aimed for the deposition of the gate contact.

The complete structure of the device is shown in Figure 4.18a. Due to the RTO process, which is isotropic and orientation-dependent, the final dimensions of the nanoscale channel are significantly altered from the design ones. The width (W) is reduced, and the length (L) is increased. For instance, a device designed with $L = 0$ nm (point contact) and $W = 70$ nm resulted in final dimensions of $L_{eff} \approx 100$ nm and $W_{eff} \approx 40$ nm (Figure 4.18b).

ToF-SIMS measurements on a co-doped flat sample with final H_{SOI} after identical processing ~ 17 nm, are reported in Figure 4.18c. However, the RTO process in the nanoscale channel is enhanced by geometry effects and potential underside oxidation, resulting in a much thinner final Si channel thickness of $H_{SET} \sim 8$ nm. The measured average P and B concentrations in the device layer are $n_D \sim 2 \times 10^{20}$ cm^{-3} and $n_A \sim 5 \times 10^{19}$ cm^{-3}, respectively. A slight depletion of B is observed near the TOX interface, likely due to out-diffusion during RTO.

Electrical characterization via 4PP sheet resistance on the flat SOI suggested much lower carrier concentrations and almost complete compensation[151]. $n_e \sim 7.4 \times 10^{19}$ cm^{-3} and $n_h \sim 5.3 \times 10^{19}$ cm^{-3}. This large discrepancy suggests that a significant fraction of P donors

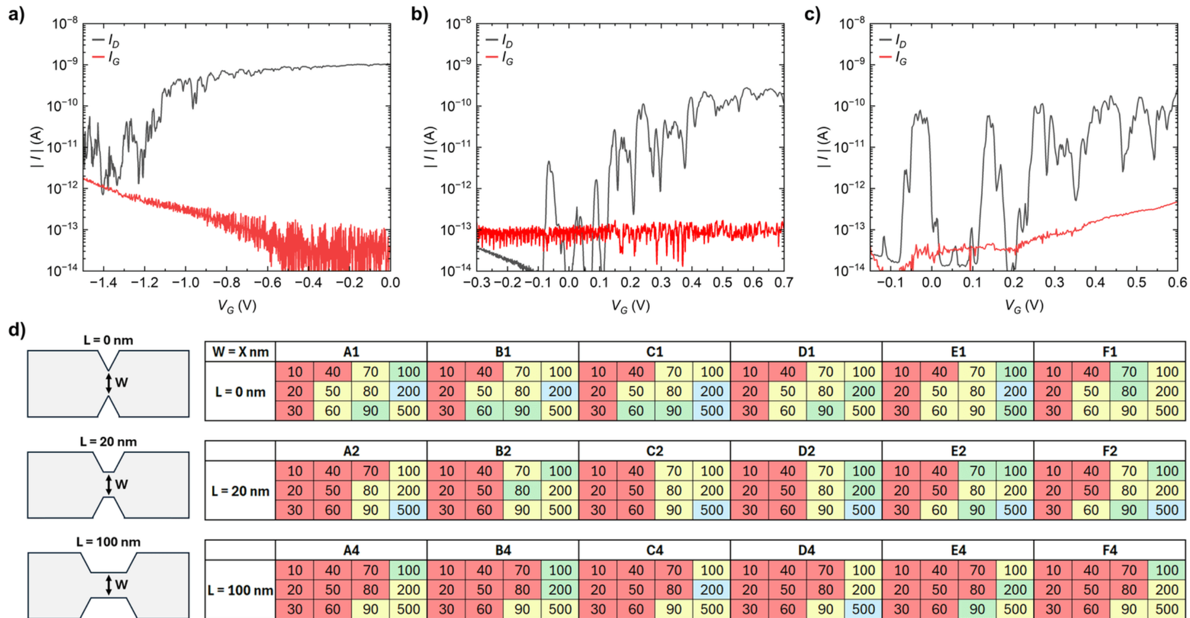


Figure 4.19: Example transfer characteristics showing SET with (a) negative V_G leakage, (b) ideal SET, and (c) SET with positive V_G leakage. (d) Yield map of SET behavior categorized by channel length and width. In red, devices which are physically disconnected. In yellow, devices either leaking or insulating. In green, fevices showing clear SET features. In blue, metallic devices.

may be electrically inactive. Some non-passivated interface states may trap carriers and reduce n_e. Furthermore, the calculation of the carrier concentrations from the extracted resistivity assumes bulk Si mobility, which is inaccurate for thin SOI films, as shown in previous sections. Lower mobility would result in effectively higher n_e. The large ~ 60 µm dimension of the S/D leads and the high dopant concentration shift the Fermi levels into the conduction band and ensure the leads are degenerately-doped and metallic, which guarantees ohmic contacts (Figure 4.18d).

4.3.3 Device yield and low-temperature characterization

Electrical measurements were performed at $T \sim 8$ K using a high-vacuum prober system with a current noise background of $\sim 10-50$ fA. The low background level enables the detection of a very small measured SET current. H_{SiO_2} was experimentally estimated to be ~ 2.8 nm based on comparison of the normalized gate leakage current density (I_G/A_G) to literature data for thin SiO_2 films [7]. While this reduced thickness results in higher I_G, it significantly improves the electrostatic control of the channel by the gate. To prevent dielectric breakdown, measurements were stopped if $I_G > 10^{-12}$ A $= 1$pA.

Figure 4.19a to 4.19c show typical SET transfer characteristics observed. All the samples measured showed clear, reproducible current oscillations peaks overlaid on a decreasing I_D as V_G was swept negatively. These features strongly indicate n-type SET transport, likely mediated by multiple-P QDs arrays uncompensated by the surrounding B. An ideal device (b) displays clear current peaks across the entire operating range with minimal leakage. A SET device with leakage at negative V_G (a), prevents the device from being fully turned OFF, and the first few ON peaks are not resolved. A SET device with leakage at positive V_G (c) in the ON FET state does not prevent the device from being fully turned OFF, and the first few ON peaks are well resolved. A protocol was introduced in order to fit each $I_G - V_G$ and subtract the gate leakage contribution if necessary. The H_{SiO_2} value extracted correlates with the different leakage behavior observed at even relatively small V_G in Figure 4.19. The different behaviors are the result of the shift in the threshold voltage (V_{th}) due to random dopant fluctuations and local variations in the gate stack composition or device geometry. In general, only (b) and (c) type SET devices were considered for SD analysis.

The yield map in Figure 4.19d classifies all the devices characterized at $T \sim 8$ K into four categories. Devices showing no conduction (red) are characterized by channels completely disconnected during processing (either during RIE or RTO), confirmed by SEM inspection of non-gated pairs. Therefore, these devices are excluded from statistical analysis. Samples with high leakage or insulating behavior (yellow) either have an inaccessible V_{th} due to excessive I_G or are entirely insulating. Wider channels (typically $W > 100$ nm) exhibits metallic behavior (blue), showing bulk conduction that was uncontrolled by V_G [151]. Devices demonstrating SET behavior (green) show clear current peaks and Coulomb blockade at low temperature.

A high SET yield of $\sim 25\%$ is observed for the $L = 0$ nm (point contact) design. Excluding the two widest channels, which are in principle expected to be metallic in this n_D range, this value is further increased. The yield stays consistent for $L = 20$ nm suggesting no significant differences in the geometry of the conductive channel and even increases to $\sim 30\%$ for the devices with $L = 100$ nm due to the significant higher fraction of disconnected devices which are not considered. Higher design L results in significantly elongated channels which can host a higher number of individual QDs in the nanoscale region between the S and D leads. The high yield verified across the chip suggests that the co-doping process leads to a favorable distribution of dopants, potentially creating well-isolated QDs more frequently, even at high nominal doping concentrations.

The stability diagrams were acquired for four $L = 0$ nm devices and are reported in Figure 4.20. The design W is varied between 60 nm (a), 70 nm (b), 80 nm (c), and 90 nm (d). The actual width W_{eff} measured by SEM inspection varies from ~ 28 nm to ~ 47 nm. Clear Coulomb diamonds (blue near zero-current regions) are identified. Initial diamonds are often well-defined, becoming more complex and smaller at higher V_G, as multiple additional conductive channels become accessible. The low variability in the stability diagrams across the designed widths correlates with the small variations in the final effective channel dimensions observed via SEM. Interestingly, sample (c) exhibits a significantly different,

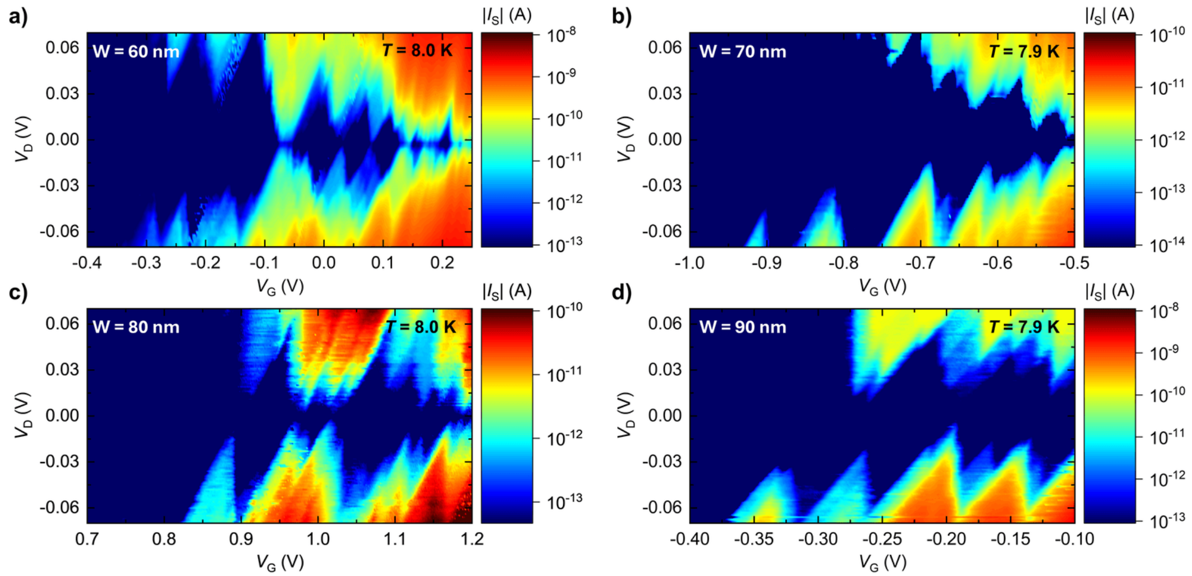


Figure 4.20: Stability diagrams ($\log|I_S|$) for $L = 0$ nm devices with varying design widths: (a) 60 nm, (b) 70 nm, (c) 80 nm, and (d) 90 nm. Clear Coulomb diamonds are visible across all devices [150, 162].

positive V_G range compared to the other nanotransistors. This shift appears particularly significant mainly due to the small statistical number of samples for which a stability diagram was measured. Actually, additional devices were found to be showing SET conduction in similar high V_G ranges, but they were difficult to characterize because of gate leakage. These V_G variations are attributed to device-to-device variability characteristic of random dopant networks, arising from local fluctuations and non-uniformities.

The stability diagrams of three $L = 20$ nm devices were acquired and are reported in Figure 4.21. For $L = 20$ nm samples (Figure 4.21), a wider design $W = 100$ nm, ($W_{\text{eff}} \sim 50$ nm) is required for conduction. The increased channel area likely incorporates a higher number of donor-induced QDs, making the stability diagrams more complex, particularly at higher V_G. This results in a high number of different conductive paths between QDs and more complex transfer characteristics but a higher probability of identifying SET features.

The subsequent analysis of the stability diagrams focuses on two $L = 0$ nm devices: (a) and (c) from Figure 4.20. Sample (d) appears to exhibit the most well-defined diamonds, although it is the consequence of the finer measurement resolution employed. However, the stability diagram is strongly asymmetric in V_D, indicating a significant displacement of the position of the QDs within the Si nanochannel. This leads to significantly different tunnel barriers and capacitive coupling to S and D, ultimately complicating the extraction of physical parameters. Sample (b) is also excluded from the discussion as it exhibits excessively high resistance, characteristic of the very open Coulomb diamonds observed. Therefore,

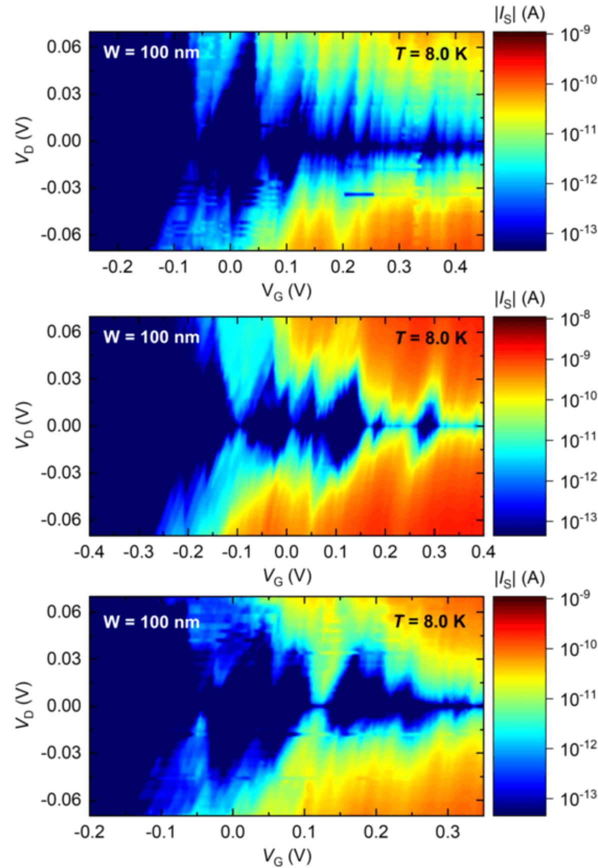


Figure 4.21: Stability diagrams for L = 20 nm devices (W_{des} = 100 nm). The increased channel area allows for more QDs, leading to more complex stability diagrams.

samples (a) and (c) were selected for further investigation as they exhibit the most symmetric and consistent data for a reliable analysis.

4.3.4 Transfer characteristics and stability

The stability diagram at T = 8.0 K for the sample with $W_{des} = 60$ nm and L = 0 nm (Device a in Figure 4.20a) is shown in Figure 4.22. The gate voltage is varied from $V_G = -0.4$ V to +0.3 V. The drain voltage is varied from $V_D = -0.07$ V to +0.07 V. The top and bottom graphs in Figure 4.22 reports the transfer characteristics traces for three positive (top) and negative (bottom) V_D values.

The transfer characteristic and the stability diagram reveals several key characteristics of the device operation. A significant open region is observed for $V_G < -0.3$ V, where no conduction above the $\sim$ 10 fA noise background is measured regardless the drain

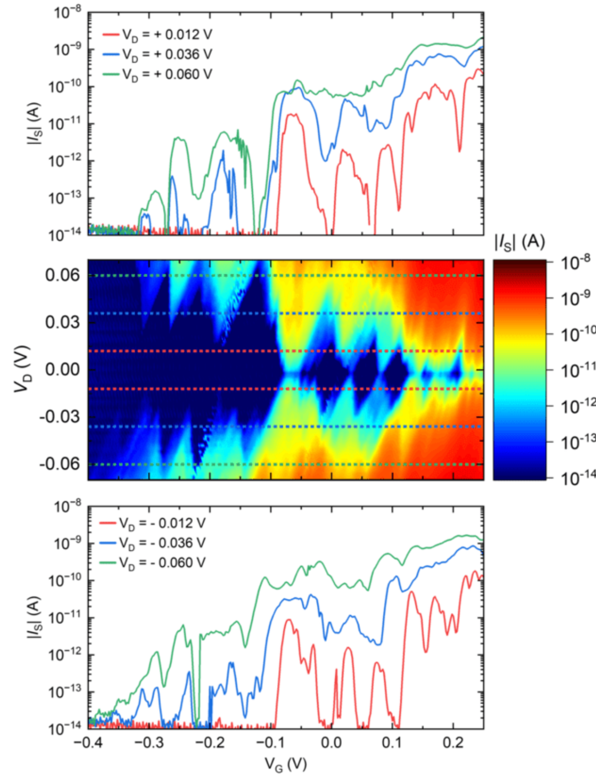


Figure 4.22: Stability diagram of L = 0 nm, W_{des} = 60 nm device. $|I_S|$-V_G transfer characteristics are shown for varying positive (top) and negative (bottom) V_D polarities.

voltage applied. This likely corresponds to the N = 0 electron state, where all QDs in the transport path are completely depleted of electrons. Therefore, the first observed current peak corresponds to the tunneling of the first electron into the deepest available ground-state energy level. The first Coulomb diamond corresponds to the stable N = 1 configuration. The enlargement of the Coulomb diamonds in this region suggests that one of the tunnel barriers, R_S or R_D, may be significantly large. In this regime, higher bias is required to align the electrochemical potentials, leading to stronger Coulomb blockade and significantly reduced current.

More energy levels become accessible increasing V_G. Actually, at high V_G, the minimum current between peaks remains above zero, indicating that the Coulomb blockade is no longer sufficient to completely prevent tunneling of additional electrons in the QD, causing the system to transition to a FET-like regime with superimposed current fluctuations from individual QDs. At the same time, increasing $|V_D|$, widens the transport window by increasing the energy offset between Fermi levels of the S and D. This allows the ground state as well as excited states and additional conductive paths to fall within the bias window, resulting in the observation of new or broadened current peaks.

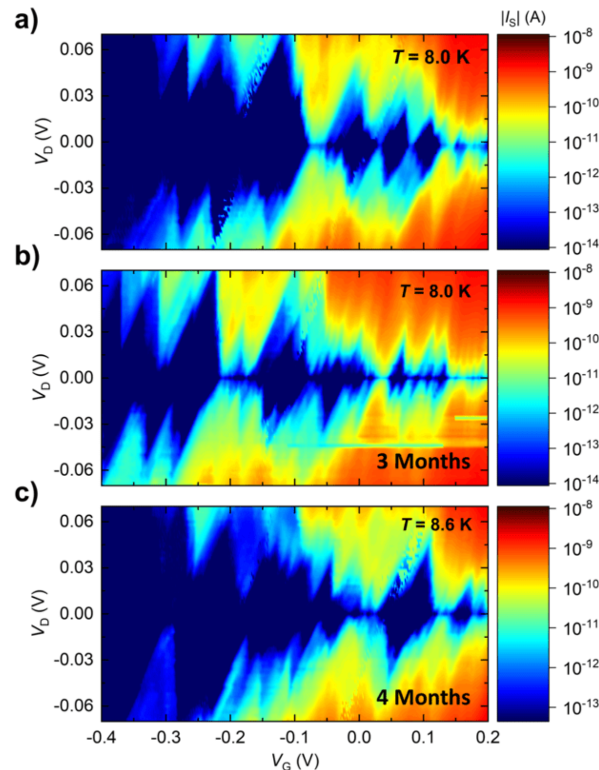


Figure 4.23: Comparison of stability diagrams for the same device over a period of four months. (a) Initial measurement. (b) After 3 months. (c) After 4 months. The slight difference in temperature is due to a small variation in the base temperature of the cryostat.

A small asymmetry is observed by changing the voltage polarity, which indicates a different coupling between the QD and the source (C_S) versus the drain (C_D) electrodes.

Sudden current jumps are observed at $V_G \sim -0.2$V, particularly visible at high $|V_D|$. Since the stability diagram is acquired by sweeping V_G at fixed V_D, these sudden jumps are not merely instrumental noise but rather manifestations of random telegraph noise (RTN). This RTN correlates with charging and discharging events in traps near the conduction path. These traps can be attributed to uncompensated B acceptors, isolated P donors, or interface states [163, 161]. Trap charging modifies the local electrostatic potential, causing a shift in the energy levels of the QD and consequently affecting the measured current, which appears as a discrete jump in the tranfer characteristic depending whether the trap is charged or not.

The same device was re-measured after multiple thermal cycles (T = 8 K to 300 K) over four months. Figure 4.23 reports the comparison of some of the stability diagrams acquired during that time. The core structure and functionality, including the prominent Coulomb blockade features and the persistent RTN features, were all preserved.

The most significant change is a shift in the working V_G range of the device. V_{th} is first

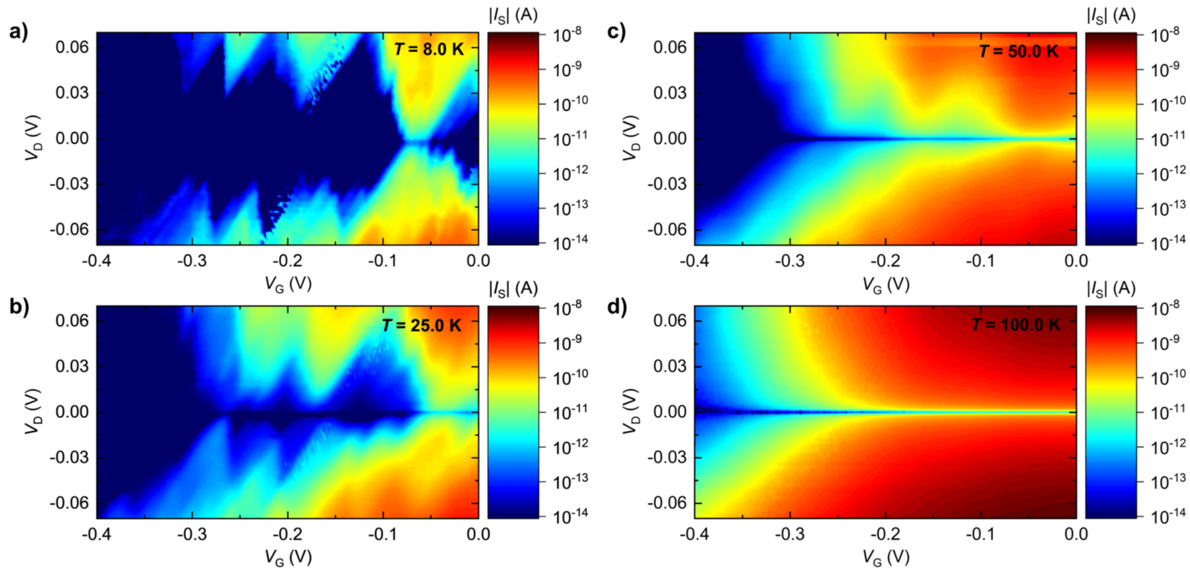


Figure 4.24: Evolution of the stability diagram showing the transition to FET behavior with increasing temperature: (a) 8 K, (b) 25 K, (c) 50 K, and (d) 100 K.

shifted toward a more negative bias over time (b) and then almost recovered after 4 months (c). This effect is likely caused by a change in the fixed charge density within the gate oxide or at the interface due to the repeated thermal cycles. This effect is a known artifact in MOS structures [7]. Closer inspection reveals finer changes in the observed peaks which suggest minor variations in the accessible energy levels, possibly due to charging and discharging of long-lived interface or fixed oxide traps between measurement cycles, which slightly modify the energy level distribution.

4.3.5 High-temperature operation

In order to investigate the high temperature functionality, the stability diagram of the same device was measured up to 100 K. Experimetal data are reported in Figure 4.24 for T = 8.0 K (a), T = 25.0 K (b), T = 50.0 K (c), and T = 100.0 K (d).

- $T \leq 25$ K: Clear Coulomb diamonds are observed. RTN features persist, indicating that the trap energy levels are deep enough to remain effective at this temperature. At T = 25 K, higher k_BT and reduced R_S and R_D values result in higher current and more closed Coulomb diamonds compared to T = 8.0 K.
- $T = 50$ K: The increased thermal energy broadens the current peaks, losing the distinct diamond shape. The device starts to behave as a conventional FET even though the superimposed SET conduction is clearly identified.

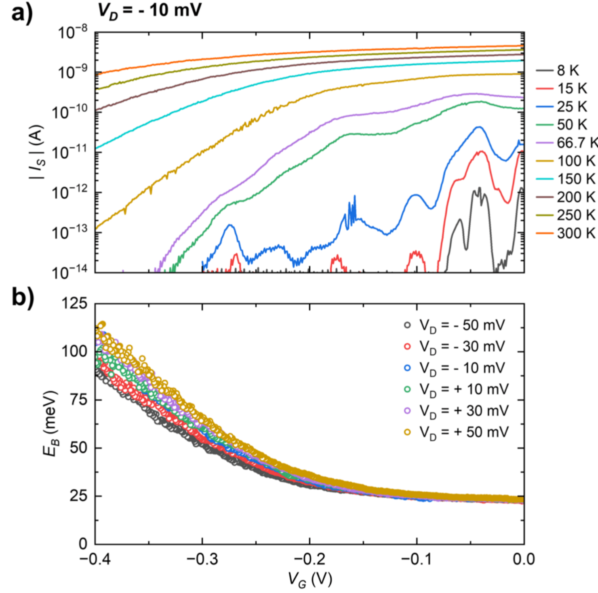


Figure 4.25: (a) Transfer characteristics at temperatures ranging from T = 8.0 K to 300 K for fixed $V_D = -10$ mV. (b) Extracted barrier height (E_B) as a function of V_G for each V_D values.

- T = 100 K: The device exhibits typical FET characteristics. V_{th} shifts to more negative V_G as T increases. Correctly, a stronger negative gate potential is required to deplete the channel, overcoming the increased thermal energy.

The transfer characteristics of the same device measured at T ranging from 8.0 to 300 K are shown in Figure 4.25a for a fixed $V_D = -10$ mV, chosen as an example. Increasing temperature correlates the thermal broadening of the SET peaks. Experimental data were used to extract the barrier height (E_B) by fitting the current as a function of the inverse temperature for a fixed V_G, following a thermally activated transport model:

$$I \propto \exp\left(-\frac{E_B}{k_B T}\right) \tag{4.7}$$

Figure 4.25b shows the evolution of E_B with V_G for each V_D, indicating that E_B increases as V_G approaches the OFF state and becomes more negative. Moreover, E_B slightly increases as V_D is changed from negative to positive. A positive V_D raises the drain energy level relative to the source, potentially increasing the effective tunnel barrier on the drain side.

As discussed, the first peak represent the transition between the $N = 0$ and $N = 1$ state. The conduction is therefore associated to the first electron tunneling in the lowest energy QD. Near the first peak, at $V_G \sim -0.3$ V, the extracted barrier height is $E_B \sim 50$ meV. This value is characteristic of a single donor QD or a cluster with only a few donors, despite the high nominal donor/acceptor concentrations. This observation is a key result of the co-doping

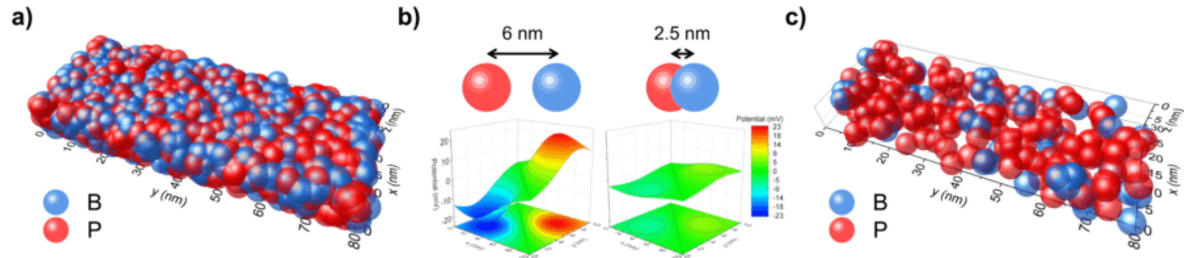


Figure 4.26: (a) Random distribution of P and B dopants in the SET nanochannel ($W = 30$ nm, $L = 80$ nm, $H_{SOI} = 8$ nm). (b) P–B compensation effect. (c) Simplified configuration showing only the uncompensated dopants that effectively contribute to conduction.

strategy, suggesting that the near-perfect compensation effectively isolates small P clusters, allowing them to function as individual, deep QDs.

The high barrier height ($\sim$ 50 meV) explains the persistence of Coulomb blockade features to intermediate temperatures ($\sim$ 50 K), significantly improving the thermal stability compared to devices limited by lower E_B values. Due to the random dopant distribution, other configuration and devices could show an even more significantly higher E_B due to B dopants favourably distributed in the nanoscale channel.

4.3.6 Statistical analysis of co-doping and multi-QD formation

Stability diagram measurements, especially the complex structure at high V_G, indicate that the observed configuration most likely originates from a multi-QD array, with each QD composed of a few dopant atoms. To test this hypothesis, a statistical analysis of the dopant distribution within the conductive channel was performed, focusing on the effect of co-doping and P-B compensation.

Although the nanotransistors operate through SET across Coulomb barriers, the device differs substantially from a single-atom QD. Due to the high dopant concentration, the transport mechanism involves the collective behavior of hundreds to thousands of dopants, while maintaining a similar ground-state alignment ($E_B \sim 50$ meV) as in simpler QD systems. Figure 4.26a shows a random distribution of P and B dopants within a representative nanochannel of dimensions $W = 30$ nm, $L = 80$ nm, and thickness 8 nm, consistent with SEM images and previous considerations.

In this particular configuration, the nominal concentrations were set to $n_A = 5.0 \times 10^{19}$ cm^{-3} for B and $n_D = 5.5 \times 10^{19}$ cm^{-3} for P. The concentration of B is based on SIMS data (Figure 4.18c). The active P concentration in the nanoscale channel is difficult to quantify, as it may differ from the values measured for the flat SOI sample due to quantum confinement, dielectric mismatch, and interface effects. This evaluation is especially difficult at the low temperature ($T = 8.0$ K) used in the analysis where a fraction of the P dopants could be deactivated due to freeze-out. Therefore, n_A was kept constant, and n_D was varied from

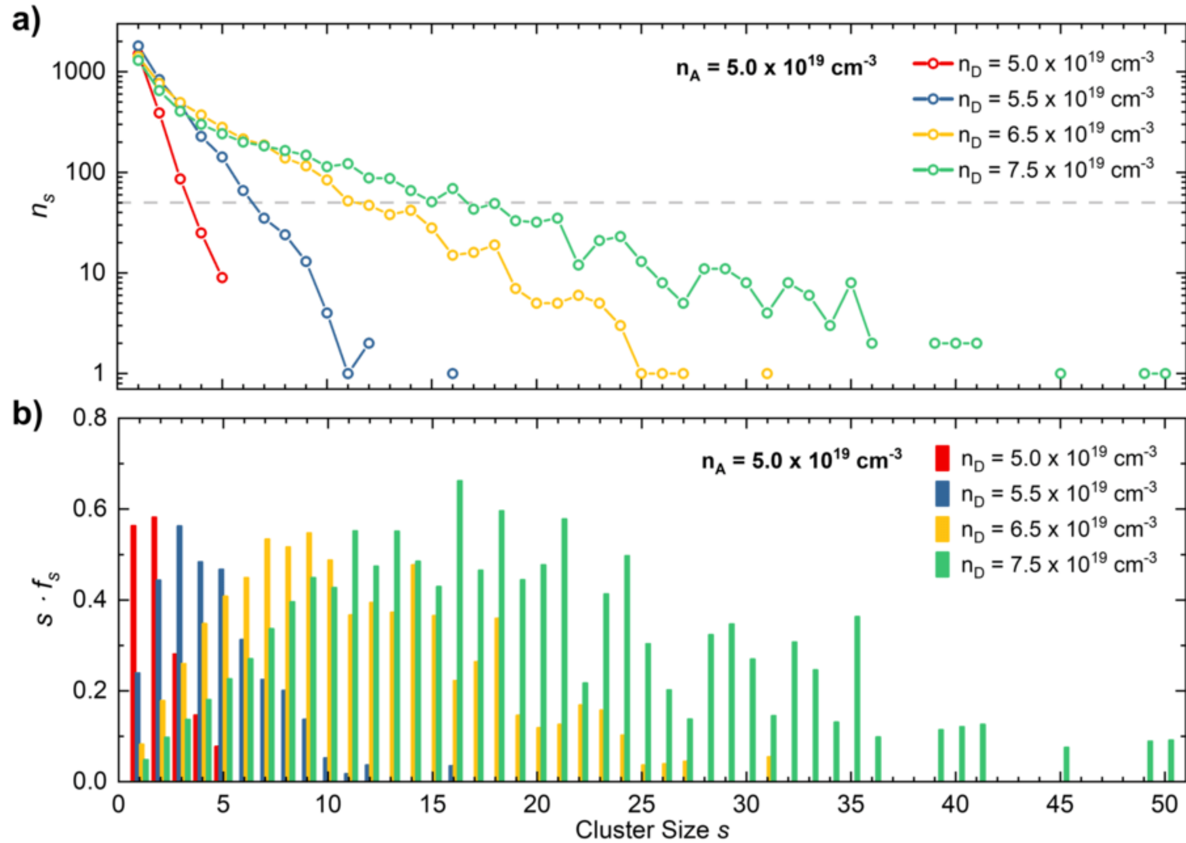


Figure 4.27: (a) Number of P clusters of size s (n_s) obtained over 50 statistical runs for different n_D. (b) Weighted probability sf_s of finding an atom in a cluster of size s.

5.0×10^{19} to 7.5×10^{19} cm^{-3}. If n_A is reduced, n_D should be scaled accordingly to maintain the compensation ratio.

To simplify the analysis, the compensation effect between P and B dopants was explicitly introduced (Figure 4.26b). When P and B atoms are separated by more than ~ 2.5 nm (r_B), they create local wells and barriers in the potential landscape, modifying it in opposite directions. However, when they are closer than r_B, their effects largely cancel out. P-B couples at a distance less than r_B are therefore removed. This compensation significantly reduces the number of active dopants contributing to conduction (Figure 4.26c). As n_D increases, more uncompensated P atoms remain in the channel, enhancing the formation of conductive P clusters.

The statistical distribution of dopants was simulated over 50 runs for each n_D value to analyze the variability in dopant positioning and compensation. Perfect compensation occurs at $n_D = 5.0 \times 10^{19}$ cm^{-3}, while $n_D = 7.5 \times 10^{19}$ cm^{-3} corresponds to a donor-rich regime. To identify QD clusters, P atoms within 4 nm of each other were grouped, defining

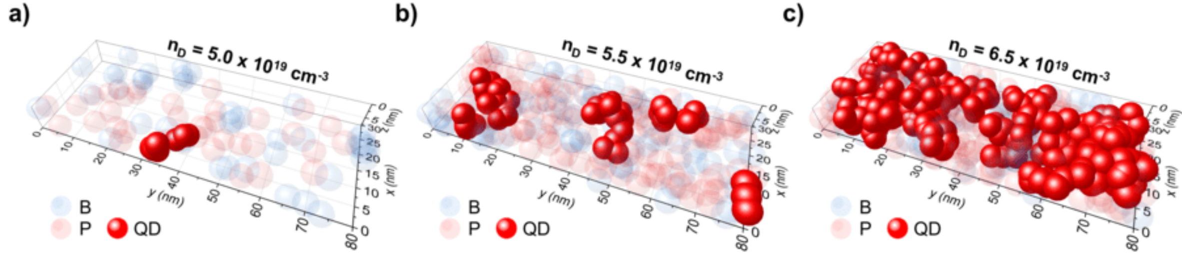


Figure 4.28: QD clusters ($s \geq 5$) in the SET nanochannel for $n_D = 5.0 \times 10^{19}$ cm^{-3} (a), $n_D = 5.5 \times 10^{19}$ cm^{-3} (b), and $n_D = 6.5 \times 10^{19}$ cm^{-3} (c).

the cluster size s and the number of clusters of a certain size n_s. Figure 4.27a shows the total n_s values after 50 runs. A value of $n_s = 50$ indicates that, on average, one cluster of that size is found in the channel in each run.

An increasing number of larger clusters is observed with higher n_D, indicating a gradual transition from isolated QDs toward extended, metallic regions. To quantify this, we define the probability of finding an atom in a cluster of size s as:

$$f_s = \frac{s n_s}{N_{TOT}}, \tag{4.8}$$

where N_{TOT} is the total number of P atoms in the channel. The weighted probability sf_s (Figure 4.27b) indicates and shows that for $n_D = 5.0 \times 10^{19}$ cm^{-3} most dopants are isolated or form small clusters, while increasing n_D results in larger, more metallic clusters. For $n_D = 5.5 \times 10^{19}$ cm^{-3}, the most likely configuration is found at $2 \leq s \leq 5$. On average, each run contains a handful of clusters in this size range, representing possible QDs in the nanochannel (Figure 4.27a). Already at $n_D = 6.5 \times 10^{19}$ cm^{-3}, the average cluster size suggests percolative connections and near-metallic conduction.

Figure 4.28 illustrates the spatial distribution of QDs (clusters with $s \geq 5$) for $n_D = 5.0$ (a), 5.5 (b), and 6.5×10^{19} cm^{-3} (c). At the lowest n_D, the channel contains few or no QDs, corresponding to a mostly insulating behavior. At intermediate concentration ($n_D = 5.5 \times 10^{19}$ cm^{-3}), discrete QDs are clearly formed and well separated. This configuration aligns with the experimentally observed stability diagrams and corresponds to the highest device yield. At higher n_D, the clusters merge, forming metallic paths that connect the S/D leads. Actually, clusters located adjacent to the S/D contacts (at $y = 0$ and $y = 80$ nm) should be excluded, as they effectively extend the metallic leads by reducing the effective channel length L.

A qualitative analysis of the 50 random runs obtained with $n_D = 5.5 \times 10^{19}$ cm^{-3} confirms the same trend. The positions of the biggest clusters obtained in the first 15 runs are reported in Figure 4.29. Most configurations show 1 to 4 small QDs composed of only a few dopants, in excellent agreement with the number of transport features extracted from the stability diagrams. Some runs yield no active QD of this size, possibly insulating, or

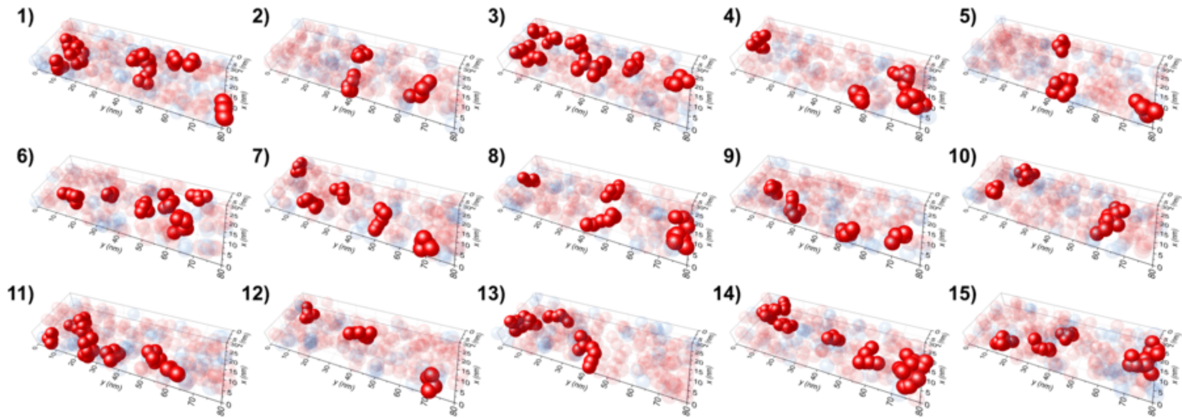


Figure 4.29: Visualization of 15 representative random runs showing the distribution of P-based QDs ($s \geq 5$) within the SET nanochannel.

elongated connected metallic clusters, matching the observed yield distribution. Reducing the dimensions of the channel, a significantly reduced number of QDs is formed, resulting in insulating behavior. Increasing W, promotes percolation pathways between the dopants atoms, favoring the interconnections between QDs and metallicity.

Overall, the simulations confirm that the experimentally observed configuration of multiple-QD arrays in the nanochannel, each composed of a few dopant per cluster, is naturally explained by co-doping-induced compensation. The presence of both donors and acceptors suppresses excessive metallic percolation paths and promotes the self-organization of discrete dopant clusters. This mechanism directly mitigates random dopant fluctuations and enhances the SET conduction regime, device reproducibility, and yield.

4.3.7 Coulomb blockade simulations and multi-QD analysis

Let's now consider the sample with $L = 0$ nm, $W = 80$ nm device (Device c in Figure 4.20), which exhibited the most defined stability diagram features. While the number and position of peaks vary between devices, this sample serves as a representative case to validate our multi-QD array transport model. This SET device shows a near-closed Coulomb diamond region, associated with the lowest tunneling resistances and operates in a positive V_G range, making its functionality at $V_G = 0$ V, normally-off. This suggests an increased ionization energy due to a deeper QD ground state and increased E_B, requiring a positive V_G to shift the energy levels into the source and drain tunneling window. The $|I_S| - V_G$ transfer characteristic for this sample at $V_D = -15$ mV is shown in Figure 4.30a. Three repeating current peaks are identified. These peaks are tentatively ascribed to three different, electrostatically independent quantum dot paths (QD_1, QD_2, QD_3). Independence, in this context, implies that the inter-dot coupling (C_{inter}) is significantly weaker than the coupling to the source and drain electrodes (C_S, C_D), making sequential tunneling through independent

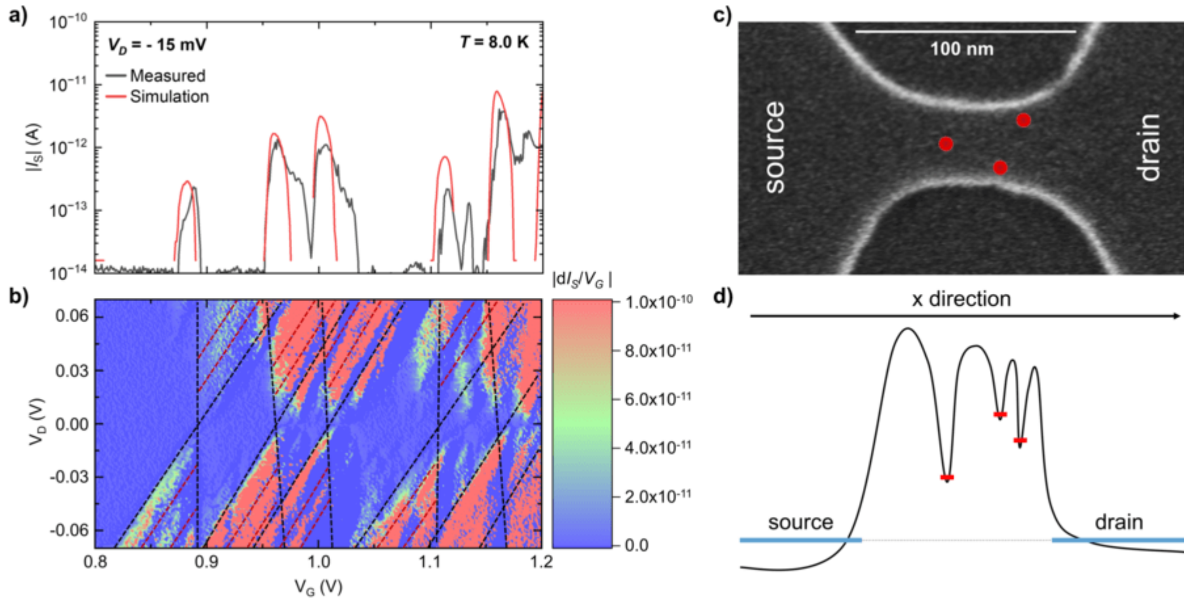


Figure 4.30: Analysis of the L = 0 nm, W = 80 nm device. (a) Transfer characteristic at $V_D = -15$ mV showing three distinct peak families. (b) V_D-V_G plot of the differential conductance ($|dI_S/dV_G|$) highlighting the boundaries of the three independent QDs. (c) SEM image of the nanochannel and schematic position of the three QDs. (d) Schematic potential profile along the channel, illustrating the different energy depths of the QDs.

dots the preferred transport mechanism over inter-dot hopping.

To confirm this hypothesis and resolve fine features, analysis of the slopes of the first derivative of the current ($|dI_S/dV_G|$) is performed on the V_D-V_G plot (Figure 4.30b). The analysis of the first derivative enhances the visualization of current variations, clearly delineating the slopes (black dashed lines) of the boundaries associated with the three QDs (Figure 4.30c). Each QD is further characterized by two sub-peaks (red dashed lines), which are consistent with the presence of multiple donors per cluster. While the three-QD model represents the primary transport path to ensure a reliable extraction of the parameters, these additional sub-peaks likely reflect the more complex internal energy level structure of the individual clusters rather than independent QDs, as schematically suggested in Figure 4.15b.

The experimental parameters were extracted from the stability diagram based on the periodicity and the slopes of the Coulomb diamond boundaries following eqs. 4.3 to 4.6.

Analysis of the periodicity (ΔV_G) determined the gate capacitance and size of the quantum dots: $C_{G,1} \sim 0.74$ aF and $C_{G,2} \sim C_{G,3} \sim 0.80$ aF. Using the parallel-plate model with $H_{SiO_2} \sim 2.8$ nm, the corresponding QD effective areas are $A_{QD,1} \sim 60$ nm^2 and $A_{QD,2} \sim A_{QD,3} \sim 65$ nm^2. This area corresponds to a QD radius of ~ 4—5 nm, which is compatible with a P cluster of a few dopants coupled near r_B. The coupling asymmetry (C_S/C_D) was determined from the slopes α^+ and α^-, in order to quantify the capacitive

Table 4.1: Extracted capacitance values for the three independent QDs.

QD	C_G (aF)	C_S (aF)	C_D (aF)	C_S/C_D
QD_1	0.74	0.047	0.030	1.57
QD_2	0.80	0.005	0.090	0.06
QD_3	0.80	0.005	0.050	0.10

coupling to the source and drain leads.

The extracted capacitance values are summarized in Table 4.1. The C_S/C_D ratio provides insight into the position of the QD within the channel and the relative proximity to the S or D leads.

- If $C_S/C_D > 1$: The QD is coupled more strongly to the source, implying it is located closer to the source electrode. ($QD_\mathbf{1}$)
- If $C_S/C_D < 1$: The QD is coupled more strongly to the drain, implying it is located closer to the drain electrode. ($QD_\mathbf{2}$ and $QD_\mathbf{3}$)

Based on this analysis, QD_1 is positioned almost in the middle of the channel, closer to the source, while QD_2 and QD_3 are situated closer to the drain.

The depth and ground state energy of the QDs is ordered based on the gate voltage required to identify the first electron tunneling through the QD. The QD that requires the most negative V_G to deplete and the most positive V_G to turn ON, as in this case, has the ground state positioned furthest away from the source energy level. The potential profile is schematically represented in Figure 4.30d, correlating the extracted positions, shown in Figure 4.30c, with the measured electrical behavior.

The extracted experimental parameters (C_G, C_S, C_D) were implemented into a Coulomb blockade simulator using a three-QDs equivalent circuit model. The tunnel resistances (R_S, R_D) and the ground state energy of each QD were adjusted to achieve the best fit for the experimental transfer characteristic (Figure 4.30a).

The reconstructed stability diagram (Figure 4.31, top) shows excellent agreement with the experimental results (Figure 4.31, bottom) in the low-V_G regime, successfully reproducing the initial Coulomb diamond patterns. Minor variations at higher V_G suggest that increasing the gate voltage activates more parallel transport paths not explicitly included in the three-QD model. Notably, the simulation predicted a peak corresponding to the $N = -1$ state of QD_3 at $V_G \sim 0.85$ V, which is not observed experimentally since the QD is already fully depleted and cannot lose an additional electron.

This section of the work demonstrates the electrical characterization of nanoscale, highly co-doped SOI-FETs exhibiting SET behavior at intermediate temperature. Despite the extremely high donor concentration ($n_D \sim 2 \times 10^{20}$ cm^{-3}), the device functionality is demonstrated by the presence of the co-doping effect introduced by the B acceptors, which significantly increases the probability of forming well-isolated and functional QDs. Both the

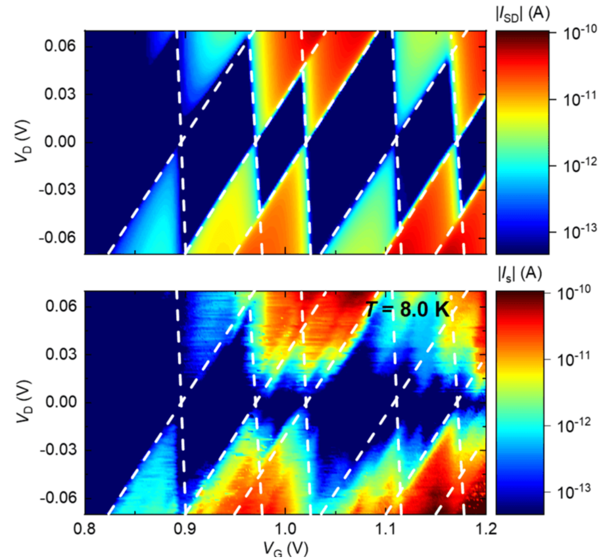


Figure 4.31: Comparison between simulated and experimental stability diagrams for the L = 0 nm, W = 80 nm device. (Top) Stability diagram reconstructed from the three-QDs equivalent circuit simulation. (Bottom) Experimental result at T = 8.0 K.

electrical data and statistical analysis, confirm that the co-doping induces a favorable near-complete compensation in the channel, isolating small clusters of P donors ($\sim 4-5$ nm radius) that act as QDs. This enables SET functionality in a high-concentration CMOS-compatible framework.

The enhanced thermal stability of the devices is evidenced by the measured barrier height of $E_B \sim 50$ meV, which is characteristic of a robust, deep-level QD configuration. This enhanced E_B allows the observation of Coulomb blockade features up to ~ 50 K, demonstrating the improved thermal stability crucial for practical applications.

Good scalability is shown by a significantly high SET yield of $\sim 30\%$ achieved despite the non-ideal gate oxide quality and thickness. This yield is exceptionally promising for a random dopant distribution device and indicates the robustness of the QD formation mechanism driven by co-doping.

Finally, multi-QD modeling was achieved and the complex experimental stability diagrams were successfully reproduced using an equivalent circuit for multiple independent QDs, confirming the multi-path transport mechanism and allowing for the extraction of key physical parameters like QD position, size and energy distribution.

The implementation of viable SET devices through a CMOS-compatible co-doping approach in Si nanostructures demonstrates significant progress toward *Beyond CMOS* technologies. The co-doping method enables the frequent formation of QDs with a high experimental yield, allowing SET nanotransistors to operate reliably up to intermediate temperatures and stable for long time scales. While the specific QD configurations vary due to the random

nature of the dopant distribution, the underlying physical mechanism is shown to be consistent, allowing for the successful modeling of complex transport characteristics through a representative multi-QD array approach. This platform could facilitates key applications such for ultra-low power logic, single-electron memory and precise single-charge pumping applications, highlighting the potential of co-doped Si nanostructures for energy-efficient, scalable, and quantum electronic devices.

Chapter 5

Conclusions and outlook

The research work presented in this thesis focuses on the characterization of charge transport in ultrathin SOI nanofilms and the implementation of device concepts for *beyond-CMOS* applications on the doped SOI platform. This final chapter summarizes the main results obtained in the investigation of dopant behavior and transport properties in these nanostructures.

In the first part of the thesis work we focused on the assessment and validation of a mild and flexible doping protocol to effectively and precisely control the doping of ultrathin SOI. We demonstrated the feasibility of extending this doping approach based on P end-terminated polymers to the nanoscale, in a process fully compatible with large-scale integration. A new processing approach, referred to as the *Double Annealing* approach, was developed to enable the injection of a significantly reduced dopant fraction into the device layer (Section 3.2). This method addressed one of the challenges associated with this technique, reducing the dopant dose due to the inherent relatively small size of the polymer molecules involved. Importantly, this technique allows independent tuning of the dopant dose regardless of the polymer molar mass, shifting the control from the chemistry and encumbrance of the molecules to the processing parameters. Furthermore, a complete lithographic protocol was introduced to accurately define mesa and test structures, particularly in the vdP configuration, to greatly improve the accuracy and repeatability of the measurements compared to the previous method based on shadow masks (Section 3.3).

This technology allowed the fabrication of ultrathin SOI substrates having a uniform concentration of P impurity atoms into the Si device layer. Accordingly, extensive investigation of charge transport in ultrathin SOI substrates was performed to discriminate among different effects associated to SiO_2/Si interface characteristics and effective confinement of charges into extremely thin films. Room temperature measurements demonstrated optimal electrical properties in SOI samples with $H_{SOI} \sim 30$ nm, consistent with literature data for similarly P doped bulk Si substrates (Section 3.4). μ_e was in excellent agreement and the n_e was fully described by the bulk incomplete ionization model of Altermatt. These results suggest full activation and ionization of the dopants at room temperature with this technique in a wide range of P concentration, Low-temperature analysis confirmed that the

activation energy of the dopants followed the expected decrease with higher n_D, indicating that 30 nm-thick films exhibit bulk-like behavior in this concentration range.

However, when H_{SOI} was reduced below 30 nm, a significant deviation from bulk behavior was observed. Samples showed an apparent incomplete dopant ionization at room temperature, with the N_e/N_D ratio significantly decreasing as both H_{SOI} and n_D were reduced (Section 3.6). In this regime, transport became dominated by interface effects due to the increased surface-to-volume ratio. The main contribution originated from interface states at non-passivated SC2-SiO_2/Si interfaces, which introduced acceptor-like energy levels within the Si bandgap, trapping a large fraction of free carriers and leading to the apparent incomplete ionization.

The resulting spatial charge depletion near the interface effectively reduced the electrically active thickness H_{eff}, confining the conduction in a thinner layer closer to the buried BOX interface. The presence of unscreened ionized centers correlated with a marked reduction in μ_e at room temperature in the ultrathin samples, attributed to the enhanced impurity scattering. To mitigate these effects, several capping and passivation strategies were explored. Among them, RTO proved most effective, substantially improving interface quality, reducing the P_b-center signal observed, and lowering the measured D_{it}.

SOI samples with RTO-SiO_2/Si capping layer exhibited an almost complete recovery of both n_e and μ_e at room temperature. Interestingly, in samples with nearly perfect interface passivation, that were measured quickly after HF treatment, enhancement in carrier mobility due to 2D confinement was observed, as the average distance between ionized impurities (d_{ave}) approached H_{SOI} (Section 3.5). When $H_{SOI}/d_{ave} \sim 1$ the progressive shift to 2D conduction results in 2D Coulomb scattering which greatly reduce the intensity of impurity scattering contribution due to the reduced number of neighboring ions compared to 3D bulk Si.

Correctly curing the interface states upon RTO, it was possible to investigate additional confinement-related effects on dopant behavior. Low-temperature measurements of R_s and N_e revealed a transition from metallic to semiconducting behavior for samples with similar high $n_D \sim 6 \times 10^{18}$ cm^{-3} as H_{SOI} decreased from 30 nm to 10 nm. This result demonstrated the distinct nature of the metal-insulator transition (MIT) in 2D nanostructures completely different than in bulk Si. For the first time in Si films, it highlighted the role of dielectric mismatch between the Si layer and the surrounding SiO_2. This mismatch between the dielectric permittivity of Si and SiO_2 and the ultrascaled 2D geometry resulted in an increase of the ionization energy of the dopants, shifting the MIT toward significantly higher n_D at the nanoscale.

Because of extremely precise control of the SOI material parameters, mainly H_{SOI} and n_D, as well as the control of the dielectric and its interface, it is possible to directly correlate these quantities with the dopant activation energy and systematically investigate their combined influence on transport. Further systematical investigation is needed to clarify how dielectric mismatch modifies the ionization energy as a function of H_{SOI} and n_D, and how this effect could couple with quantum confinement in ultrathin SOI when the Si device layer thickness

is scaled below 10 nm. The results reported herein defines the methodological background and the scientific landscape to properly tackle these fundamental phenomena.

The evidence of some of these quantum phenomena has already been explored in this work. At very low temperatures, highly doped samples exhibited an unexpected upturn of the measured R_s, even in the metallic regime. This increase was correlated with the 2D conduction regime and tentatively attributed to a Kondo effect arising from exchange interactions between conduction electrons and the localized magnetic moments exhisting in dopant clusters at high P concentration (Section 3.7). Fitting the experimental data using a Kondo model, followed by normalization to the universal Kondo curve, supported this interpretation. Moreover, the extracted Kondo temperature (T_K) exhibited a clear upward shift toward higher temperatures with increasing 2D confinement, consistent with the enhanced interaction strength in reduced dimensionality systems.

Low-temperature transport in highly doped ultrathin films confirmed the transition to the 2D conduction regime when reducing H_{SOI}. Negative magnetoresistance revealed WL effects, signature of coherent quantum interference in confined systems. HLN fits of the negative WL data yielded an α-prefactor close to unity and l_Φ values exceeding the sample dimensions at low temperature. Furthermore, the evolution with temperature of l_Φ followed the expected $T^{-1/2}$ behavior for the 2D systems, confirming the quantum coherent nature of conduction in these ultrathin Si nanofilms.

These promising features suggest the possibility of engineering graphene-like band structures in doped 2D Si films by introducing the periodic honeycomb topological modulations. Preliminary tests toward this objective successfully transferred the topology of a BCP cylinder mask into the Si device layer via RIE, serving as an initial step toward this objective (Section 3.8). Further investigation is still needed to improve the anisotropy and uniformity of the pattern transfer, and provide the complete characterization and demonstration of the resulting honeycomb structure.

The experimental results demonstrate the development of a versatile platform that provides unparalleled insight into fundamental physical phenomena in confined Si systems. This deep understanding enables the design of innovative device structures that exploit the unique electronic properties of doped SOI substrates.

Building on this platform, some of the advanced device concepts implemented on doped SOI substrates were presented in the second part of the thesis work. An experimental protocol was developed to achieve precise mesa patterning and device fabrication through sequential photolithography steps, enabling the realization of well-defined device masks. Using this approach, masks for junctionless transistors (Section 4.2) and multi-electrode devices (Section 4.1) were successfully designed and fabricated demonstrating, the complete Si-based processing workflow necessary for such structures, which was previously not investigated in the laboratory.

In the case of SOI Dopant Network Processing Units (SOI-DNPU), transfer characteristics revealed that, at microscale dimensions, the combined effect of the BOX and the presence of a small Schottky barrier at the Al/Si contact interface introduces pronounced nonlinearity in

the IV behavior between two contacts. Moreover, the transport characteristics were found to be tunable by applying a control voltage polarization to one of the electrodes located near the output terminal. Initial experiments already demonstrated NDR, a fundamental property enabling nonlinear computation and the implementation of linearly inseparable classification operations in unconventional and neuromorphic architectures. This intrinsic nonlinearity is of particular interest for *beyond-CMOS* applications, where nonlinear transfer functions are essential for emerging computational paradigms.

The final part of this work focused on the low-temperature characterization of dopant-based QDs arrays in Si nanotransistors (Section 4.3). Specifically, the feasibility of employing co-doping with P and B in highly doped channels was explored as a strategy to promote the formation of QDs through compensation effects, random spatial distribution, and dopant fluctuations. Clear identification of Coulomb blockade and Coulomb diamonds was obtained in the transfer characteristics and the stability diagrams. Co-doping yielded devices with remarkably high stability and reproducibility, maintaining consistent behavior over multiple thermal cycles and several months of measurements. Despite the elevated dopant concentration, these devices exhibited barrier heights comparable to those observed in QDs formed by only a few dopant atoms, enabling SET signatures even at moderate temperatures (up to $T \sim 70$ K). Furthermore, by exploiting random dopant fluctuations, the effective barrier height and charging energy could be further enhanced.

The electronic properties and spatial distribution of the QDs within the conductive nanochannels were quantitatively extracted by fitting of the slopes of the stability diagrams and validated through the comparison with Coulomb blockade simulation of the equivalent three QD circuit, confirming the single-electron nature of transport in these co-doped Si nanostructures.

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